



N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS(min)} (V)	$R_{DS(on)}\left(\Omega\right)$	V _{GS(th)} (V)	I _D (mA)		
60	1.40 at V _{GS} = 10 V	1 to 2.5	500		

SC-89 S₁ G₂ G₂ Marking Code: E Top View

Ordering Information: Si1026X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low On-Resistance: 1.40 Ω
 Low Threshold: 2 V (typ.)
 Low Input Capacitance: 30 pF
- Fast Switching Speed: 15 ns (typ.)
- Low Input and Output Leakage
- ESD Protected: 2000 V
- Miniature Package
- Compliant to RoHS Directive 2002/95/EC

BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- · High-Speed Circuits
- Low Error Voltage
- Small Board Area

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- · Battery Operated Systems
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	60		V	
Gate-Source Voltage		V_{GS}	± 20			
Continuous Dusin Comment /T 150 90\8	T _A = 25 °C	I _D	320	305		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 85 °C		230	220		
Pulsed Drain Current ^b		I _{DM}	- 650		mA	
Continuous Source Current (Diode Conduction) ^a		I _S	450	380		
M	T _A = 25 °C	P _D	280	250	mW	
Maximum Power Dissipation ^a	T _A = 85 °C		145	130		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V	

Notes:

- a. Surface mounted on FR4 board.
- b. Pulse width limited by maximum junction temperature.

ROHS COMPLIANT HALOGEN FREE

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			<u>'</u>	<u>'</u>			
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	60			v	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 0.25 \text{ mA}$	1		2.5		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$		± 150	m A	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 50	nA	
Zava Cata Valtaga Dvain Current	1	V _{DS} = 60 V, V _{GS} = 0 V		1		μΑ	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			10	1	
		V _{DS} = 10 V, V _{GS} = 4.5 V	500			1	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 7.5 \text{ V}, V_{GS} = 10 \text{ V}$	800			mA	
Drain-Source On-Resistance ^a		$V_{GS} = 4.5 \text{ V}, I_D = 200 \text{ mA}$			3.0		
	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$			1.40	Ω	
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}, T_J = 125 \text{ °C}$			2.50		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 200 mA		200		mS	
Diode Forward Voltage ^a	V_{SD}	V _{GS} = 0 V, I _S = 200 mA			1.40	V	
Dynamic ^b							
Total Gate Charge	Q_g			600			
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, I_D = 250 \text{ mA}, V_{GS} = 4.5 \text{ V}$		120		рС	
Gate-Drain Charge	Q_{gd}			225			
Input Capacitance	C _{iss}			30			
Output Capacitance	C _{oss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		6		pF	
Reverse Transfer Capacitance	C _{rss}	I = I WINZ		3			
Switching ^{b, c}							
Turn-On Time	t _(on)	V_{DD} = 30 V, R_L = 150 Ω		15			
Turn-Off Time	t _(off)	I_D = 200 mA, V_{GEN} = 10 V, R_g = 10 Ω		20		ns	

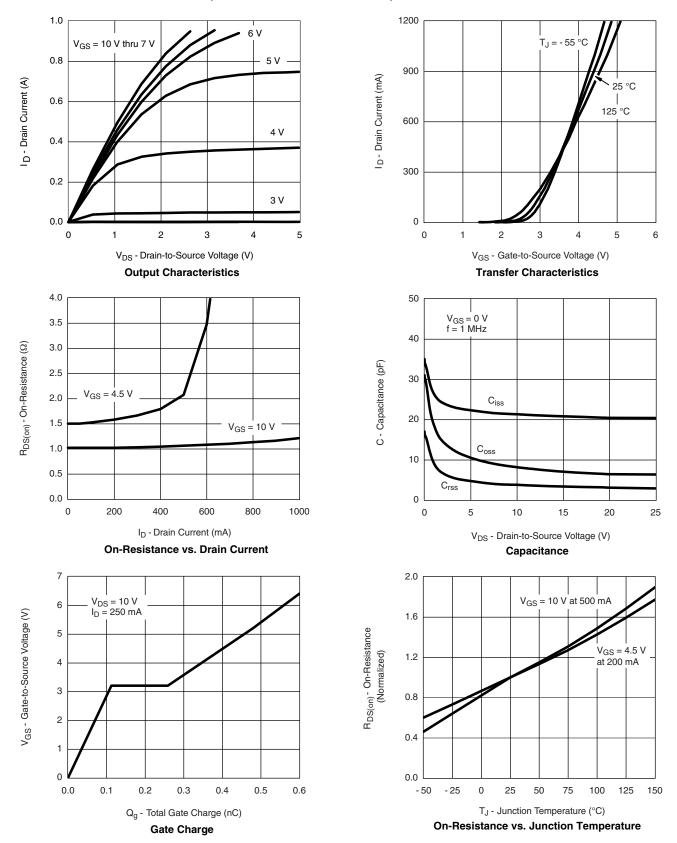
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. For DESIGN AID ONLY, not subject to production testing.
- c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



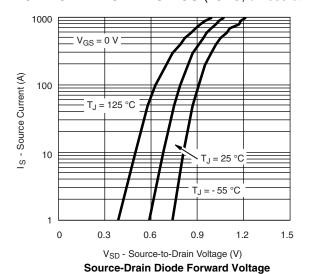
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

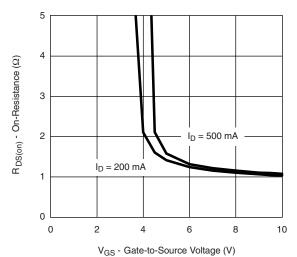


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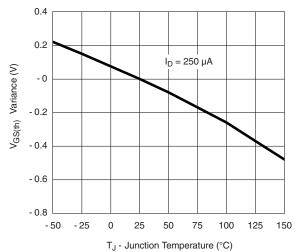
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

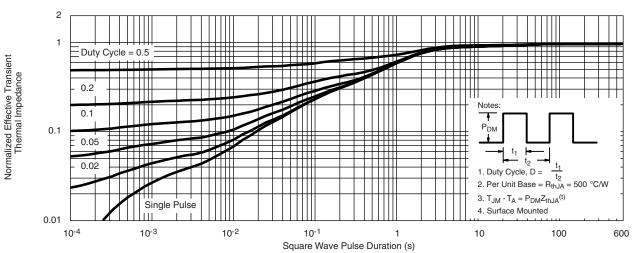




On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage Variance Over Temperature

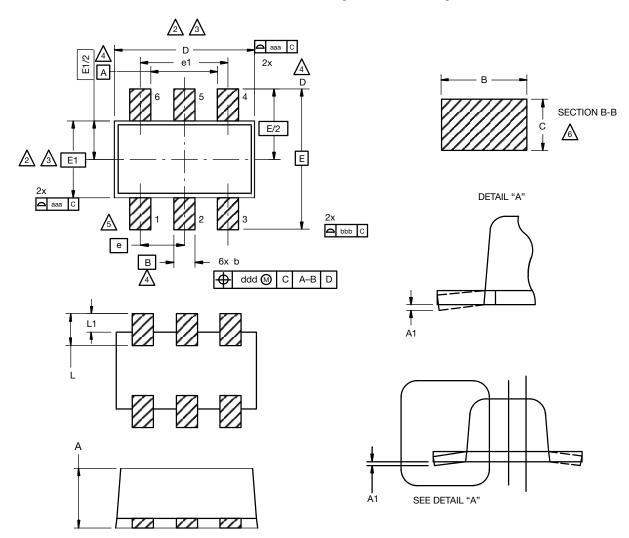


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71434.



SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

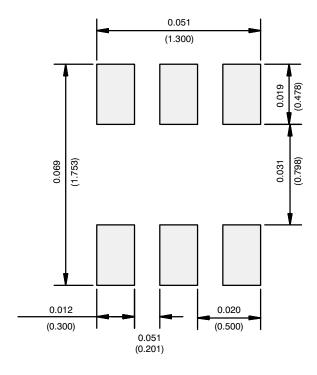
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS			
	MIN.	NOM.	MAX.	
Α	0.56	0.58	0.60	
A1	0	0.02	0.10	
b	0.15	0.22	0.30	
С	0.10	0.14	0.18	
D	1.50	1.60	1.70	
E	1.50	1.60	1.70	
E1	1.15	1.20	1.25	
е	0.45	0.50	0.55	
e1	0.95	1.00	1.05	
L	0.25	0.35	0.50	
L1	0.10	0.20	0.30	
C14-0439-Rev. C, 11-Aug-14 DWG: 5880				



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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