4 MHz, 7 nV/√Hz, Low Offset and Drift, High Precision Amplifier

Enhanced Product

ADA4077-2-EP

FEATURES

- Low offset voltage and low offset voltage drift
  - Maximum offset voltage: 90 µV at T_A = 25°C
  - Maximum offset voltage drift: 1.2 µV/°C
- Moisture sensitivity level 1 (MSL1) rated
- Low input bias current: 1 nA maximum at T_A = 25°C
- Low voltage noise density: 6.9 nV/√Hz typical at f = 1000 Hz
- CMRR, PSRR, and A_V > 120 dB minimum
- Low supply current: 400 µA per amplifier typical
- Wide gain bandwidth product: 3.9 MHz at V_{SY} = ±5 V
- Dual-supply operation: ±2.5 V to ±15 V
- Unity gain stable
- No phase reversal

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available upon request

APPLICATIONS

- Process control front-end amplifiers
- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls: thermocouples, RTDs, strain gages, and shunt current measurements
- Precision filters

PIN CONNECTION DIAGRAM

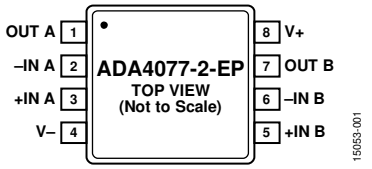

Figure 1.

GENERAL DESCRIPTION

The dual ADA4077-2-EP amplifier features extremely low offset voltage and drift, and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, and strain gages), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4077-2-EP is useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

Unlike amplifiers by some competitors, theADA4077-2-EP has an MSL1 rating that is compliant with the most stringent of assembly processes, and is specified over the extended industrial temperature range from −55°C to +125°C for the most demanding operating environments.

The ADA4077-2-EP is available in an 8-lead MSOP.

Additional application and technical information can be found in the ADA4077-2 data sheet.

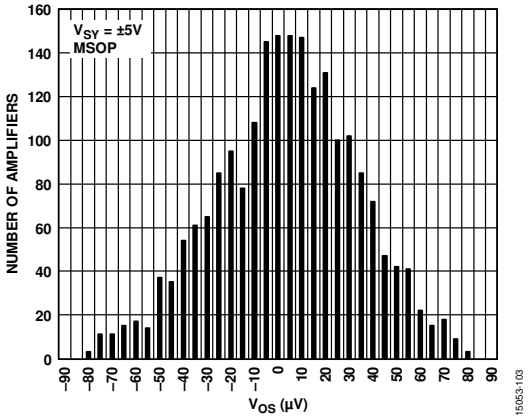

Figure 2. Offset Voltage Distribution

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

12/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	90	µV
		−55°C < T_A < +125°C			220	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C < T_A < +125°C		0.5	1.2	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−55°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA
		−55°C < T_A < +125°C	−1.0		+1.0	nA
Input Voltage Range			−3.8		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.8 V to +3 V	122	140		dB
		V_{CM} = −3.8 V to +3 V, −55°C < T_A < +85°C	120			dB
		V_{CM} = −3.8 V to +2.8 V, 85°C < T_A < 125°C	120			dB
Large Signal Voltage Gain	A_V	R_L = 2 kΩ, V_O = −3.0 V to +3.0 V	121	130		dB
		−55°C < T_A < +125°C	120			dB
Input Capacitance	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	3.8			V
		−55°C < T_A < +125°C	3.7			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−3.8	V
		−55°C < T_A < +125°C			−3.7	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.6 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−55°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	450	µA
		−55°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		3		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.9		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		55		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		µV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ELECTRICAL CHARACTERISTICS, ±15 V

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	90	µV
		−55°C < T_A < +125°C			220	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C < T_A < +125°C		0.5	1.2	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−55°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA
		−55°C < T_A < +125°C	−1.0		+1.0	nA
Input Voltage Range			−13.8		+13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.8 V to +13 V	132	150		dB
		−55°C < T_A < +125°C	130			dB
Large Signal Voltage Gain						
	A_V	R_L = 2 kΩ, V_O = −13.0 V to +13.0 V	125	130		dB
		−55°C < T_A < +125°C	120			dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	13.8			V
		−55°C < T_A < +125°C	13.7			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−13.8	V
		−55°C < T_A < +125°C			−13.7	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−55°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	µA
		−55°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/µs
Settling Time to 0.01%	t_S	V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		16		µs
Settling Time to 0.1%	t_S	V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		10		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.6		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.5		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		58		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		µV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Maximum Reflow, Soldering (10 sec)	260°C
ESD Human Body Model (HBM)[2]	6 kV
Field Induced Charge Device Model (FICDM)[3]	1.25 kV

[1] The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] ESDA/JEDEC JS-001-2011 applicable standard.
[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RM-8[1]	170	77	°C/W

[1] Thermal impedance simulated values are based on JEDEC JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

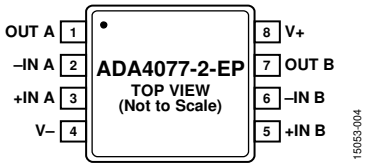

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

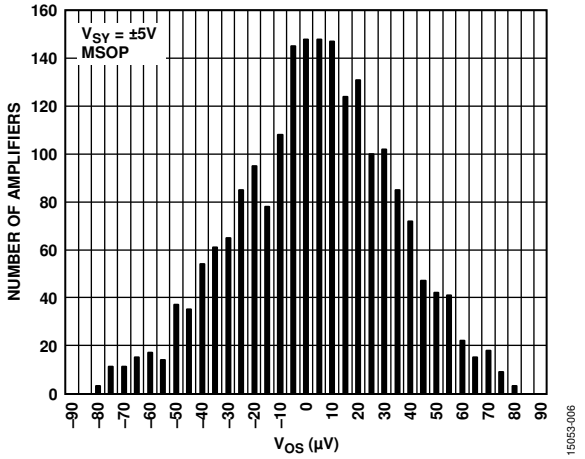

Figure 4. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

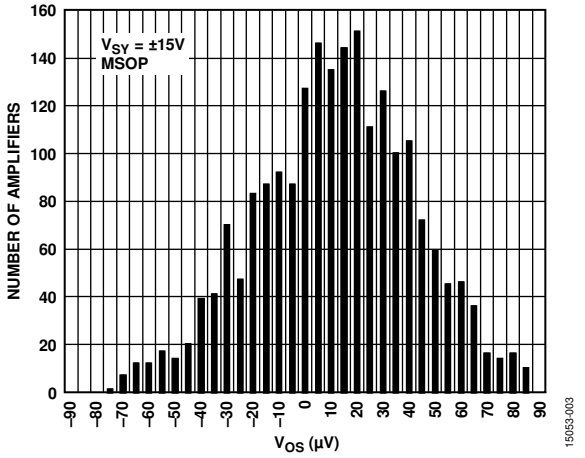

Figure 7. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

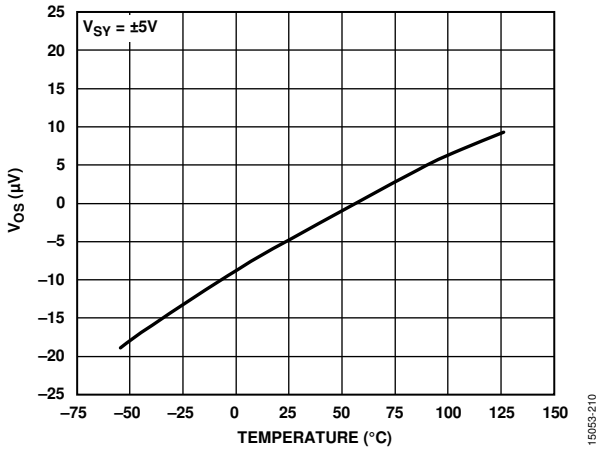

Figure 5. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V

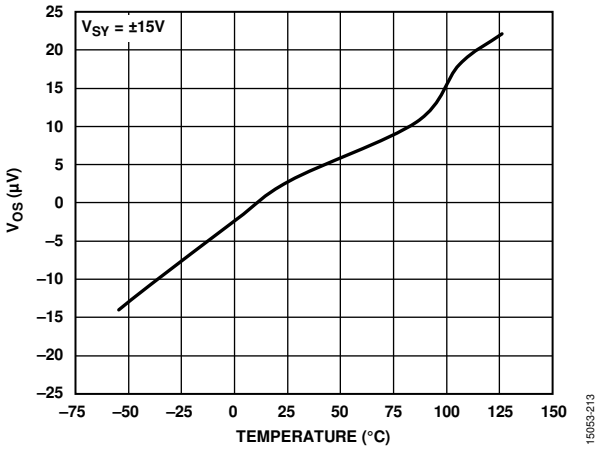

Figure 8. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V

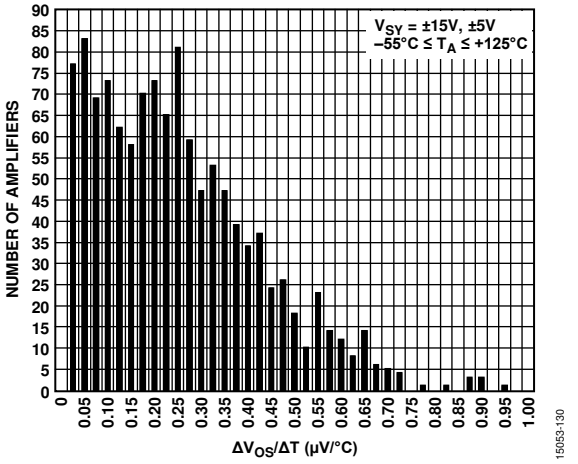

Figure 6. Offset Voltage Drift ($\Delta V_{OS}/\Delta T$) Distribution

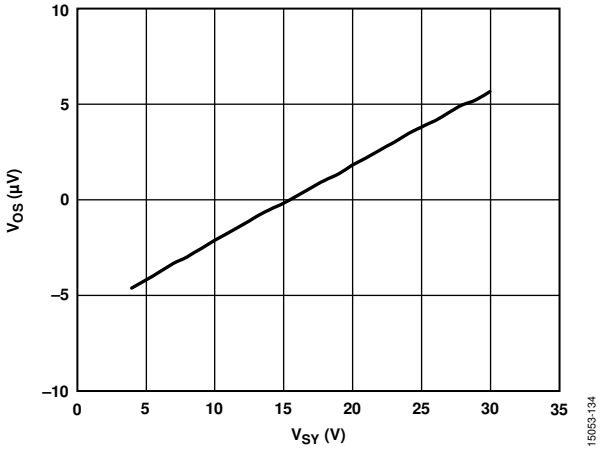

Figure 9. Offset Voltage (V_{OS}) vs. Power Supply Voltage (V_{SY})

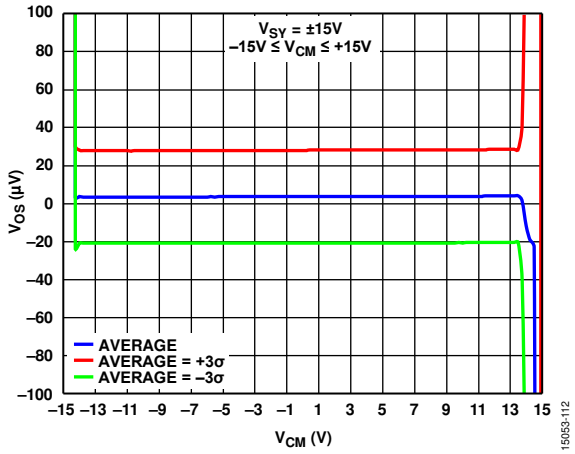

Figure 10. Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V

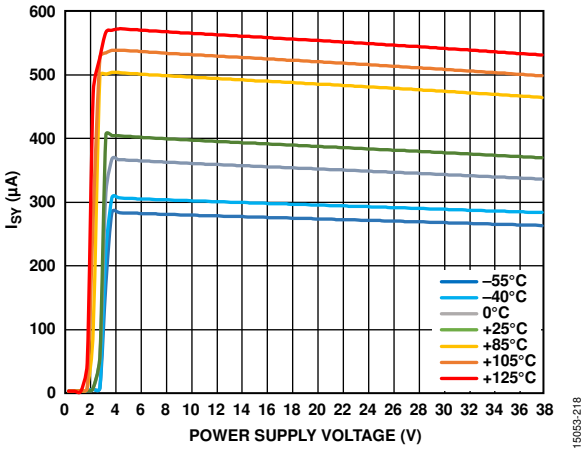

Figure 13. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

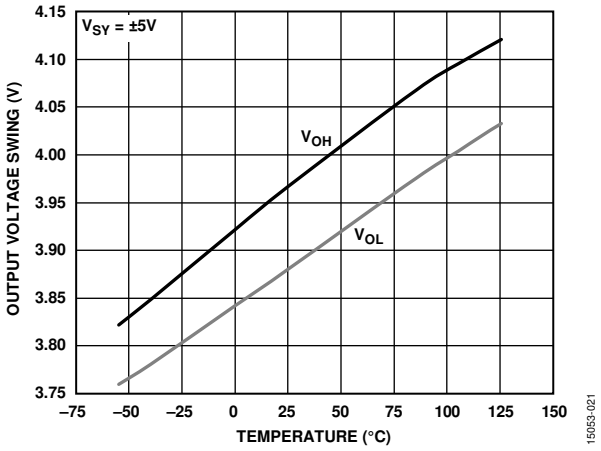

Figure 11. Output Voltage Swing vs. Temperature, V_{SY} = ±5 V

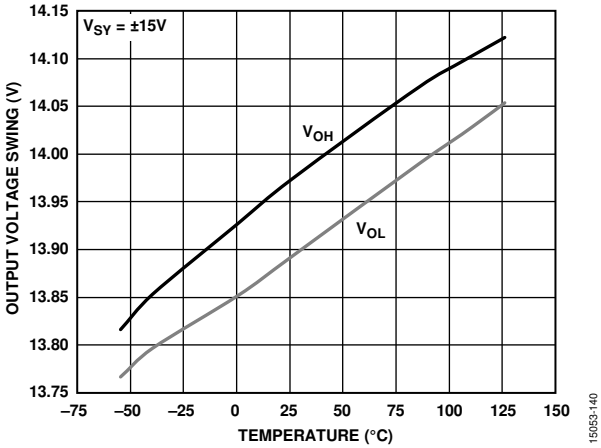

Figure 14. Output Voltage Swing vs. Temperature, V_{SY} = ±15 V

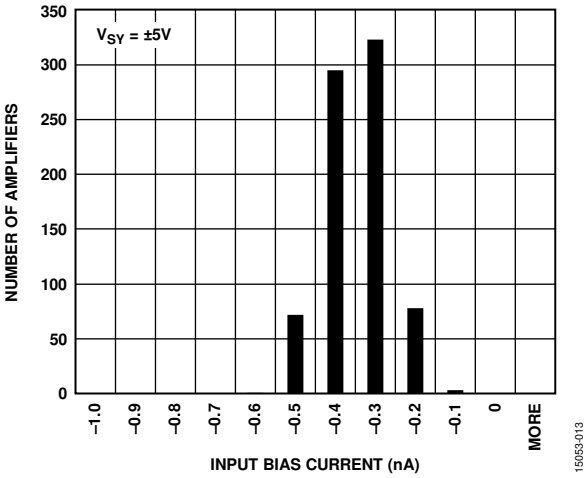

Figure 12. Input Bias Current Distribution, V_{SY} = ±5 V

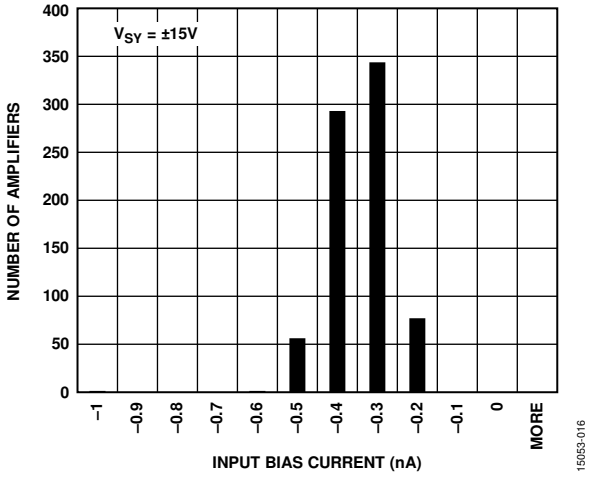

Figure 15. Input Bias Current Distribution, V_{SY} = ±15 V

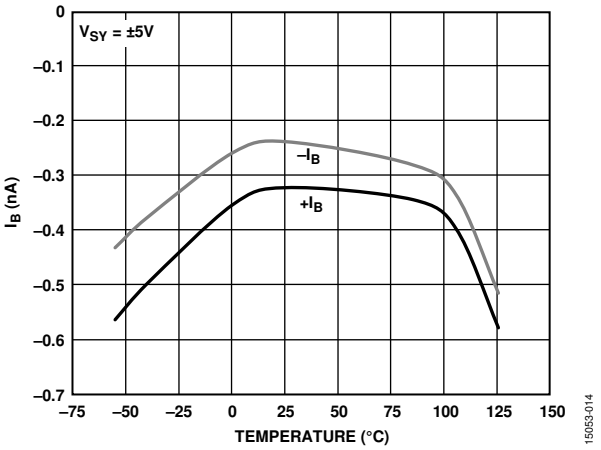

Figure 16. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

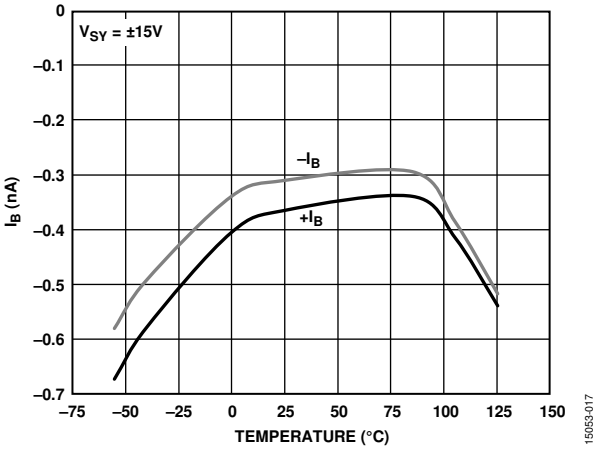

Figure 19. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

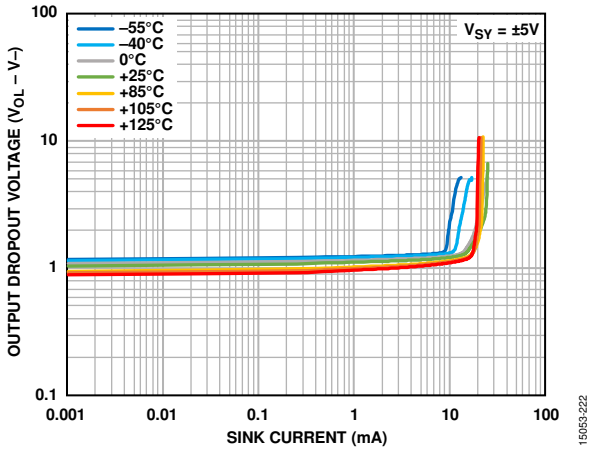

Figure 17. Output Dropout Voltage vs. Sink Current, V_{SY} = ±5 V

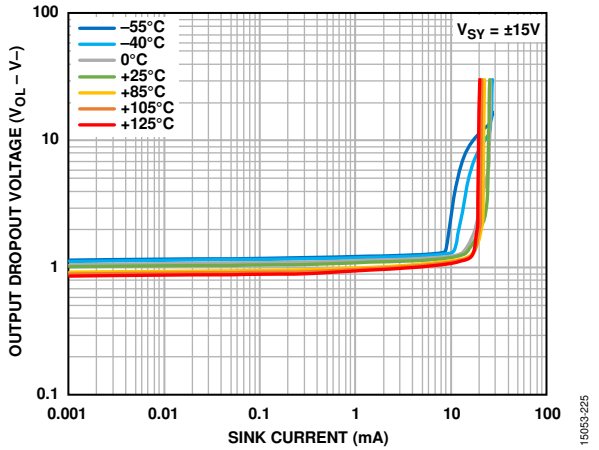

Figure 20. Output Dropout Voltage vs. Sink Current, V_{SY} = ±15 V

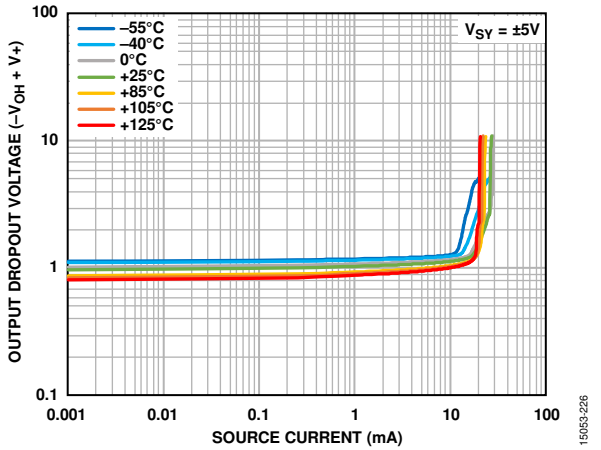

Figure 18. Output Dropout Voltage vs. Source Current, V_{SY} = ±5 V

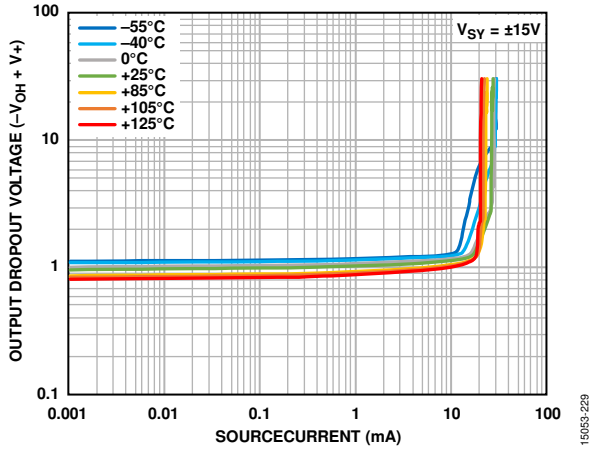

Figure 21. Output Dropout Voltage vs. Source Current, V_{SY} = ±15 V

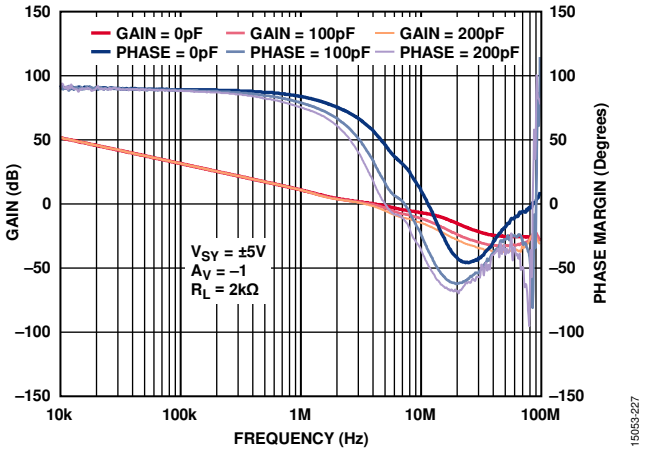

Figure 22. Open-Loop Gain and Phase Margin vs. Frequency, V_{SY} = ±5 V

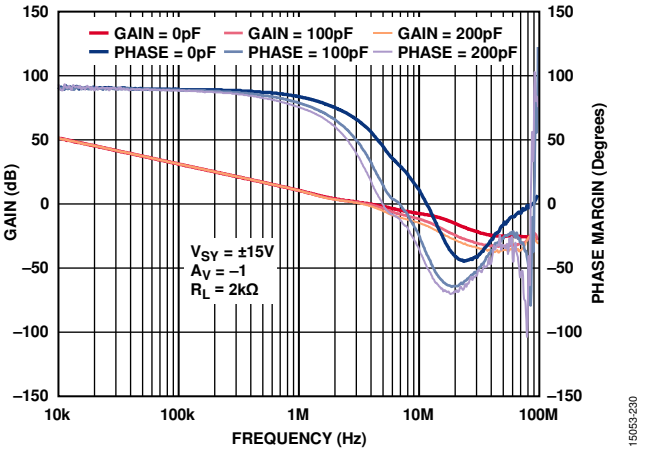

Figure 25. Open-Loop Gain and Phase Margin vs. Frequency, V_{SY} = ±15 V

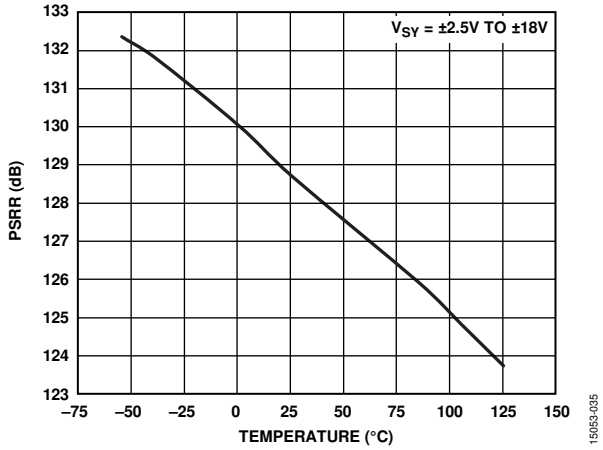

Figure 23. PSRR vs. Temperature, V_{SY} = ±2.5 V to ±18 V

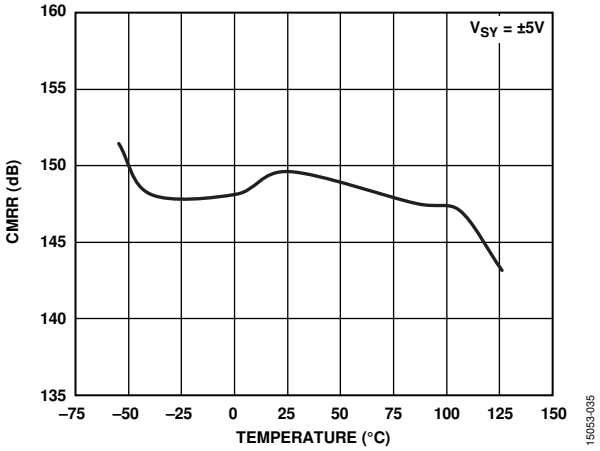

Figure 26. CMRR vs. Temperature, V_{SY} = ±5 V

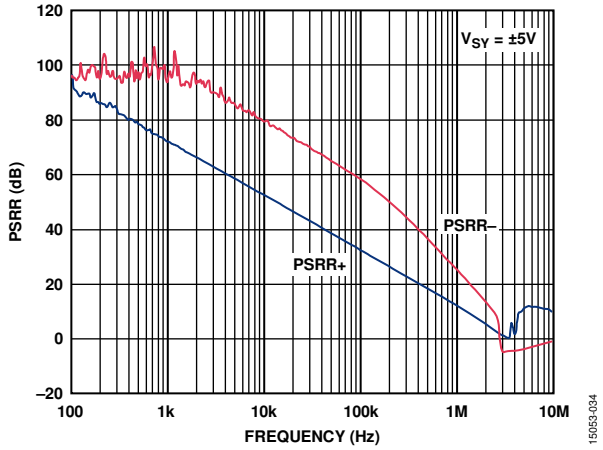

Figure 24. PSRR vs. Frequency, V_{SY} = ±5 V

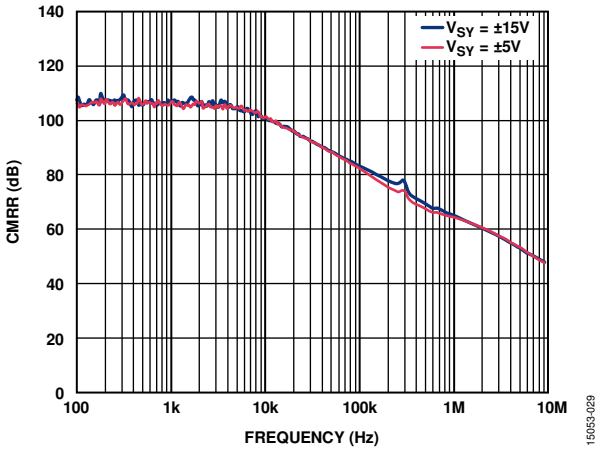

Figure 27. CMRR vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

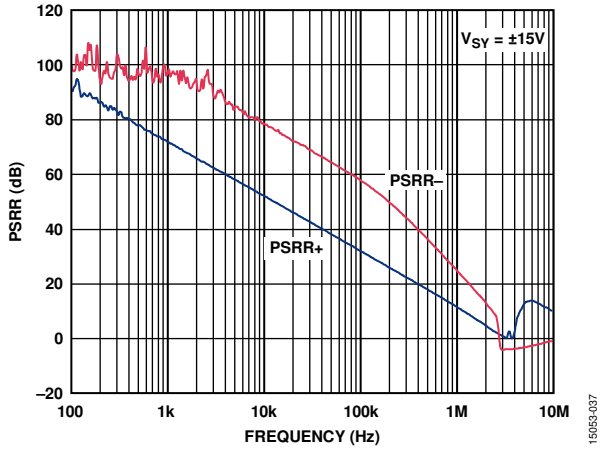

Figure 28. PSRR vs. Frequency, V_{SY} = ±15 V

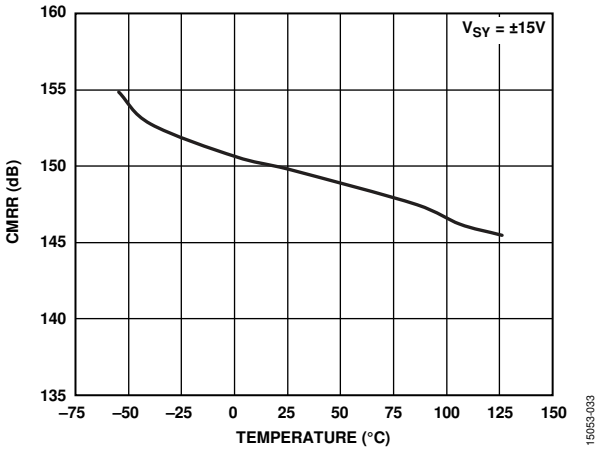

Figure 31. CMRR vs. Temperature, V_{SY} = ±15 V

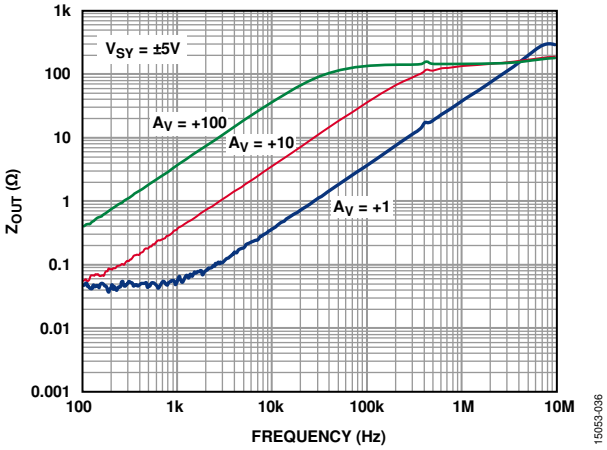

Figure 29. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

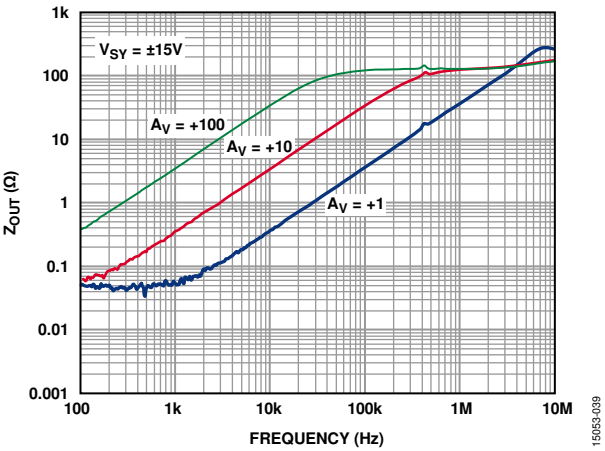

Figure 32. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

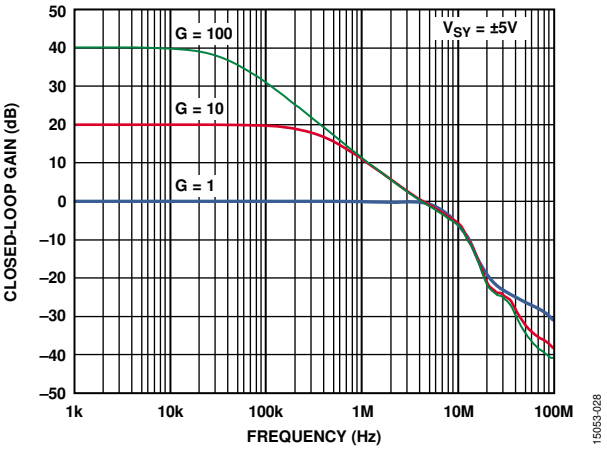

Figure 30. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

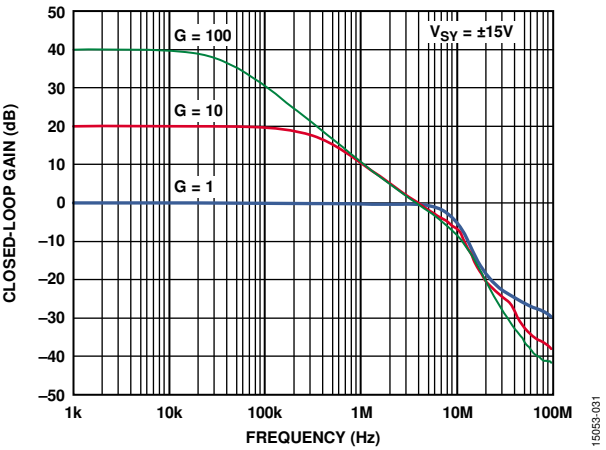

Figure 33. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

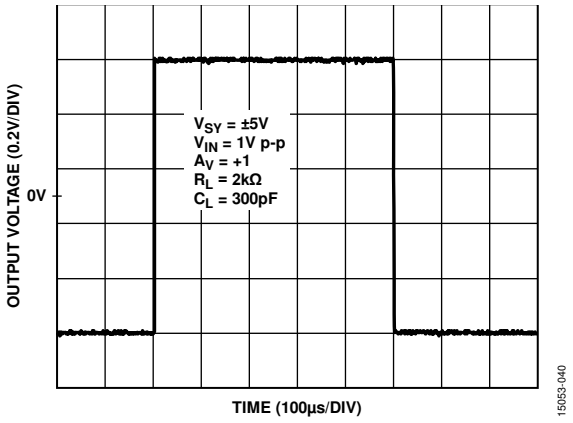

Figure 34. Large Signal Transient Response, V_{SY} = ±5 V

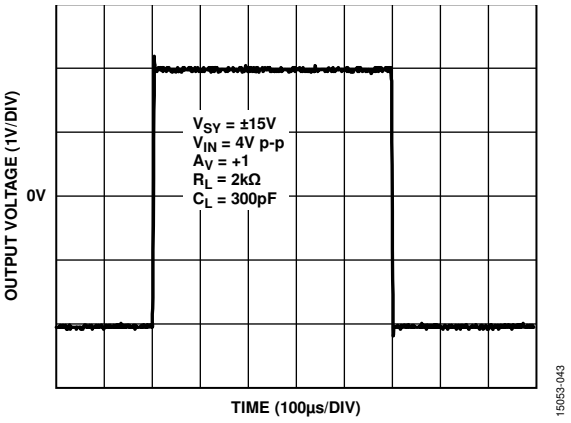

Figure 37. Large Signal Transient Response, V_{SY} = ±15 V

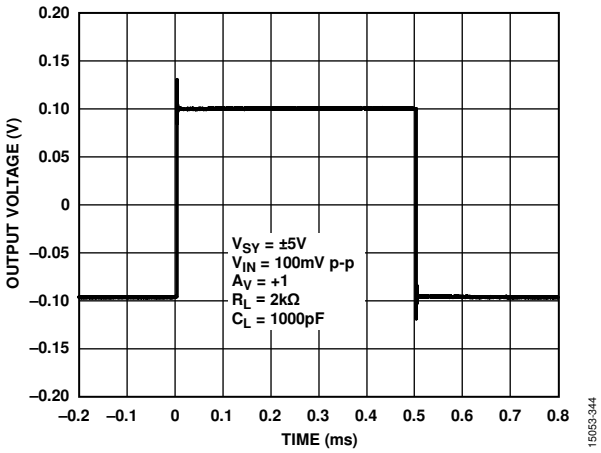

Figure 35. Small Signal Transient Response, V_{SY} = ±5 V

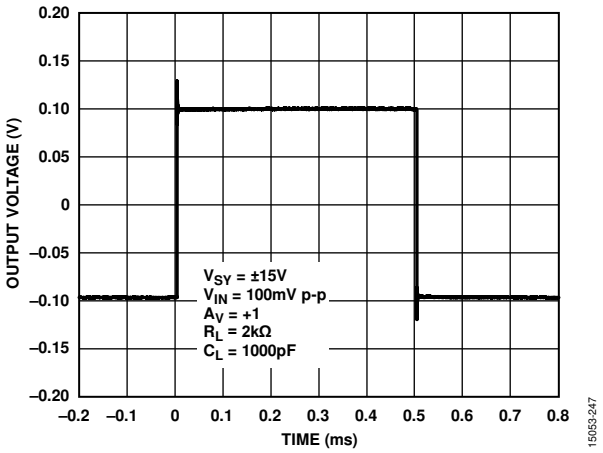

Figure 38. Small Signal Transient Response, V_{SY} = ±15 V

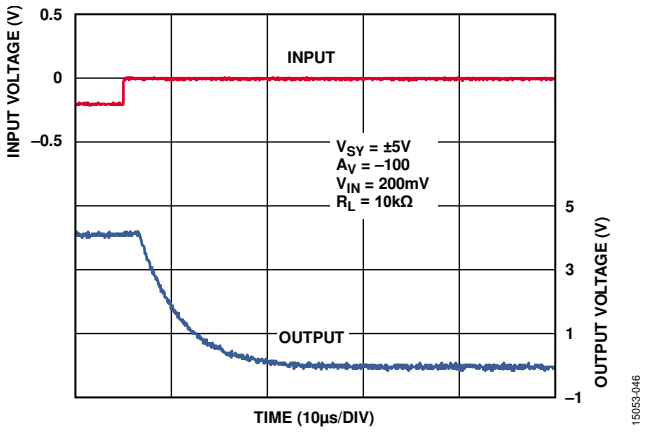

Figure 36. Positive Overload Recovery, V_{SY} = ±5 V

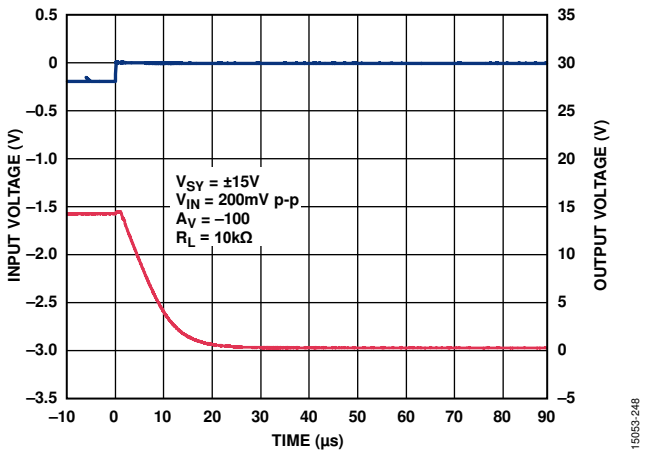

Figure 39. Positive Overload Recovery, V_{SY} = ±15 V

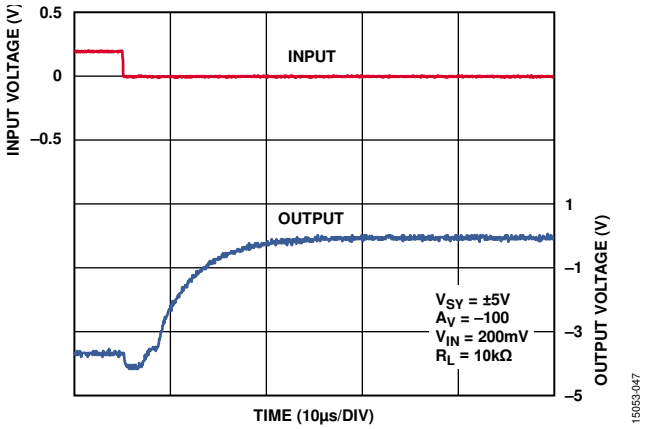

Figure 40. Negative Overload Recovery, V_{SY} = ±5 V

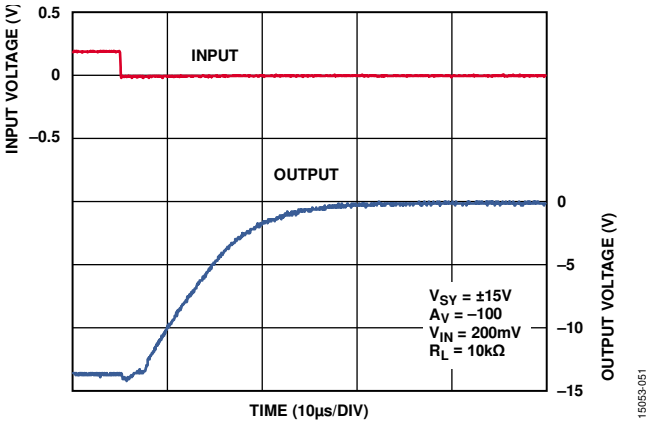

Figure 43. Negative Overload Recovery, V_{SY} = ±15 V

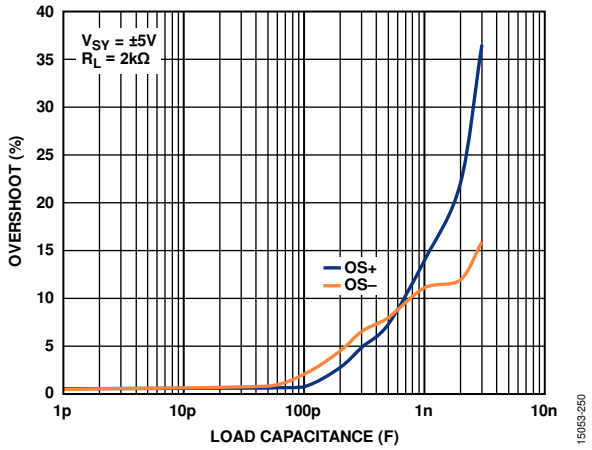

Figure 41. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V

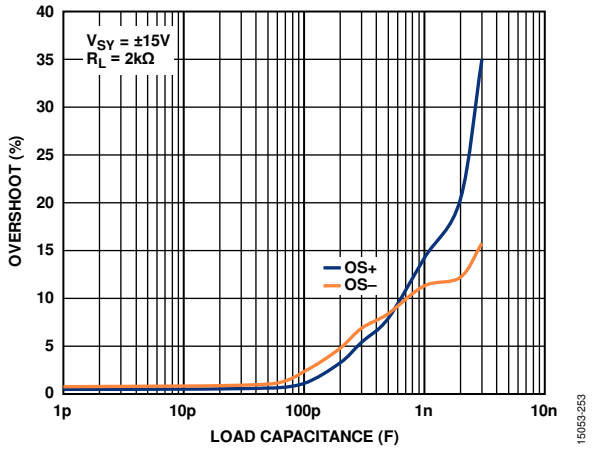

Figure 44. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±15 V

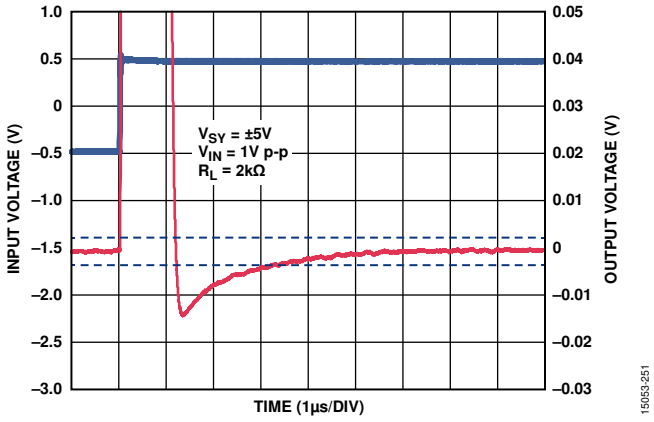

Figure 42. Positive 0.1% Settling Time, V_{SY} = ±5 V

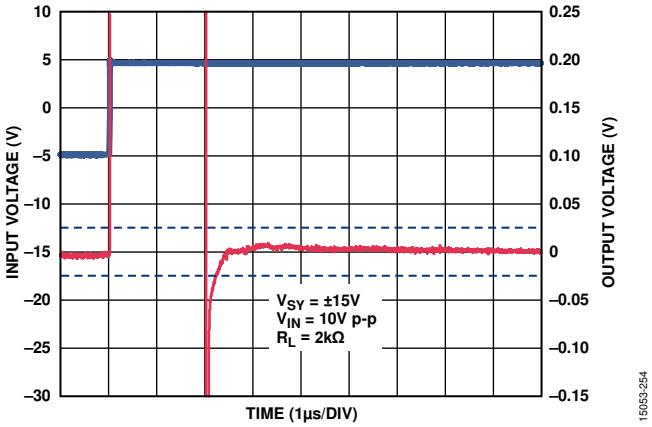

Figure 45. Positive 0.1% Settling Time, V_{SY} = ±15 V

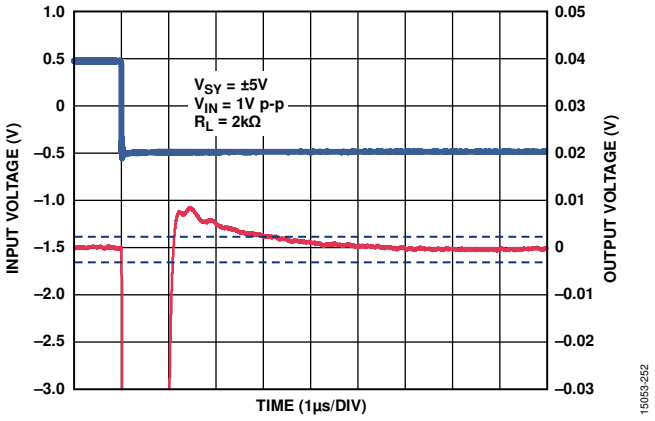

Figure 46. Negative 0.1% Settling Time, V_{SY} = ±5 V

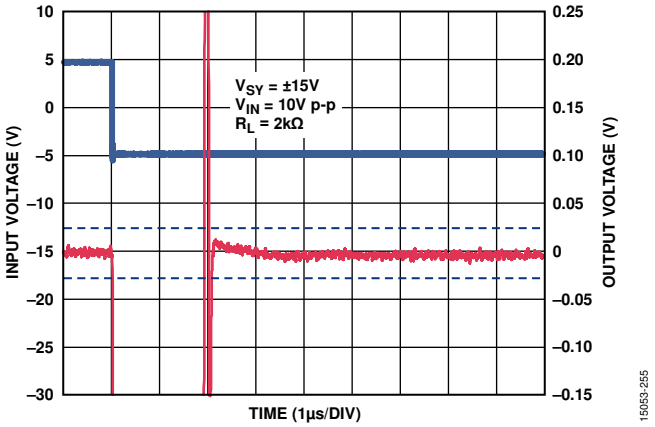

Figure 49. Negative 0.1% Settling Time, V_{SY} = ±15 V

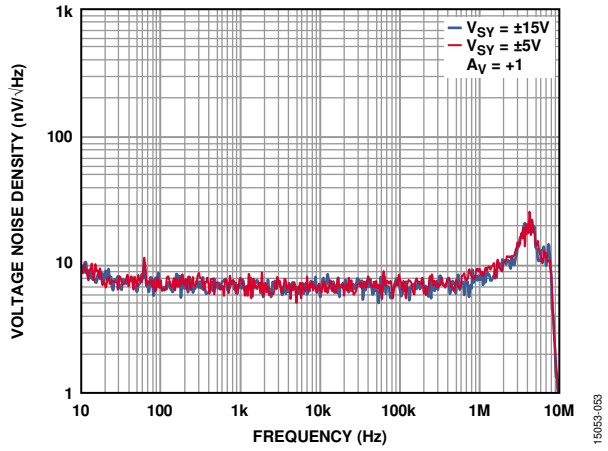

Figure 47. Voltage Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

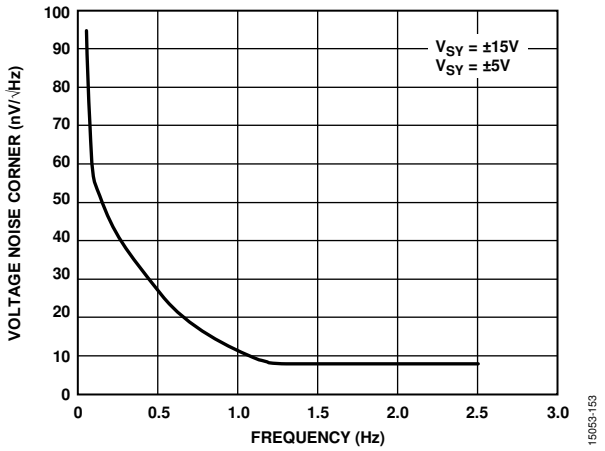

Figure 50. Voltage Noise Corner vs. Frequency, V_{SY} = ±15 V and V_{SY} = ±5 V

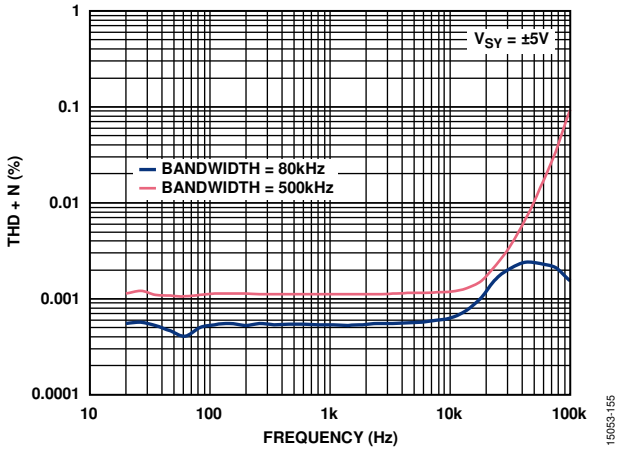

Figure 48. THD + N vs. Frequency, V_{SY} = ±5 V

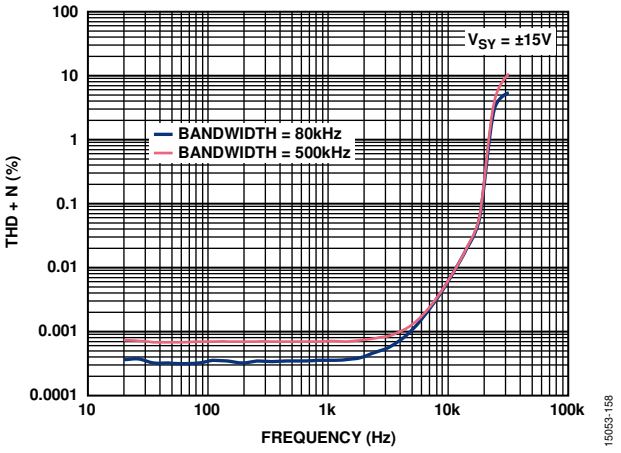

Figure 51. THD + N vs. Frequency, V_{SY} = ±15 V

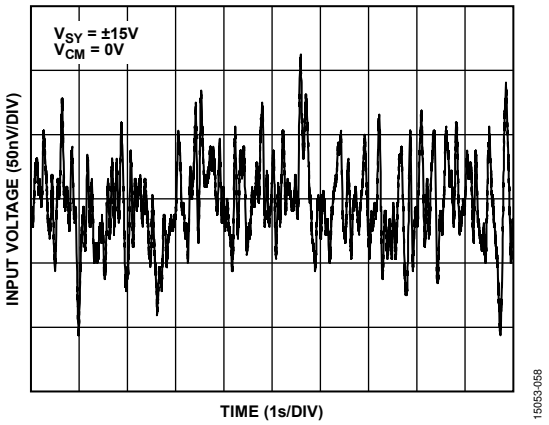

Figure 52. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V

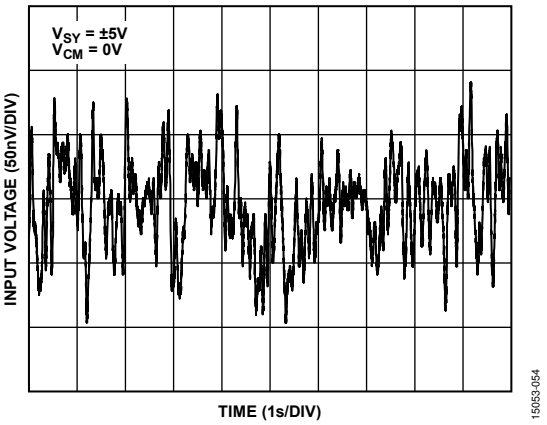

Figure 55. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

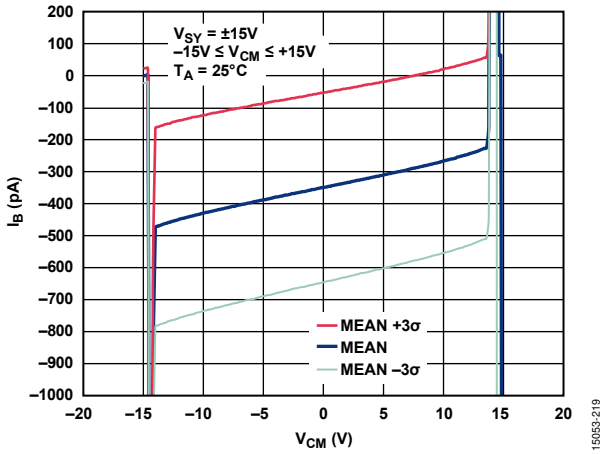

Figure 53. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM})

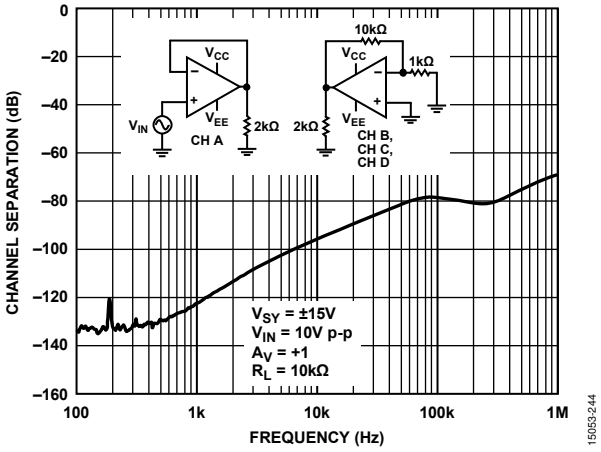

Figure 56. Channel Separation, V_{SY} = ±15 V

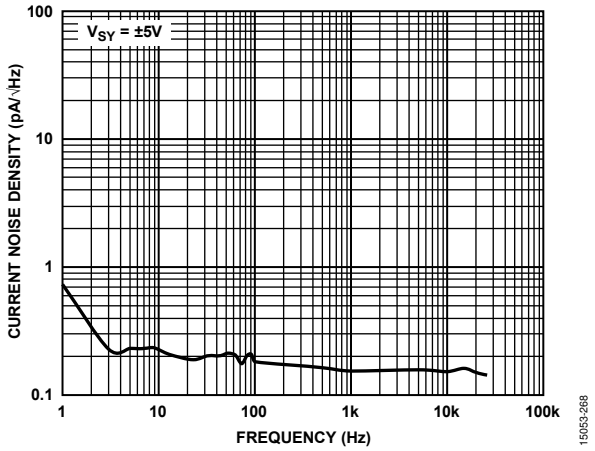

Figure 54. Current Noise Density vs. Frequency, V_{SY} = ±5 V

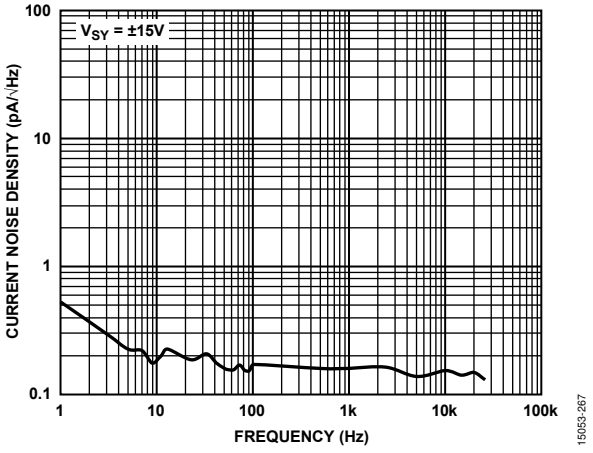

Figure 57. Current Noise Density vs. Frequency, V_{SY} = ±15 V

OUTLINE DIMENSIONS

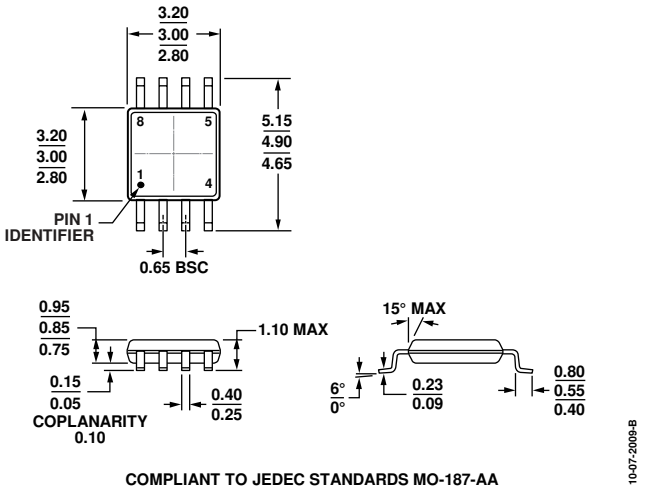

Figure 58. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4077-2TRMZ-EP	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y6Q
ADA4077-2TRMZ-EPR7	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y6Q

[1] Z = RoHS Compliant Part.

D15053-0-12/16(0)