

1-Mbit (64K x 16) Static RAM

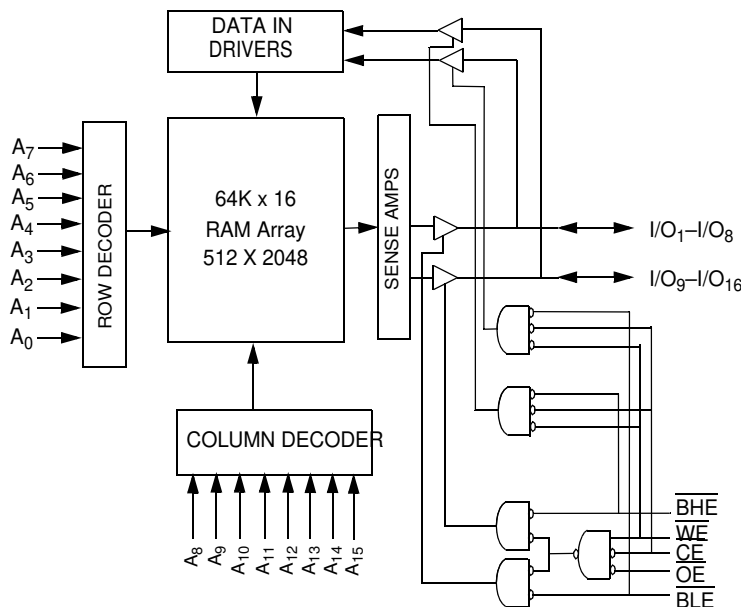
Features

- **Temperature Ranges**
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive-A: -40°C to 85°C
 - Automotive-E: -40°C to 125°C
- **High speed**
 - $t_{AA} = 10$ ns (Commercial)
 - $t_{AA} = 15$ ns (Automotive)
- **CMOS for optimum speed/power**
- **Low active power**
 - 825 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in Pb free and non Pb free 44-pin TSOP II and 44-pin 400-mil-wide SOJ**

Functional Description^[1]

The CY7C1021BN/CY7C10211BN is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₁ to I/O₈. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₉ to I/O₁₆. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₁ through I/O₁₆) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1021BN/CY7C10211BN is available in standard 44-pin TSOP Type II and 44-pin 400-mil-wide SOJ packages. Customers should use part number CY7C10211BN when ordering parts with 10 ns t_{AA} , and CY7C1021BN when ordering 12 ns and 15 ns t_{AA} .

Pin Configurations

SOJ / TSOP II Top View

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	\overline{OE}
A ₀	5	40	\overline{BHE}
\overline{CE}	6	39	\overline{BLE}
I/O ₁	7	38	I/O ₁₆
I/O ₂	8	37	I/O ₁₅
I/O ₃	9	36	I/O ₁₄
I/O ₄	10	35	I/O ₁₃
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₅	13	32	I/O ₁₂
I/O ₆	14	31	I/O ₁₁
I/O ₇	15	30	I/O ₁₀
I/O ₈	16	29	I/O ₉
\overline{WE}	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Selection Guide

		7C10211B-10	7C1021B-12	7C1021B-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Com'l / Ind'l	150	140	130
	Automotive-A			130
	Automotive-E			130
Maximum CMOS Standby Current (mA)	Com'l / Ind'l	10	10	10
	Com'l / Ind'l (L version)	0.5	0.5	0.5
	Automotive-A (L version)			0.5
	Automotive-E			15

Pin Definitions

Pin Name	SOJ, TSOP–Pin Number	I/O Type	Description
A ₀ –A ₁₅	1–5, 18–21, 24–27, 42–44	Input	Address Inputs used to select one of the address locations.
I/O ₁ –I/O ₁₆	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	No Connects. Not connected to the die.
\overline{WE}	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
\overline{CE}	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
\overline{BHE} , \overline{BLE}	40, 39	Input/Control	Byte Write Select Inputs, active LOW. \overline{BHE} controls I/O ₁₆ –I/O ₉ , \overline{BLE} controls I/O ₈ –I/O ₁ , .
\overline{OE}	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage on V _{CC} Relative to GND ^[2]	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to V _{CC} +0.5V
DC Input Voltage ^[2]	-0.5V to V _{CC} +0.5V
Current into Outputs (LOW)	20 mA

Static Discharge Voltage..... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature (T _A) ^[3]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	2.2	6.0	V	
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	Com'l / Ind'l	-1	+1	-1	+1	-1	+1	μA
			Automotive-A					-1	+1	μA
			Automotive-E					-4	+4	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	Com'l / Ind'l	-1	+1	-1	+1	-1	+1	μA
			Automotive-A					-1	+1	μA
			Automotive-E					-4	+4	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l / Ind'l		150		140		130	mA
			Automotive-A						130	
			Automotive-E						130	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l / Ind'l		40		40		40	mA
			Automotive-A						40	
			Automotive-E						50	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l / Ind'l		10		10		10	mA
			Com'l / Ind'l (L)		0.5		0.5		0.5	
			Automotive-A (L)						0.5	
			Automotive-E						15	

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		8	pF

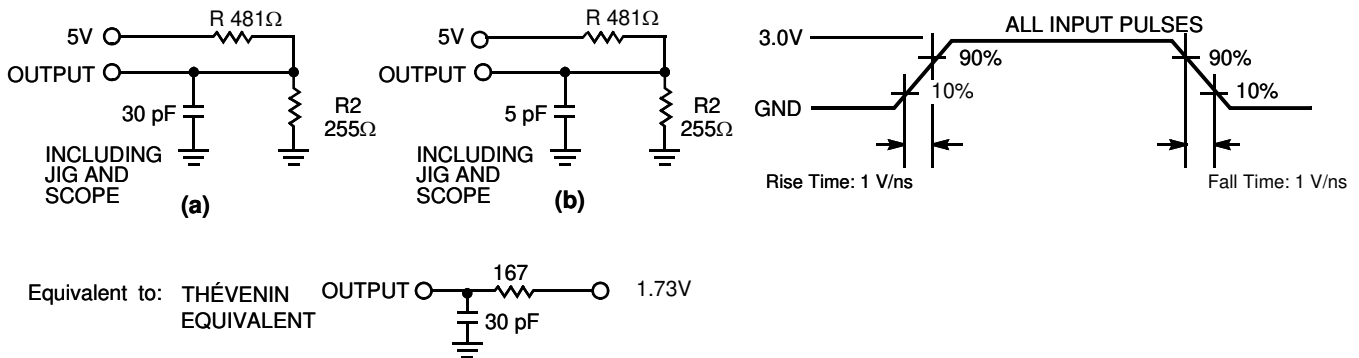
Notes:

- V_{IL} (min.) = -2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance^[4]

Parameter	Description	Test Conditions	44-pin SOJ	44-pin TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	64.32	76.89	$^{\circ}\text{C}/\text{W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		31.03	14.28	$^{\circ}\text{C}/\text{W}$

AC Test Loads and Waveforms



Switching Characteristics^[5] Over the Operating Range

Parameter	Description	7C10211B-10		7C1021B-12		7C1021B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		ns
t_{HZBE}	Byte Disable to High Z		5		6		7	ns

Notes:

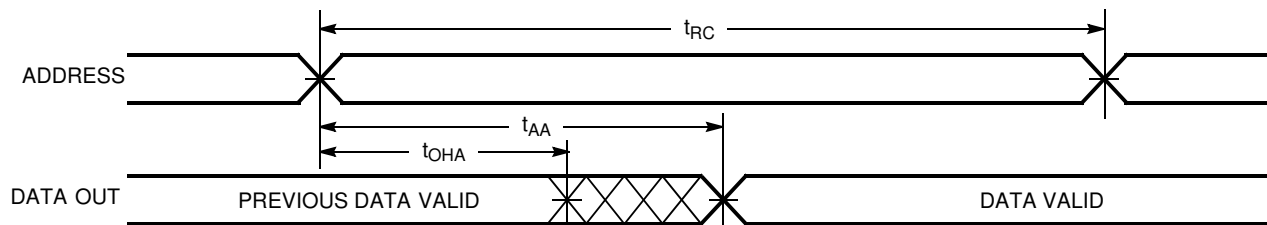
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

Switching Characteristics^[5] Over the Operating Range (continued)

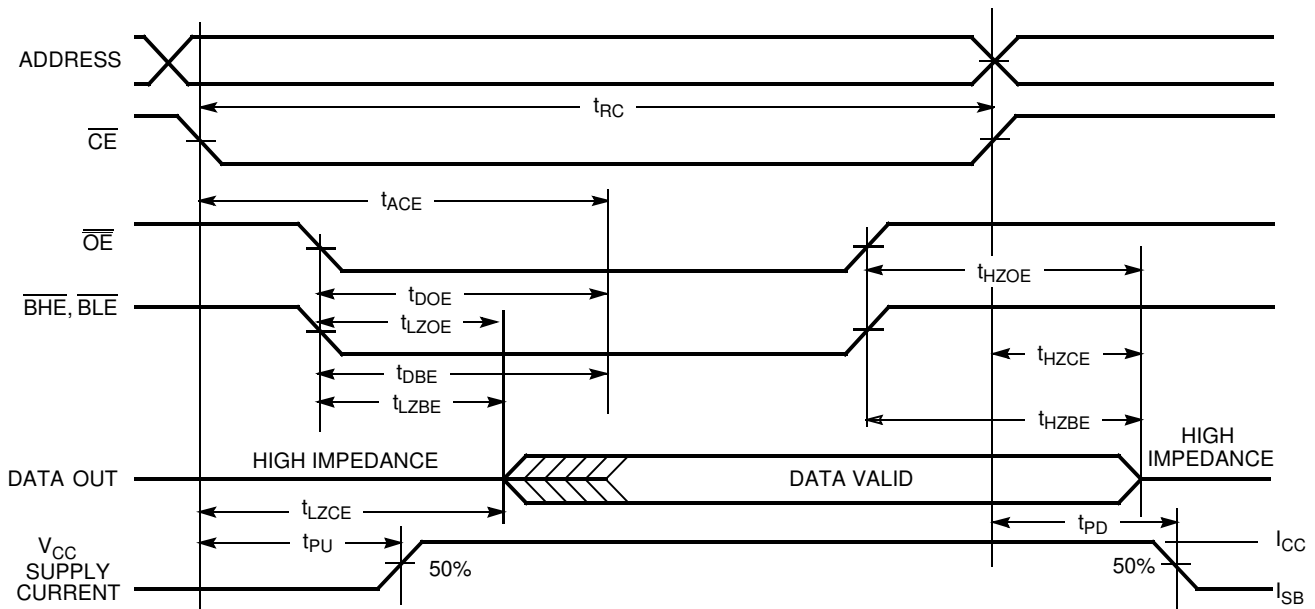
Parameter	Description	7C10211B-10		7C1021B-12		7C1021B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle^[8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	8		9		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		5		6		7	ns
t_{BW}	Byte Enable to End of Write	7		8		9		ns

Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]

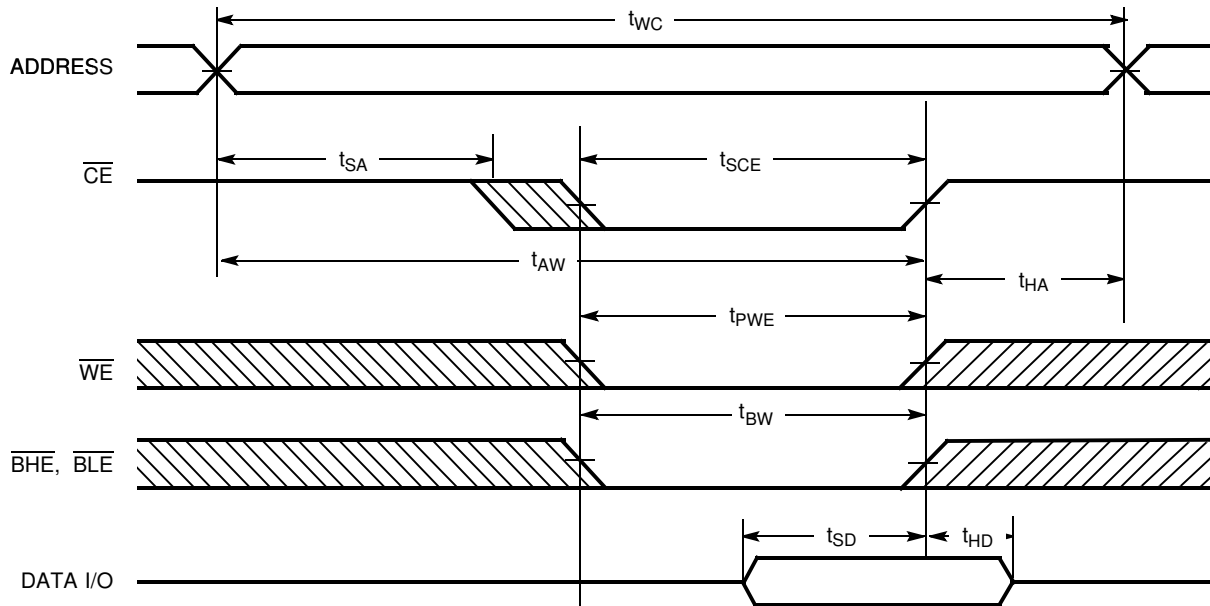


Notes:

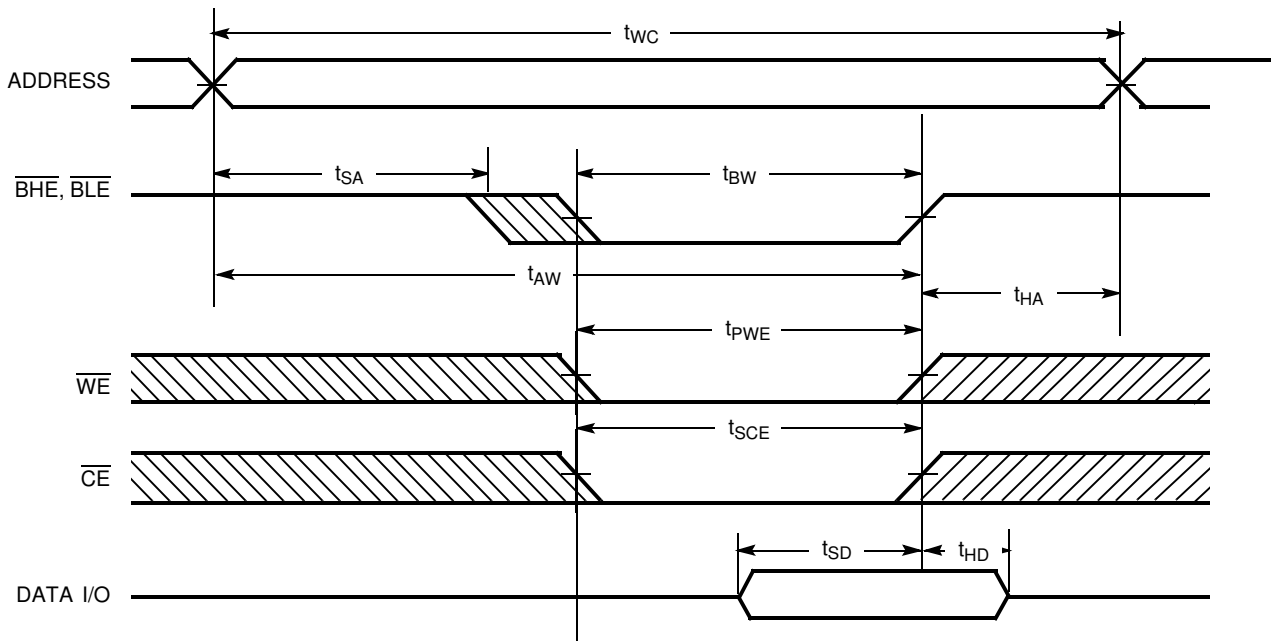
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE} / \overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE} / \overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
10. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12, 13]



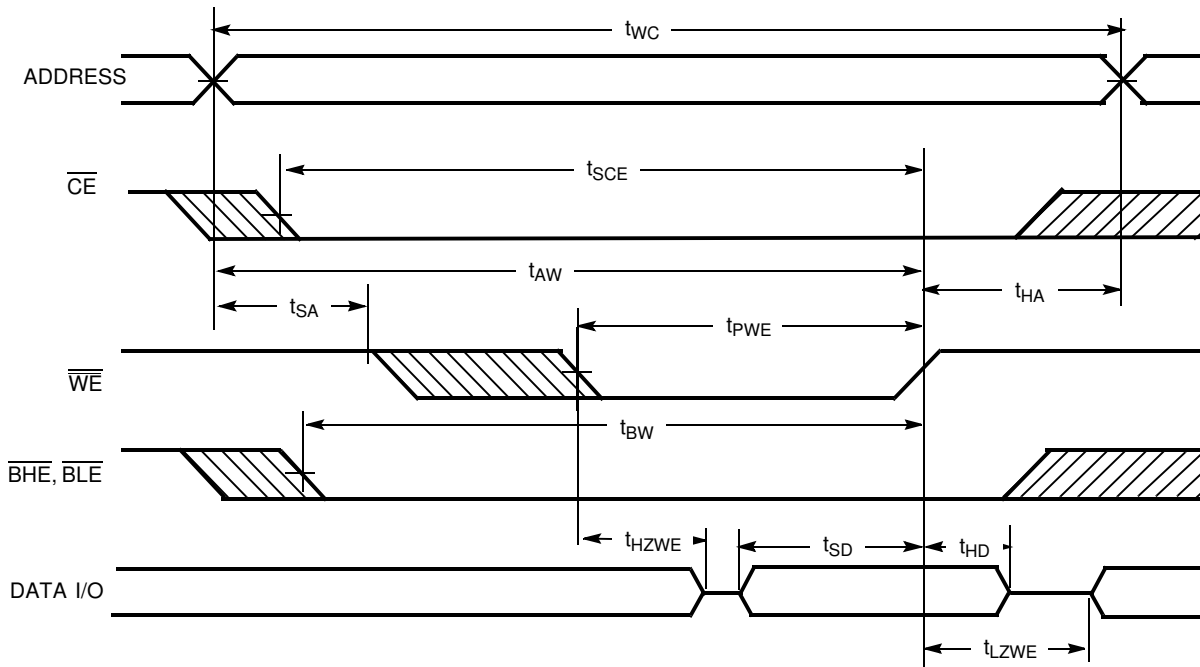
Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes:

11. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
12. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

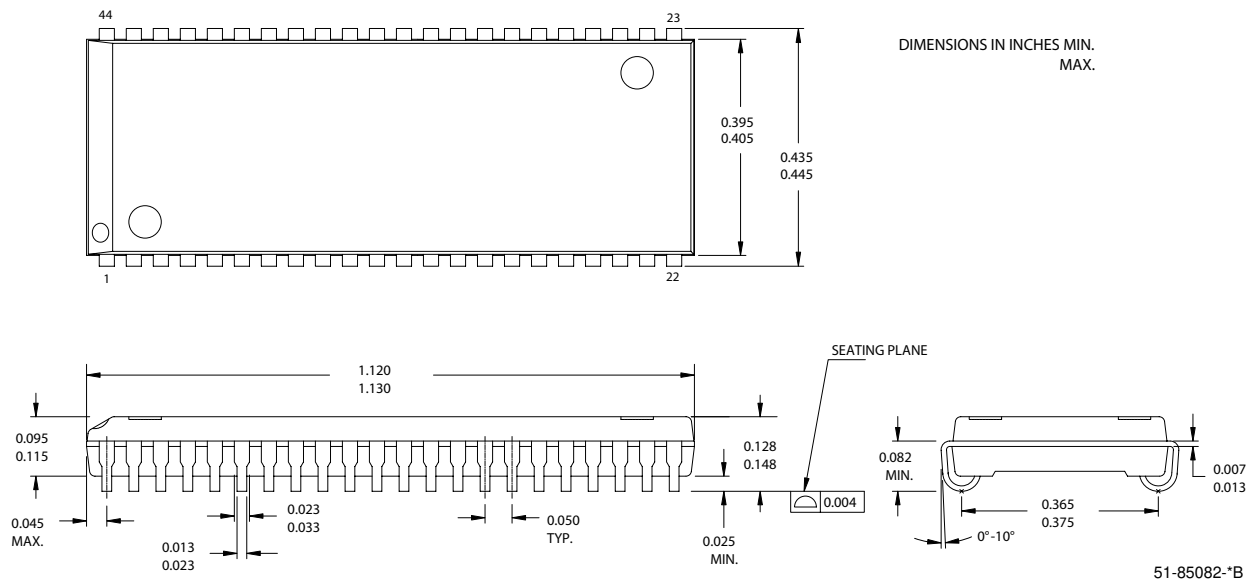
\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₁ -I/O ₈	I/O ₉ -I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I _{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I _{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I _{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I _{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C10211BN-10ZXC	51-85087	44-pin TSOP Type II	Commercial
12	CY7C1021BN-12VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021BN-12VXC		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021BN-12ZC	51-85087	44-pin TSOP Type II	
	CY7C1021BN-12ZXC		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BN-12VI	51-85082	44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021BN-12VXI		44-pin (400-Mil) Molded SOJ (Pb-Free)	
15	CY7C1021BN-15VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021BN-15VXC		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021BNL-15VXC		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021BN-15ZC	51-85087	44-pin TSOP Type II	
	CY7C1021BN-15ZXC		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BNL-15ZC		44-pin TSOP Type II	
	CY7C1021BNL-15ZXC		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BN-15VI	51-85082	44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021BN-15VXI		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021BN-15ZI	51-85087	44-pin TSOP Type II	
	CY7C1021BNL-15ZI		44-pin TSOP Type II	
	CY7C1021BN-15ZXI		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BNL-15ZXI		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BNL-15ZSXA	51-85087	44-pin TSOP Type II (Pb-Free)	Automotive-A
	CY7C1021BN-15VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-Free)	Automotive-E
	CY7C1021BN-15ZSXE	51-85087	44-pin TSOP Type II (Pb-Free)	

Package Diagrams

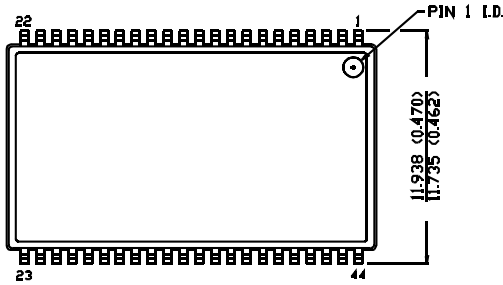
44-pin (400-Mil) Molded SOJ (51-85082)



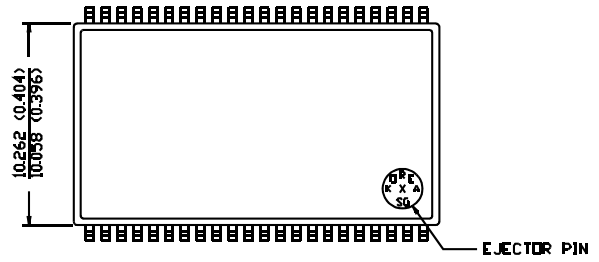
Package Diagrams (continued)

44-Pin TSOP II (51-85087)

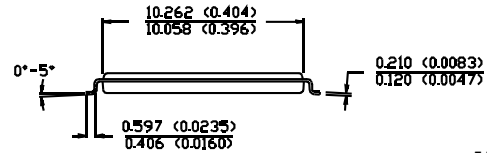
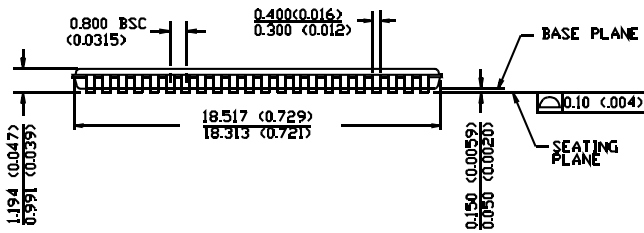
DIMENSION IN MM (INCH)
MAX
MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY7C1021BN/CY7C10211BN (64K x 16) Static RAM				
Document Number: 001-06494				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New Data Sheet
*A	505726	See ECN	NXR	Removed I _{OS} parameter from DC Electrical Characteristics table. Added Automotive products Updated ordering Information table