



F²MC-8FX Family

LQFP-100P (0.5 mm pitch) Header Board MB2146-250 Operation Manual

Doc. # 002-07371 Rev. *A

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intl): +1.408.943.2600
www.cypress.com

Copyrights

© Cypress Semiconductor Corporation, 2006-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Contents



1. Product Outline	5
2. Checking the Delivered Product	7
3. Handling Precautions	8
4. Notes on Designing	9
5. Procedure for Connecting to the User System	12
6. Mounting Mass Production MCUs	15
7. Product specification	17
8. Additional Informations	23
Revision History	24

Preface



Thank you for purchasing the LQFP-100P (0.5 mm pitch) *¹ header board (Model number : MB2146-250) for the F²MC -8FX family.

MB2146-250 is a header board used to connect the MCU board (Model number : MB2146-301, MB2146-303) which mounted F²MC-8FX family evaluation MCU to a user system.

This manual explains the handling of the MB2146-250 for the F²MC-8FX family. Before using MB2146-250, be sure to read this manual.

Consult the Sales representatives or the Support representatives of Cypress for mass-produced MCUs and evaluation MCUs which correspond on MB2146-250.

*1 : The lead pitch of package (FPT-100P-M05) is 0.5 mm and the body size is 14 mm × 14 mm.

■ Caution of the products described in this document

The following precautions apply to the product described in this manual.



The wrong use of a device will give an injury and may cause malfunction on customers system.

Cuts	This product has parts with sharp points that are exposed. Do not touch edge of the product with your bare hands.
Damage	When connect the header board to the user system, correctly position the index mark (▲) on the NQPACK mounted on the user system with the 1 pin direction(1) on the header board, otherwise the MCU board and user system might be damaged.
Damage	When mounting a mass production MCU, correctly position pin 1, otherwise the mass production MCU and user system might be damaged.

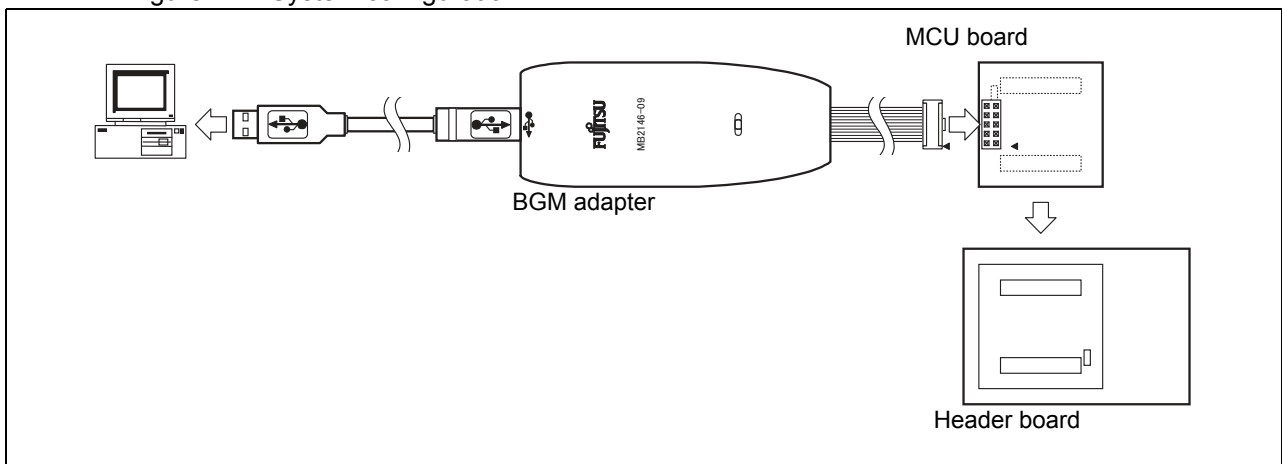
1. Product Outline



■ Product outline

This product is a header board (referred to as header board) used to connect the MCU board (Model number : MB2146-301, MB2146-303) which mounted an evaluation MCU in the F²MC-8FX family of Fujitsu 8-bit microcontrollers to a user system. To build an F²MC-8FX evaluation environment, combine three products as shown in Figure 1-1: the header board, MCU board, and BGM adapter (Model number : MB2146-09).

Figure 1-1. System configuration



■ Product configuration

Table 1-1 lists the product configuration in the header board, and Table 1-2 lists options.

Table 1-1. Product configuration

Name	Description	Remarks
F ² MC-8FX LQFP-100P (0.5 mm pitch) header board [Model number : MB2146-250]	Connector/LQFP100pin (0.5 mm pitch) Package conversion	-
[Model number : YQPACK100SD] (Tokyo Eletech Corporation)	I/F between header board and NQPACK	Accessory (Finishing connection)
[Model number : NQPACK100SD] (Tokyo Eletech Corporation)	User system mounting	Accessory
[Model number : HQPACK100SD] (Tokyo Eletech Corporation)	It is used at the time of mass-production MCU mounting to NQPACK.	Accessory

Figure 1-2. Option

Name	Description	Remarks
BGM adapter [Model number : MB2146-09]	ICE unit for F ² MC-8FX	-
MCU board [Model number : MB2146-301, MB2146-303]	Built-in MB95FV100B-101, MB95FV100B-103	Built-in F ² MC-8FX evaluation MCU *

* : Several types of evaluation MCUs are available depending on their applications. Purchase the one that satisfies the service conditions.

2. Checking the Delivered Product



Before using the MB2146-250, confirm that the following components are included in the box:

- LQFP-100P (0.5 mm pitch) Header board *¹: 1
- Screws for securing Header board (M2 × 10 mm, 0.4 mm pitch) : 4
- NQPACK100SD *²: 1
- HQPACK100SD *³: 1
- Operation manual (English version, this manual) : 1

¹Referred to as "header board". Header board is mounted on YQPACK100SD (Tokyo Eletech Corporation) , referred to as "YQPACK".
²IC socket manufactured by Tokyo Eletech Corporation, referred to as "NQPACK", and supplied with a special screwdriver and 2 guide pins. A socket offering higher reliability, NQPACK100SD-SL (Tokyo Eletech Corporation, sold separately) , can be used by making an IC socket mounting hole on the user system board. For more information, contact Tokyo Eletech Corporation.
³IC socket cover manufactured by Tokyo Eletech Corporation, referred to as "HQPACK", with 4 screws for securing HQPACK (M2 × 6 mm, 0.4 mm pitch) .

3. Handling Precautions



The header board is precision-manufactured to improve dimensional accuracy and to ensure reliable contact. The header is therefore sensitive to mechanical shock. To ensure correct use of the header in the proper environment, observe the following points regarding its insertion and removal:

- To avoid placing stress on the NQPACK mounted on the user system board during connecting the header board.

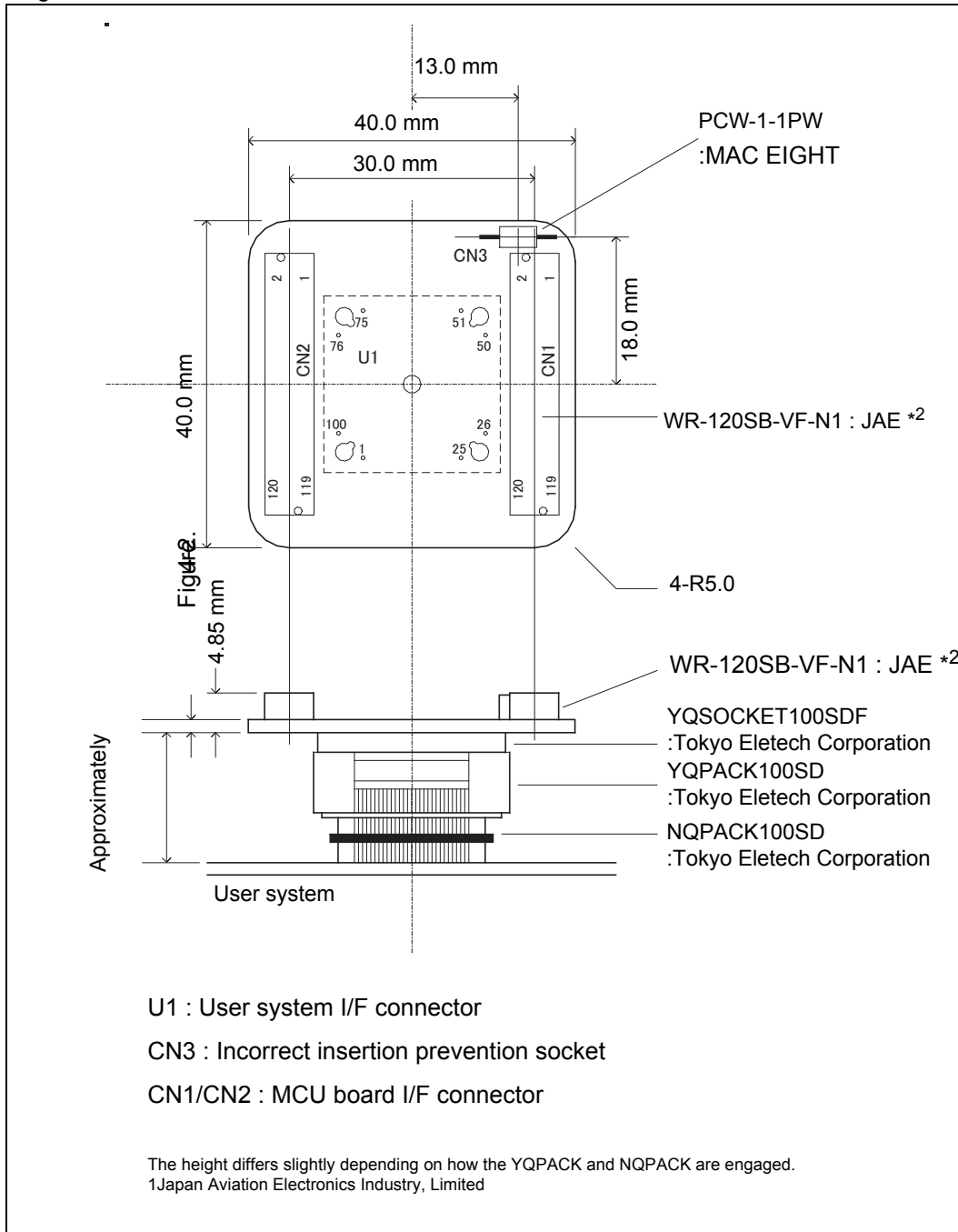
4. Notes on Designing



■ Notes on designing PC board for the user system

When the header board is connected to the user system, the parts mounted around the NQPACK in the user system may be touched the header board if the height of the parts is tall. To prevent this, design the printed circuit board for the user system such that the components do not exceed the height shown in Figure 4-1. Figure 4-1 shows dimension of the header board.

Figure 4-1. Header board dimensions



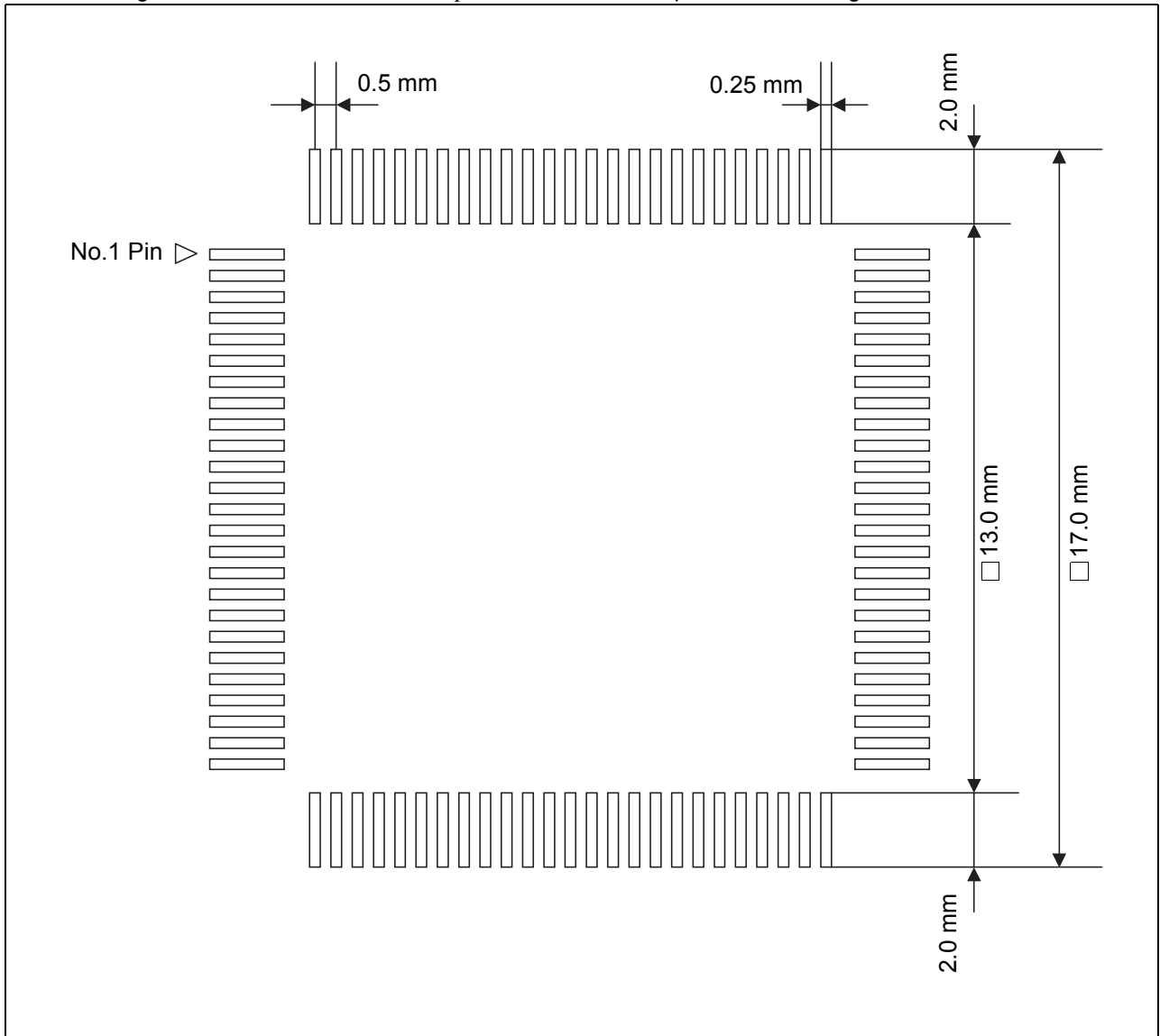
■ **MCU footprint design notes**

Figure 4-3 shows the recommended footprint dimensions of the NQPACK mounted on the printed circuit board for the user system.

Take the footprint in Figure 4-3 into consideration as well as the footprint of the mass production MCU when designing the printed circuit board for the user system.

To follow updated information, be sure to contact Tokyo Eletech Corporation whenever designing the PC board.

Figure 4-3. Recommended footprint dimensions footprint for mounting the NQPACK



5. Procedure for Connecting to the User System

System

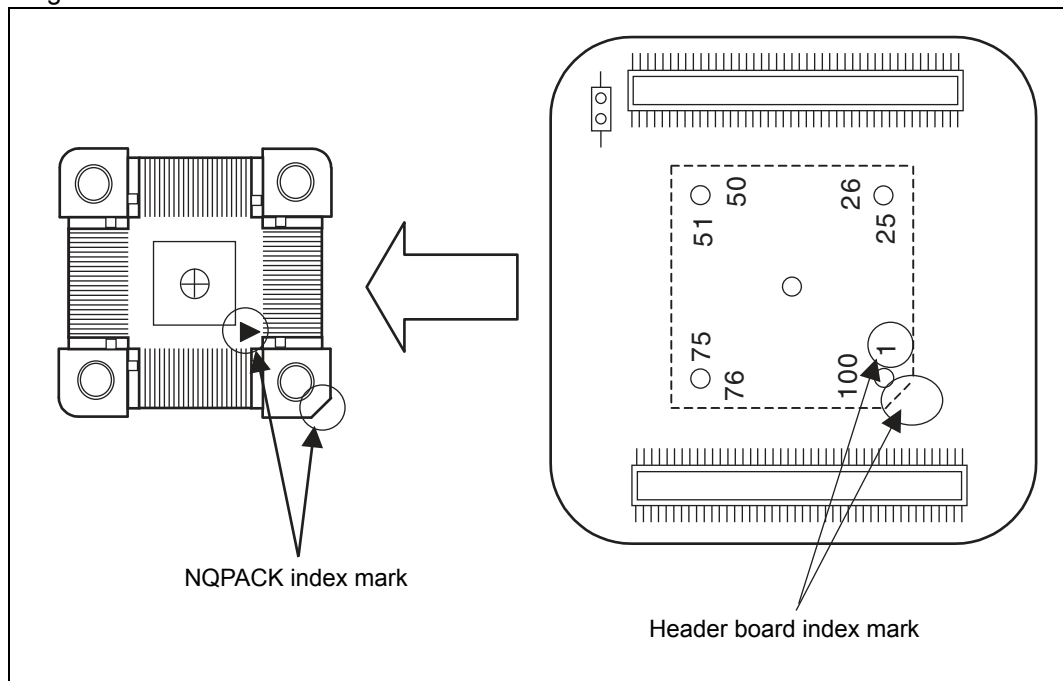


■ Connecting

Please mount the supplied NQPACK on the user system before using the LQFP-100P (0.5 mm pitch) header board.

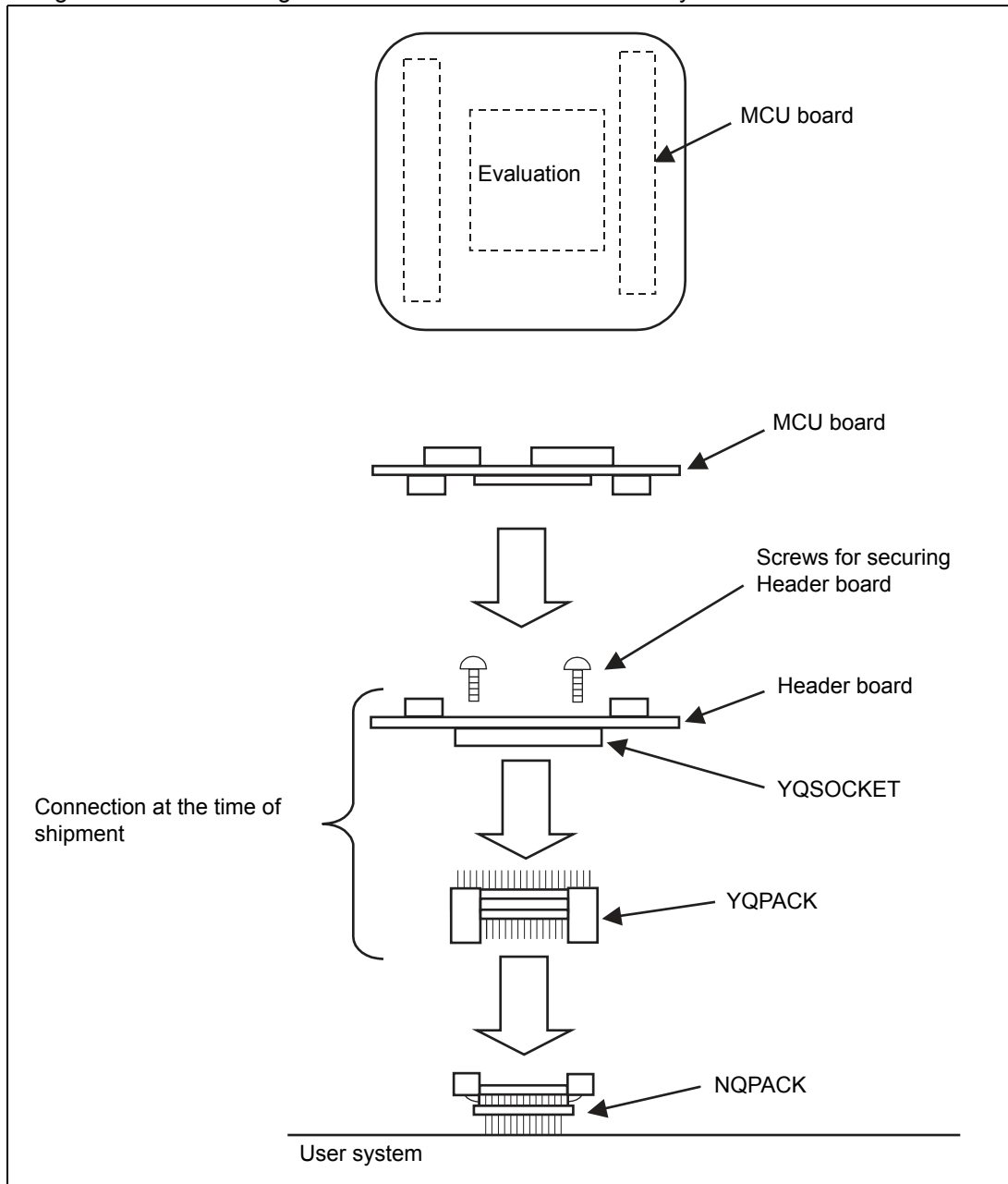
1. To connect the header board to the user system, match pin 1 indicated by the index mark (▲) on the NQPACK mounted on the user system with pin 1 indicated by the index mark (angle cut linearly at one place only in silk screen) on the header board and then insert it (See Figure 5-1) . The pin of YQPACK is thin and easy to bend. Insert NQPACK after confirm that the pin of YQPACK is not bent.

Figure 5-1. Index Position



- 2 Insert each screw for securing header board in each of the four drilled holes on the header board, and then tighten the screws diagonally. The center screw hole is not used. To tighten the screws, use the special screwdriver supplied with the NQPACK to finally tighten the four screws in sequence. Tightening the screws too tight might result in a defective contact.
- 3 Connect the MCU board to the header board while being careful not to excessively force the NQPACK. The MCU board can be connected to the header board only in the correct orientation as they have an incorrect insertion header socket to prevent reverse connection. Figure 4-2 illustrates how the MCU board, header board, NQPACK, and user system are connected together.

Figure 5-2. Connecting MCU board/header board to user system



■ **Disconnection**

1. Remove the MCU board from the header board. Detach the four corners slowly in sequence not to excessively force the junction with the NQPACK.
2. Remove all of the four screws from the header board. Pull out the header board vertically from the NQPACK. Remove the header board slowly not to excessively force the junction with the NQPACK.

6. Mounting Mass Production MCUs

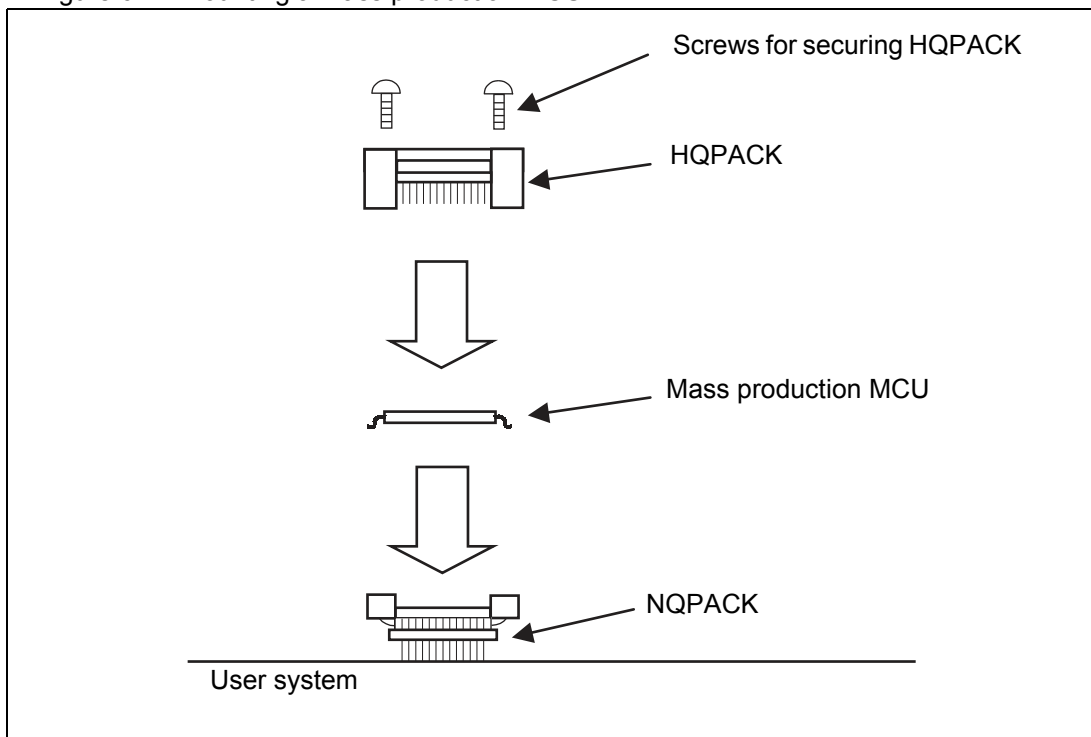


■ Mounting

To mount a mass production MCU on the user system, use the supplied HQPACK (IC socket cover) (See Figure 6-1) .

1. To mount a mass production MCU on the user system, match the index mark (▲) on the NQPACK mounted on the user system with the index mark (●) on the mass production MCU.
2. Confirm that the mass production MCU is correctly mounted on the NQPACK. Next, match the index mark of HQPACK with the index mark of NQPACK and insert it (angle cut linearly at one place only) .
The pin of HQPACK is thin and easy to bend. Insert NQPACK after confirm that the pin of HQPACK is not bent.
3. Insert each screw for securing HQPACK in each of four drilled holes on the HQPACK, and then tighten the screws diagonally.
To tighten the screws, use the special screwdriver supplied with the NQPACK to finally tighten the four screws in sequence. Tightening the screws too tight might result in a defective contact.

Figure 6-1. Mounting a mass production MCU



■ Disconnection

To remove the HQPACK, remove all of the four screws and pull out the HQPACK vertically from the NQPACK. When you take out the mass production MCU, the mass production MCU is handled by using a vacuum pick-up tool. Do not attempt to remove the mass production MCU forcibly, for example, using a screwdriver as doing so can bend the pins of the mass production MCU or break the NQPACK.

7. Product specification



■ General specification

Table 7-1 lists the general specifications of the header board.

Table 7-1. General specification

Item	Description
Operating temperature and storage temperature	5 °C to 35 °C (operation) , 0 °C to 40 °C (storage)
Operating humidity and storage humidity	20 % to 80 % (operation) , 20 % to 80 % (storage)
Dimensions	Approximately 40 mm × 40 mm × 16 mm (Height contains YQPACK and NQPACK)

■ Main part

The main part of a header board is shown in Table 7-2.

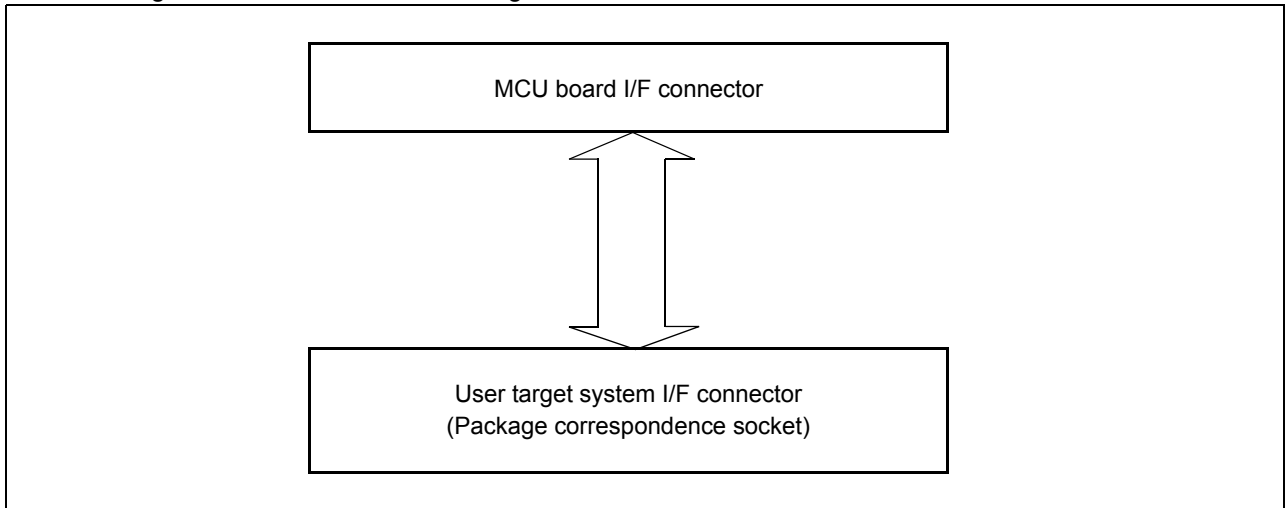
Table 7-2. Main part

Part	Description
MCU board I/F connector	120 pins, 0.5 mm pitch, 2-piece connector (straight) × 2 [Model number : WR-120SB-VF-N1 (Japan Aviation Electronics Industry, Limited)]
Incorrect insertion prevention socket	2 pins, 2.54 mm pitch, 1-piece socket (Straight) [Model number : PCW-3-1-1PW (MAC EIGHT)]
User target system I/F connector	Socket 100 pins, 0.5 mm pitch [Model number : YQSOCKET100SDF (Tokyo Eletech Corporation)]

■ Functional block diagram

A header board performs socket conversion between the MCU board I/F connector and YQPACK. The header board does not contain any ICs or other internal components. A Figure 7-1 shows the block diagram.

Figure 7-1. Functional block diagram



■ **MCU board I/F connector(CN1/CN2/CN3)**

CN1 and CN2 are MCU board I/F connectors. CN3 is the incorrect insertion prevention socket of a MCU board. The pin assignment of the MCU board I/F connector CN1 is shown in Table 7-3, and the pin assignment of the MCU board I/F connector CN2 is shown in Table 7-4.

Table 7-3. Pin assignment of the MCU board I/F connector CN1

Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name	Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name	Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name
1	A9	PC4	41	E2	LVR3	81	P3	BSOUT
2	B9	PC1	42	E1	LVSS	82	P4	BDBMX
3	C9	PC2	43	F4	LVDREXT	83	R1	P83
4	D9	PC3	44	F3	LVDBGR	84	R2	BRSTX
5	A8	PC0	45	F2	LVDENX	85	R3	X0A
6	B8	PB4	46	F1	P22A	86	R4	RSTX
7	C8	PB5	47	-	GND	87	T1	ROMS1
8	D8	PB6	48	-	GND	88	T2	BSIN
9	A7	PB7	49	G4	P20A	89	T3	Vss
10	B7	PB2	50	G3	NC1	90	T4	X0
11	C7	PB0	51	G2	P21A	91	U1	BEXCK
12	D7	PB1	52	G1	P23A	92	U2	X1
13	A6	PB3	53	H4	P24A	93	U3	MOD
14	B6	PA2	54	H3	P25A	94	U4	PF2
15	C6	P95	55	H2	P26A	95	V1	X1A
16	D6	PA0	56	H1	P27A	96	V2	Vcc53
17	A5	PA3	57	J4	P24B	97	-	GND
18	B5	P94	58	J3	P50	98	-	GND
19	C5	P90	59	J2	P23B	99	V3	PINT0
20	D5	P91	60	J1	P51	100	V4	PSEL_EXT
21	A4	PA1	61	K1	P52	101	R5	PF1
22	A3	P93	62	K2	P55	102	T5	PF0
23	-	GND	63	K3	P54	103	U5	NC2
24	-	GND	64	K4	P53	104	V5	PENABLE
25	A2	CSVENX	65	L1	P70	105	R6	APBENX
26	A1	Vss	66	L2	P74	106	T6	PINT1
27	B4	P92	67	L3	P73	107	U6	PCLK
28	B3	TCLK	68	L4	P72	108	V6	PADDR0
29	B2	LVCC	69	M1	P71	109	R7	PACTIVE
30	B1	LVDIN	70	M2	P76	110	T7	PLOCK
31	C4	Cpin	71	M3	P80	111	U7	PWRITE
32	C3	Vcc51	72	M4	P77	112	V7	PADDR1
33	C2	LVDENX2	73	-	GND	113	R8	PADDR2
34	C1	LVR4	74	-	GND	114	T8	PADDR3
35	D4	TESTO	75	N1	P75	115	U8	PADDR4
36	D3	LVDOUT	76	N2	P82	116	V8	PADDR5
37	D2	LVR2	77	N3	PG0	117	R9	PADDR7
38	D1	BGOENX	78	N4	P84	118	T9	PRDATA0
39	E4	LVR1	79	P1	P81	119	U9	PADDR6
40	E3	LVR0	80	P2	ROMS0	120	V9	PRDATA1

Table 7-4. Pin assignment of the MCU board I/F connector CN2

Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name	Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name	Connector Pin Numbers	Evaluation MCU Pin Numbers	Signal name
1	A10	PC5	41	E17	NC4	81	P16	P34
2	B10	PD0	42	E18	SEL0	82	P15	P35
3	C10	PC6	43	F15	SEL3	83	R18	P44
4	D10	PC7	44	F16	SEL4	84	R17	P36
5	A11	PD1	45	F17	SEL1	85	R16	P31
6	B11	PD2	46	F18	P04C	86	R15	AVcc3
7	C11	PD3	47	–	GND	87	T18	P40
8	D11	PD4	48	–	GND	88	T17	P32
9	A12	PD5	49	G15	P06C	89	T16	AVss
10	B12	PD7	50	G16	P07C	90	T15	AVR
11	C12	P61	51	G17	P05C	91	U18	P33
12	D12	P60	52	G18	P00C	92	U17	P30
13	A13	PD6	53	H15	P01C	93	U16	AVR3
14	B13	P64	54	H16	P02C	94	U15	P15
15	C13	P66	55	H17	P03C	95	V18	AVcc
16	D13	P65	56	H18	P07A	96	V17	DA0
17	A14	P62	57	J15	P04A	97	–	GND
18	B14	PE0A	58	J16	P05A	98	–	GND
19	C14	PE3A	59	J17	P06A	99	V16	P14
20	D14	PE2A	60	J18	P03A	100	V15	P10
21	A15	P63	61	K18	P02A	101	R14	P16
22	A16	P67	62	K17	P07B	102	T14	DA1
23	–	GND	63	K16	P01A	103	U14	P13
24	–	GND	64	K15	P00A	104	V14	PWDATA7
25	A17	PE4A	65	L18	P06B	105	R13	P11
26	A18	Vcc54	66	L17	P05B	106	T13	P12
27	B15	PE1A	67	L16	P04B	107	U13	NC3
28	B16	PE5A	68	L15	P03B	108	V13	PWDATA3
29	B17	PE7A	69	M18	P02B	109	R12	PWDATA5
30	B18	PE3B	70	M17	P00B	110	T12	PWDATA6
31	C15	PE6A	71	M16	P46	111	U12	PWDATA4
32	C16	Vss	72	M15	P47	112	V12	PRDATA7
33	C17	PE2B	73	–	GND	113	R11	PWDATA0
34	C18	PE7B	74	–	GND	114	T11	PWDATA1
35	D15	PE1B	75	N18	P01B	115	U11	PWDATA2
36	D16	PE0B	76	N17	P43	116	V11	PRDATA6
37	D17	PE6B	77	N16	P41	117	R10	PRDATA3
38	D18	SEL2	78	N15	P42	118	T10	PRDATA4
39	E15	PE5B	79	P18	P45	119	U10	PRDATA5
40	E16	PE4B	80	P17	P37	120	V10	PRDATA2

■ User system I/F YQPACK (U1)

The pin assignment of user system I/F YQPACK in a header board is shown in Table 7-5.

Table 7-5. Pin assignment of the user system I/F YQPACK in header board

Connector Pin Numbers	Signal name	Connector Pin Numbers	Signal name	Connector Pin Numbers	Signal name
1	V _{SS}	35	P40/AN08	69	PD3/S19
2	PG0 (C pin)	36	P41/AN09	70	PD2/S18
3	P00/INT00/HC00	37	P42/AN10	71	PD1/S17
4	P01/INT01/HC01	38	P43/AN11	72	PD0/S16
5	P02/INT02/HC02	39	P53/TRG1	73	PC7/S15
6	P03/INT03/HC03	40	P70/TO0	74	PC6/S14
7	P04/INT04/HC04	41	P71/TI0	75	PC5/S13
8	P05/INT05/HC05	42	P67/S39/SIN	76	V _{CC}
9	P06/INT06/HC06	43	P66/S38/SOT	77	PC4/S12
10	P07/INT07/HC07	44	P65/S37/SCK	78	PC3/S11
11	P10/UI0	45	P64/S36/EC1	79	PC2/S10
12	P11/UO0	46	P63/S35/TO11	80	PC1/S09
13	P12/UCK0	47	P62/S34/TO10	81	PC0/S08
14	P13/TARG0/ADTG	48	RSTX/FTST	82	PB7/S07
15	P14/PPG0	49	X0A	83	PB6/S06
16	P20/PPG00	50	X1A	84	PB5/S05
17	P21/TO00	51	V _{SS}	85	PB4/S04
18	P22/TO00	52	X1	86	PB3/S03
19	P23/TO01	53	X0	87	PB2/S02
20	P24/EC0	54	MOD	88	PB1/S01
21	P50/SCL0	55	P61/S33/PPG11	89	PB0/S00
22	P51/SDA0	56	P60/S32/PPG10	90	PA3/COM3
23	P52/PPG1	57	PE7/S31/INT13	91	PA2/COM2
24	AVR	58	PE6/S30/INT12	92	PA1/COM1
25	A _{VCC}	59	PE5/S29/INT11	93	PA0/COM0
26	A _{VSS}	60	PE4/S28/INT10	94	P95/C1
27	P30/AN00	61	PE3/S27	95	P94/C0
28	P31/AN01	62	PE2/S26	96	P93/V0
29	P32/AN02	63	PE1/S25	97	P92/V1
30	P33/AN03	64	PE0/S24	98	P91/V2
31	P34/AN04	65	PD7/S23	99	P90/V3
32	P35/AN05	66	PD6/S22	100	V _{CC}
33	P36/AN06	67	PD5/S21		
34	P37/AN07	68	PD4/S20		

8. Additional Informations



For more informations please visit our websites:

<http://www.cypress.com/documentation/development-kitsboards/mb2146-301a-e>

<http://www.cypress.com/documentation/development-kitsboards/mb2146-09a-e>

Please contact your local support team for any technical question.

Revision History



Document Revision History

Document Title: F ² MC-8FX Family LQFP-100P (0.5 mm pitch) Header Board MB2146-250 Operation Manual				
Document Number: 002-07371				
Revision	ECN#	Issue Date	Origin of Change	Description of Change
**	—	02/20/2006	HUAL	Initial release
*A	5282940	05/24/2016	HUAL	Migrated to Cypress format