

FQB27N25TM F085/FQI27N25TU F085

May 2014

### **N-Channel MOSFET**

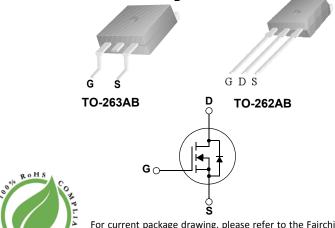
250 V, 25.5 A, 131 mΩ

#### **Features**

- Typ  $R_{DS(on)}$  = 108m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 25.5A
- Typ  $Q_{q(tot)}$  = 45nC at  $V_{GS}$  = 10V,  $I_D$  = 27A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

### **Applications**

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging

#### MOSFET Maximum Ratings T<sub>.1</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage		250	V
V <sub>GS</sub>	Gate to Source Voltage		±30	V
	Drain Current - Continuous (V <sub>GS</sub> =10) (Note 1)	T <sub>C</sub> = 25°C	25.5	^
I <sub>D</sub>	Pulsed Drain Current	T <sub>C</sub> = 25°C	See Figure 4	Α
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 2)	972	mJ
Г	Power Dissipation		417	W
$P_D$	Derate above 25°C		3.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to + 150	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.3	°C/W
R <sub>0.IA</sub>	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	43	°C/W

### **Package Marking and Ordering Information**

Device Marking	Device Package Reel Size Tape		Tape Width	Quantity	
FQB27N25TM	FQB27N25TM_F085	TO-263AB	330mm	24mm	800 units
FQI27N25TU	FQI27N25TU_F085	TO-262AB	Tube	N/A	50 units

- 1: Current is limited by bondwire configuration.
- Starting T<sub>J</sub> = 25°C, L = 4.67mH, I<sub>AS</sub> = 20.4A, V<sub>DD</sub> = 100V during inductor charging and V<sub>DD</sub> = 0V during time in avalanche.
   R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

Units

Max.

Тур.

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted.

**Parameter** 

Off Characteristics							
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250μA, \	/ <sub>GS</sub> = 0V	250	-	-	V
I <sub>DSS</sub> Drain to Source Leakage Current	Dunin to Course I college Courset	V <sub>DS</sub> =250V,	$T_{J} = 25^{\circ}C$	-	-	1	μΑ
	$V_{GS} = 0V$	$T_J = 150^{\circ} C(Note 4)$	-	-	250	uA	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 30V$		-	-	±100	nA

**Test Conditions** 

Min.

### On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		3.0	4.1	5.0	V
R <sub>DS(op)</sub> Drain to Source On Resistance	I <sub>D</sub> = 25.5A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	108	131	mΩ	
R <sub>DS(on)</sub>	R <sub>DS(on)</sub> Drain to Source On Resistance	V <sub>GS</sub> = 10V	$T_J = 150^{\circ}C(Note 4)$	-	265	310	mΩ

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		-	1800	-	pF
C <sub>oss</sub>	Output Capacitance			-	350	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			-	45	-	pF
$R_g$	Gate Resistance	f = 1MHz		-	0.82	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	V <sub>DD</sub> = 125V	-	45	49	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2V$	I <sub>D</sub> = 27A	-	3.3	4	nC
$Q_{gs}$	Gate to Source Gate Charge		_	-	12	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	23	-	nC

## **Switching Characteristics**

t <sub>on</sub>	Turn-On Time	$V_{DD}$ = 125V, $I_{D}$ = 27A, $V_{GS}$ = 10V, $R_{GEN}$ = 25 $\Omega$	-	-	196	ns
t <sub>d(on)</sub>	Turn-On Delay		-	36	-	ns
t <sub>r</sub>	Rise Time		-	122	-	ns
t <sub>d(off)</sub>	Turn-Off Delay		-	81	-	ns
t <sub>f</sub>	Fall Time		-	60	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	164	ns

### **Drain-Source Diode Characteristics**

.,	0 , 5 ; 5; 1 , 7 ;	I <sub>SD</sub> = 25.5A, V <sub>GS</sub> = 0V	-	-	1.5	V
$V_{SD}$	Source to Drain Diode Voltage	I <sub>SD</sub> = 12.75A, V <sub>GS</sub> = 0V	-	-	1.25	V
t <sub>rr</sub>	ReverseRecovery Time	$I_F = 27A$ , $dI_{SD}/dt = 100A/\mu s$ ,	-	205	238	ns
Q <sub>rr</sub>	ReverseRecovery Charge	V <sub>DD</sub> =200V	-	1.8	2.3	nC

#### Notes

4: The maximum value is specified by design at  $T_J$  = 150°C. Product is not tested to this condition in production.

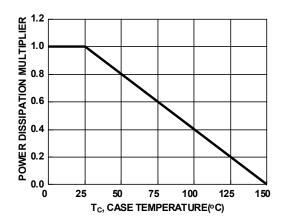
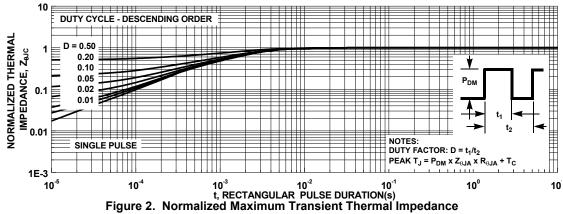


Figure 1. Normalized Power Dissipation vs. Case **Temperature** 



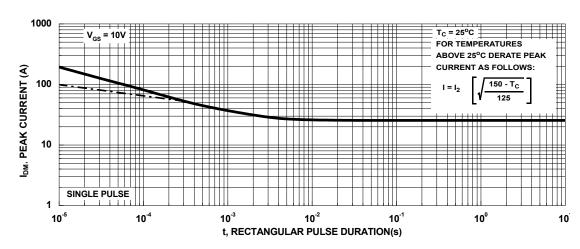


Figure 3. Peak Current Capability

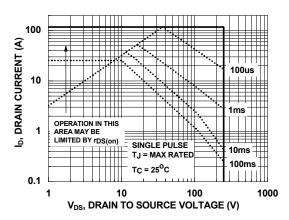
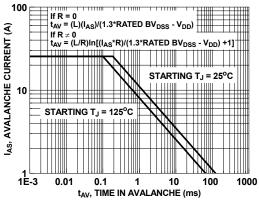


Figure 4. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching

Capability

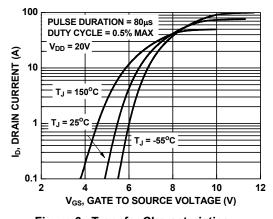


Figure 6. Transfer Characteristics

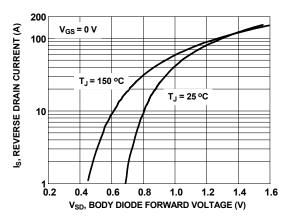


Figure 7. Forward Diode Characteristics

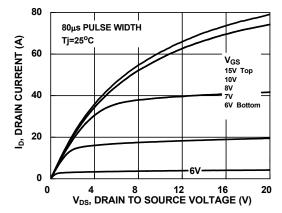


Figure 8. Saturation Characteristics

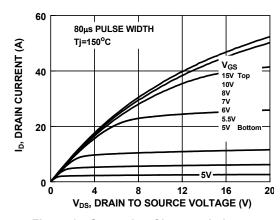


Figure 9. Saturation Characteristics

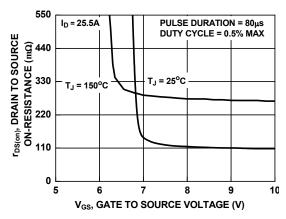


Figure 10. R<sub>DSON</sub> vs. Gate Voltage

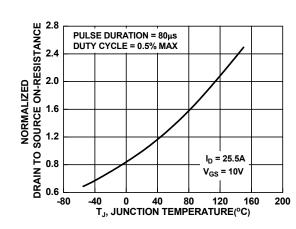


Figure 11. Normalized R<sub>DSON</sub> vs. Junction Temperature

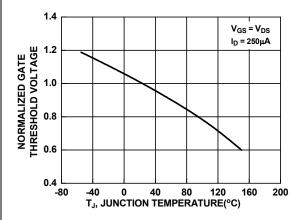


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

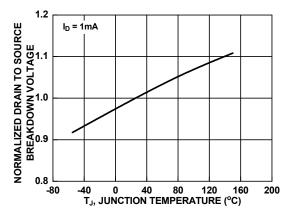


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

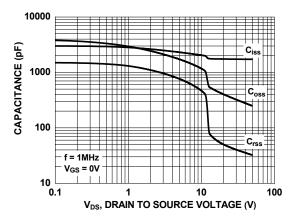


Figure 14. Capacitance vs. Drain to Source Voltage

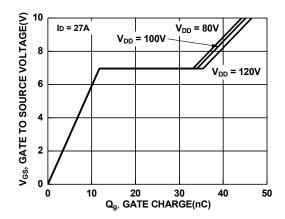


Figure 15. Gate Charge vs. Gate to Source Voltage





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