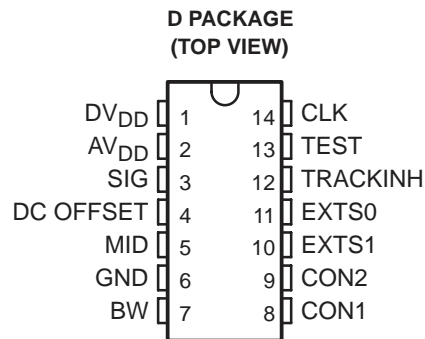- **Supports FLEX™ Protocol Pagers With The TLV5591 FLEX Decoder**
- **3-Pole Butterworth Low-Pass Selectable Dual-Bandwidth Audio Filter**
  - **BW 1 = 1 kHz ±5% (– 3 dB)**
  - **BW 2 = 2 kHz ±5% (– 3 dB)**
- **Both Peak and Valley Detectors Available**
- **2-Bit Analog-to-Digital Converter**
- **Operating Temperature Range . . . –25°C to 85°C**

- **Four Modes of Operation:**
  - **Fast Acquisition**
  - **Slow Acquisition**
  - **Hold Acquisition**
  - **Standby**
- **2.7-V to 3.3-V Single Power Supply Operation**

## applications

- **FLEX Protocol Numeric and Alphanumeric Pagers**
- **One-Way or Two-Way**

## description

The TLV5590 analog-to-digital converter is a system level solution to interface a 4-level baseband audio signal to a digital decoder. The TLV5590 is a direct interface to the TLV5591BVF† FLEX decoder. Designed primarily for pager applications, the TLV5590 incorporates signal conditioning, both peak and valley detection along with analog-to-digital conversion. A selectable third-order Butterworth filter with cutoff frequencies of 1 kHz and 2 kHz is included. The peak and valley detectors are implemented with a unique design that does not require external capacitors. Two 8-bit digital-to-analog converters (DACs) are used in a feedback loop to automatically adjust to the peak and valley levels. The DAC outputs are used to set $V_{ref+}$ and $V_{ref-}$ for the 2-bit analog-to-digital converter (ADC). Modes of operation include fast track, slow track, hold, and standby. The standby mode maximizes battery life. The TLV5590 operates on a single supply down to 2.7 V.

**D PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| DV$_{DD}$ | 1 | 14 | CLK |
| AV$_{DD}$ | 2 | 13 | TEST |
| SIG | 3 | 12 | TRACKINH |
| DC OFFSET | 4 | 11 | EXTS0 |
| MID | 5 | 10 | EXTS1 |
| GND | 6 | 9 | CON2 |
| BW | 7 | 8 | CON1 |

**AVAILABLE OPTIONS**

| T$_A$ | PACKAGE |
|---|---|
| | SMALL OUTLINE (D) |
| –25°C to 85°C | TLV5590ED |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FLEX is a trademark of Motorola, Incorporated.
† TLV5591BVF Data Manual Literature Number – SLWS048

**TEXAS INSTRUMENTS**

## functional block diagram

## Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $AV_{DD}$ | 2 | I | Analog supply voltage |
| BW | 7 | I | Digital bandwidth select. A high level on BW selects the 2-kHz filter cutoff and a low level selects the 1-kHz filter cutoff. |
| CON1 | 8 | I | Digital control 1 input. In conjunction with CON2, CON1 selects the fast acquisition mode, slow acquisition mode, hold or standby. |
| CON2 | 9 | I | Digital control 2 input. In conjunction with CON1, CON2 selects the fast acquisition mode, slow acquisition mode, hold or standby. |
| CLK | 14 | I | Digital clock input. CLK input is a 50% duty cycle TTL-level clock input with nominal frequency of 38.4 kHz. The CLK input is edge sensitive in all non-test modes. For all test modes, the CLK input is level sensitive. |
| DC OFFSET | 4 | I | Analog dc offset correction input. The dc component of the audio signal should be applied to DC OFFSET. |
| $DV_{DD}$ | 1 | I | Digital supply voltage |
| EXTS0 | 11 | O | Digital output 0 of the ADC. Data bit 0 is the LSB. |
| EXTS1 | 10 | O | Digital output 1 of the ADC. Data bit 1 is the MSB. |
| GND | 6 | | Return terminal for the IC current. |
| SIG | 3 | I | Analog audio signal input. An appropriate RC low-pass filter (antialiasing filter) should be connected to SIG. |
| MID | 5 | O | Analog midpoint output. MID is a buffered output of $AV_{DD}$/2. |
| TEST | 13 | I | Digital test input enable. TEST should be connected to ground in normal operation. |
| TRACKINH | 12 | I | Digital track inhibit logic input. A high level on TRACKINH disables the peak and valley detector counters, and a low level enables the peak and valley detector counters. The counters continue to decay at the decay rate while TRACKINH is a low level. |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $AV_{DD}$, $DV_{DD}$ | −0.5 V to 6.5 V |
| Input voltage range, $V_I$ | −0.3 V to $AV_{DD}$ + 0.3 V |
| Output voltage range, EXTS0, EXTS1 | −0.3 V to $DV_{DD}$ + 0.3 V |
| Offset input voltage, $V_{IO}$ | −0.3 V to $AV_{DD}$ + 0.3 V |
| Peak input current (any input) | ±20 mA |
| Operating free-air temperature range, $T_A$ | −25°C to 85°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $AV_{DD}$, $DV_{DD}$ | | 2.7 | | 3.3 | V |
| Power supply ripple | | | | 0.002 | $V_{pp}$ |
| Input clock frequency, $f_{(CLK)}$ | | | 38.4 | | kHz |
| Input clock duty cycle | | 45 | 50 | 55 | % |
| Voltage offset applied at DC OFFSET, $V_{I(DC\ OFFSET)}$ (see Notes 1 and 2) | | 0.25 | | $V_{DD}$−0.25 | V |
| Analog input voltage, $V_{I(pp)}$ (See Notes 1 and 2) | $V_{DD}$ = 3.1 V | 0.25 | | $V_{DD}$ − 0.25 | $V_{pp}$ |
| High-level control input voltage, $V_{IH}$ | $V_{DD}$ = 2.7 V to 3.3 V | | | 0.2 $DV_{DD}$ | V |
| Low-level control input voltage, $V_{IL}$ | $V_{DD}$ = 2.7 V to 3.3 V | 0.8 $DV_{DD}$ | | | V |
| Operating free-air temperature, $T_A$ | | −25 | | 85 | °C |

NOTES: 1. $V_{I(OFFSET)} = V_Q − V_{I(DC\ OFFSET)}$ where $V_Q$ is the dc quiescent voltage of the signal applied to the SIG terminal.

NOTES: 2.
$$V_{I(PEAK)} = \frac{\left(\dfrac{V_{DD}}{2} - 0.25\ V\right)}{4.217} - V_{I(OFFSET)} - 80\ mV$$

The pass-band filter gain represents the maximum specified voltage gain in volts/volt of the filter. The maximum gain for the filter is 4.217 V/V (12.5 dB). The input voltage range from this equation defines the maximum allowable input signal at the SIG terminal with a given voltage, $V_{I(DC\ OFFSET)}$, applied at the DC OFFSET terminal and a quiescent dc input voltage, $V_Q$, of the signal applied at the SIG terminal. When the input voltage is within this range, the peak and valley DACs do not over range. The 80 mV value is the tolerance on the voltage output at the MID terminal.

## electrical characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 2.7$ V to 3.3 V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

### power

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{DD}$ | Operating supply current | Fast track, slow track, or hold mode | | 250 | µA |
| $I_{DD(standby)}$ | Standby supply current | $V_{I(DC\ OFFSET)} = 0.8$ V, $V_{I(SIG)} = 0.8$ V, For all digital inputs, $0 < V_I < 0.5$ V or $V_I > DV_{DD} -0.5$ V | | 1 | µA |

### digital

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH} = -100$ µA | $DV_{DD} -0.5$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 100$ µA | | | 0.5 | V |
| $I_{IH}$ | High-level input current | $V_I = DV_{DD}$ | | 0.1 | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_I = 0$ | | −0.1 | −1 | µA |
| $C_i$ | Input capacitance, digital input | | | 10 | | pF |

### analog

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Voltage accuracy at MID | $V_{DD} = 3$ V, $C_{L(MID)} = 220$ nF | 1.42 | 1.5 | 1.58 | V |
| $Z_i$ | Input impedance at SIG (see Note 3) | $f_{(IN)} = 800$ Hz | | | 1 | MΩ |
| $Z_{i(offset)}$ | Input impedance at DC OFFSET (see Note 3) | | 1 | 3 | | MΩ |
| $I_{I(SIG)}$ | Average input current into SIG | $GND < V_I < AV_{DD}$ | | 50 | 200 | nA |
| $C_i$ | Input capacitance, analog input at SIG | | | 10 | | pF |

NOTE 3: The input is capacitive and, therefore, is dynamic. Impedance specifications are based on $f_{(CLK)} = 38.4$ kHz.

## operating characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 3$ V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

### peak-and-valley DACs

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Step size, LSB | | | $V_{DD}/255$ | | V |
| $E_{FS}$ | Full-scale error | | | | ±1 | LSB |
| $E_{ZS}$ | Zero-code error | | | | ±3 | LSB |
| | Voltage output drift | Hold mode | | 0 | | mV/ms |
| $E_D$ | Differential linearity error | | | | ±1 | LSB |

### low-pass filter

| | PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| G | Pass band filter gain | | $V_{I(DC\ OFFSET)} = 0.8$ V, | $V_I = \pm 125$ mV | 11.5 | 12 | 12.5 | dB |
| | Filter attenuation | 1-kHz filter | $V_I = \pm 500$ mV | $f_{I(SIG)} = 1$ kHz | 2 | 3 | 4 | dB |
| | | 2-kHz filter | $V_I = \pm 500$ mV | $f_{I(SIG)} = 2$ kHz | 2 | 3 | 4 | dB |
| $t_S$ | Stabilization time | | Off mode to hold mode (see Table 1) | | | | 5 | ms |

## PARAMETER MEASUREMENT INFORMATION
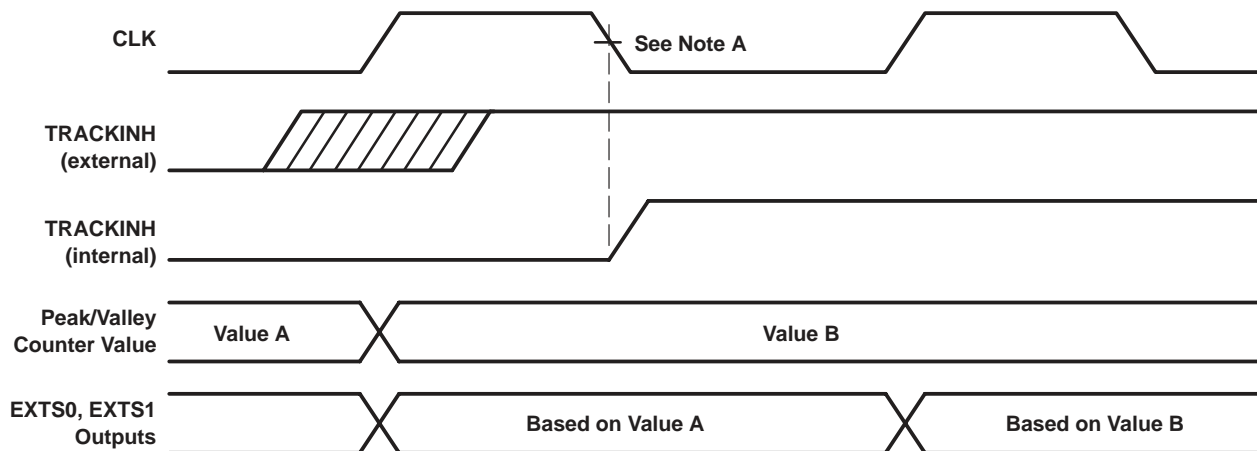


NOTE A: Internally the device recognizes input conditions on the falling edge of the clock only.

**Figure 1. Timing Diagram**
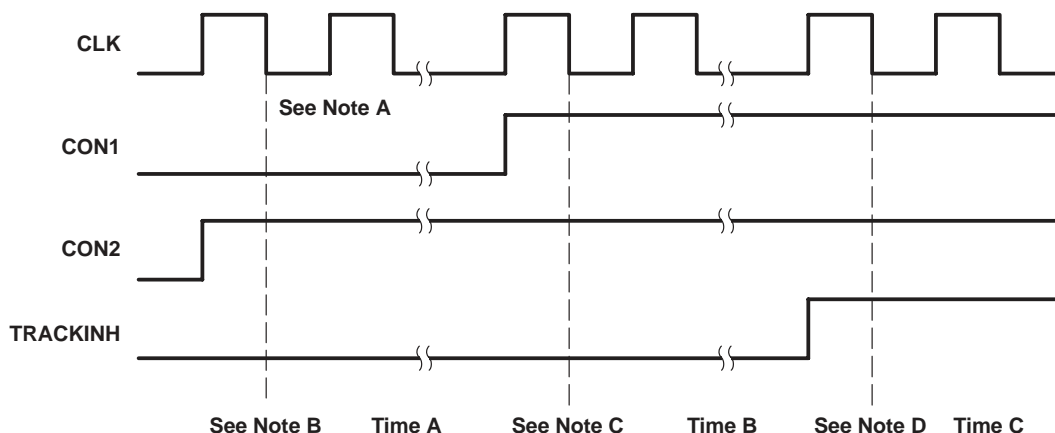


NOTES: A. Internally the device recognizes input conditions on the falling edge of the clock only.
B. On the next falling edge of the clock with the input conditions shown, the TLV5590 tracks signal in fast mode (peak DAC counter counts down by 8 and up by 4) in time A.
C. On the next falling edge of the clock with the input conditions shown, the TLV5590 tracks signal in slow mode (peak DAC counter counts up by 2 and down by 1 every 40 clock cycles) in time B.
D. On the next falling edge of the clock with the input conditions shown, the TLV5590 holds previous peak and valley levels in time C. For the 2 bit ADC, when TRACKINH = 1, EXTS0 and EXTS1 outputs respond in real time to the condition of SIG and DC OFFSET as long as the CLK signal is present.

**Figure 2. Track and Lock Timing**

## TYPICAL CHARACTERISTICS
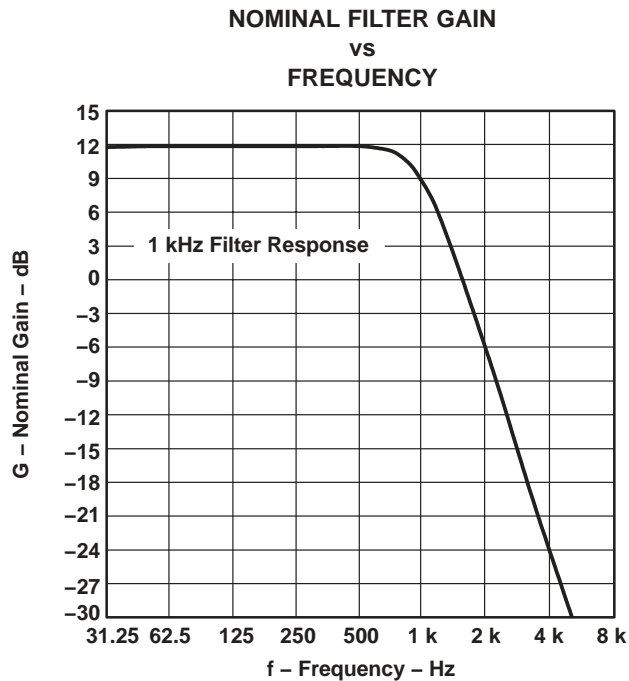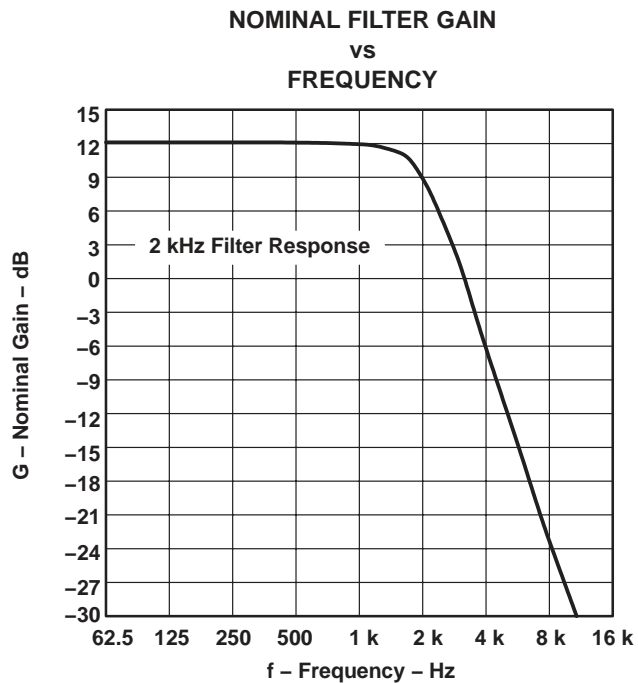
**NOMINAL FILTER GAIN**
**vs**
**FREQUENCY**



1 kHz Filter Response

G – Nominal Gain – dB

f – Frequency – Hz

**Figure 3**

**NOMINAL FILTER GAIN**
**vs**
**FREQUENCY**



2 kHz Filter Response

G – Nominal Gain – dB

f – Frequency – Hz

**Figure 4**

## PRINCIPLES OF OPERATION

### analog input operation

Referring to the functional block diagram, the signal input is dc-coupled using a single input terminal, SIG. The nominal dc content of the signal input should be supplied on an additional terminal, DC OFFSET. This allows the device to gain the signal to acceptable levels for threshold detection, without saturating against the supplies. The signal processed by the device is effectively the voltage difference between the SIG and DC OFFSET terminals.

There is no antialiasing filter incorporated in the device and it is recommended that this filtering be added externally by an external RC filter set at the appropriate cutoff (see Figure 5).

The maximum peak analog-signal voltage that can be applied to the SIG input terminal is given by:

$$V_{I(PEAK)} = \frac{\left(\dfrac{V_{DD}}{2} - 0.25\right)}{4.217} - V_{I(OFFSET)} - 80 \text{ mV}$$

where

$$V_{DD}/2 = \text{the nominal output voltage at the MID terminal}$$

$$V_Q = \text{the dc quiescent voltage of the input signal}$$

$$V_{I(DC\ OFFSET)} = \text{the voltage applied to the DC OFFSET terminal}$$

and

$$V_{I(OFFSET)} = V_Q - V_{I(DC\ OFFSET)}$$

The value of 80 mV is the tolerance of the output voltage for the MID terminal at the output of the internal filter amplifier.

The peak-to-peak input voltage swing is double the result shown in the equation.

The main signal path consists of a third-order switched-capacitor butterworth filter, with a switchable bandwidth between 1 kHz and 2 kHz, to remove the noise from the input signal. The peak and valley amplitudes of the filter output signal are detected and subsequently used to convert the 4-level audio into 2-level digital signals using three switched capacitor comparators.

### digital operation

The peak and valley detection is performed by a mixed mode solution, using an 8-bit DAC and an up/down counter that has nonsymmetrical up and down count rates. Various modes are included to force the peak and valley circuits to slow track, fast track, or hold. An off mode is included that forces the device into a low-power condition. The decay rate of the peak and valley circuits are controlled by independent counters.

The device is clocked with a 38.4 kHz square wave supplied externally. The attack and decay times of the peak and valley circuits, and the filter cut-off frequencies are directly related to this clock frequency. The decay timer is gated by the track inhibit input TRACKINH, and is reset to 1 after an attack occurs, and is reset to 40 after a decay enable. The TRACKINH also prevents attack enable inputs from affecting the peak and valley counters.

**PRINCIPLES OF OPERATION**

### digital control

There are five digital inputs that control the TLV5590, along with the CLK input. The five signals are BW, CON1, CON2, TRACKINH and TEST. All digital control inputs are latched internally on the falling edge of the CLK input. The BW input selects the cut-off frequency of the input signal third-order Butterworth switched-capacitor filter. The CON1 and CON2 inputs determine when the TLV5590 is in tracking fast, tracking slow, hold, or low-power standby mode. In test mode the CLK input is level sensitive, and in all other modes the CLK input is edge-sensitive.

Table 1 lists the functions for the five control inputs.

**Table 1. Control Inputs Function Table**

| BW | | SWITCHED-CAPACITOR FILTER (– 3 dB POINT) |
|---|---|---|
| Low | | 1-kHz filter cutoff |
| High | | 2-kHz filter cutoff |
| **CON1** | **CON2** | **MODE** |
| Low | Low | Low-power standby (off) mode |
| Low | High | Fast track mode |
| High | Low | Hold mode |
| High | High | Slow track mode |
| **TRACKINH** | | **RESULT** |
| Low | | Tracking enabled |
| High | | Tracking disabled |

### track inhibit

The TRACKINH input enables the counters to the peak and valley detector DACs. When enabled, the counters are adjusting to create a DAC output that is the same as the filtered input-signal peak and valley. The counters decay at the fast or slow decay rates while the TRACKINH input is held low. The TRACKINH line should be connected to SYMCLK terminal on the TLV5591.

### analog-to-digital conversion

The TLV5590 employs a 2-bit ADC to convert a 4-level analog signal to digital data. The digital output is presented on EXTS0 and EXTS1 with EXTS0 being the LSB. The peak and valley DACs provide the maximum and minimum voltages ($V_{ref+}$ and $V_{ref-}$) to the ADC. The input to the 2-bit ADC is the output of the Butterworth low-pass filter, FILOUT, as shown in the block diagram. The ADC transfer function is shown in Table 2.

**Table 2. Filter Output Voltage Selection (see Note 4)**

| EXTS1 | EXTS0 | FILTER OUTPUT VOLTAGE (FILOUT) |
|---|---|---|
| Low | Low | FILOUT < ((peak – valley) x 50/256) + valley |
| High | Low | ((peak – valley) x 50/256) + valley < FILOUT < ((peak – valley) x 134/256) + valley |
| High | High | ((peak – valley) x 134/256) + valley < FILOUT < (( peak – valley) x 217/256) + valley |
| Low | High | FILOUT > ((peak – valley) x 217/256) + valley |

NOTE 4.   The constants 50/256, 134/256, and 217/256 have a $\pm$ 5% tolerance.

## PRINCIPLES OF OPERATION

The thresholds for the ADC comparators are set by capacitor ratios in switched-capacitor comparators. For a 2-bit ADC, three comparators are used with thresholds set as shown in Table 3.

**Table 3. Comparators and Associated Threshold Values (see Notes 4 and 5)**

| COMPARATOR | VALUE | UNIT |
|---|---|---|
| Lower threshold | ((peak – valley) x 50/256) + valley | V |
| Middle threshold | ((peak – valley) x 134/256) + valley | V |
| Upper threshold | ((peak – valley) x 217/256) + valley | V |

NOTES:  4. The constants 50/256, 134/256, and 217/256 have a $\pm$ 5% tolerance.
5. The comparator thresholds are measured with the input voltage level of the SIG terminal at 125 mV ac centered on 800 mV dc and the input voltage at the DC OFFSET terminal is 800 mV dc.

### peak and valley timing

The peak and valley attack and delay times are controlled by two 8-bit up/down counters clocked by the CLK input. The rate that the counters are clocked depends on whether the counters are in attack or decay mode. The peak counter is in attack mode when the input signal amplitude is greater than the output voltage from the peak DAC, and it is in decay mode when the input signal amplitude is less that the peak DAC output voltage. The valley counter is in attack mode when the input signal amplitude is less than the output voltage from the valley DAC, and it is in decay mode when the input signal amplitude is greater than the valley DAC output voltage.

When TRACKINH is held high, the attack and decay enable inputs to the peak and valley counters are disabled. When held low the attack and decay enable inputs to the peak and valley counters are enabled. The effect of the TRACKINH signal is exactly the same as when the device is configured in hold mode.

### slow-acquisition-mode attack and decay times

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 2] / 256$ / (TRACKINH duty cycle). So the peak and valley counter is incremented/decremented by a count of 2 on every clock cycle when the input signal amplitude is greater or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)}] / (256 \times 40)$ / (TRACKINH duty cycle). So the peak and valley counter is decremented or incremented once every 40 clock cycles when the input signal amplitude is less or greater than the peak and valley DAC output voltage.

When the counters receive an attack enable at the same time as a decay enable then the attack enable takes precedence. The decay counter is reset to 1 after an attack and reset to 40 following a decay.

With a $V_{DD}$ supply variation of 2.7 V to 3.3 V, and a fixed clock input of 38.4 kHz, the attack and decay times are given in Table 4.

**Table 4. Slow Acquisition Mode Attack and Decay Times**

| DESCRIPTION | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Attack Rate (ATTR) | TRACKINH = Low | 810 | 990 | mV/ms |
| Decay Rate (DECR) | TRACKINH = Low | 10.125 | 12.375 | mV/ms |

**TEXAS INSTRUMENTS**

**PRINCIPLES OF OPERATION**

**fast-acquisition-mode attack and decay times**

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 4] / 256 / $ (TRACKINH duty cycle). So the peak and valley counter is incremented or decremented by a count of 4 on every clock cycle when the input signal amplitude is greater or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 8] / 256 / $ (TRACKINH duty cycle). So the peak and valley counter is decrement or increment by a count of 8 on every clock cycle when the input signal amplitude is less or greater than the peak and valley DAC output voltage.

When the device is in fast aquistion mode then the decay counter is reset to 1.

With a $V_{DD}$ supply variation of 2.7 V to 3.3 V, and a fixed clock input of 38.4 kHz, the attack and decay times are given in Table 5.

**Table 5. Fast Acquisition Mode Attack and Decay Times**

| DESCRIPTION | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Attack Rate (ATTR) | TRACKINH = Low | 1620 | 1980 | mV/ms |
| Decay Rate (DECR) | TRACKINH = Low | 3240 | 3960 | mV/ms |

**hold mode**

In hold mode the peak and valley counters are disabled from counting when either attack or decay enable signals are present. There is no change to the peak and valley DAC output voltages in this mode.

When the device is in hold mode then the decay counter is reset to 1.

**off mode**

In the off mode the peak and valley counters are disabled from counting, and the device is set into low power standby mode. The peak and valley voltages both float to the $V_{DD}$ voltage as the resistor string element within the DAC structure is isolated from the GND supply to conserve power. When the off state is released the peak and valley voltages return to the previously set values.

When the device is in off mode then the decay counter is reset to 1.

**test**

The TEST input allows access to internal circuitry for production testing purposes and the pager system debug. For normal operation, TEST should be tied to ground. For the debug and test mode, the TEST input should be held high. The various operating modes are described in the following sections.

## PRINCIPLES OF OPERATION

### test mode 0 – peak and valley DACs and logic testing

Test mode 0 can be used for production testing and allows complete testing of the peak and valley DAC counters, decay counters, and the peak and valley DACs. The peak and valley DAC voltage outputs are accessible on the EXTS1 and EXTS0 terminals respectively, and the decay rate-counter outputs are accessible on the SIG terminal. The DAC counters are controlled by the various digital inputs. The BW input controls the counter reset, and the TRACKINH input controls the peak and valley DAC counters up and down control, and multiplexes the decay rate-counter outputs onto the SIG terminal. The DC OFFSET input selects the counters fast and slow modes of operation. The counters are enabled and are clocked on each rising edge of the CLK input. Table 6 contains a terminal function summary of this test mode.

**Table 6. Test Mode 0 Selection**

| TEST = HIGH, CON1 = LOW, CON2 = LOW | | |
|---|---|---|
| **TEST INPUTS** | | |
| **TERMINAL** | **INPUT** | **RESULT / MODE** |
| BW | Low | Logic enabled |
| | High | Logic reset |
| TRACKINH | Low | Peak and valley counters count down, valley-decay counter output on SIG terminal. |
| | High | Peak and valley counters count up, peak decay-counter output on SIG terminal. |
| DC OFFSET | Low | Device taken from fast mode to test mode 0:<br>a) Peak counter counts in slow mode<br>b) Valley counter counts in fast mode |
| | | Device taken from slow mode to test mode 0, and the peak and valley counters count in slow mode. |
| | High | Device taken from fast mode to test mode 0:<br>a) Peak counter counts in fast mode<br>b) Valley counter counts in slow mode |
| | | Device taken from slow mode to test mode 0, and the peak and valley counters count in fast mode. |
| **TEST OUTPUTS** | | |
| **TERMINAL** | **CONDITIONS** | **RESULT / MODE** |
| EXTS1 | | Peak DAC voltage |
| EXTS0 | | Valley DAC voltage |
| SIG† | TRACKINH = Low | Valley-decay counter output |
| | TRACKINH = High | Peak-decay counter output |

† This function is valid when transitioning from slow mode to the test mode 0. In fast mode, the DC OFFSET terminal function is inverted for the valley counter only.

**PRINCIPLES OF OPERATION**

### test mode 1 – switched-capacitor filter test

Test mode 1 places the output of the switched-capacitor low-pass filter directly on EXTS1. Note that the filter output is not capable of driving an external load and, therefore, must be buffered externally at the EXTS1 terminal of the TLV5590. The BW input selects the filter cut-off frequency. The peak and valley DAC counters, the decay counters, and the 2-bit ADC are all disabled during this test mode. Table 7 contains a terminal function summary of this test mode.

**Table 7. Test Mode 1 Selection**

| TEST = HIGH, CON1 = LOW, CON2 = HIGH | | |
|---|---|---|
| **TEST INPUT** | | |
| **TERMINAL** | **INPUT** | **RESULT/MODE** |
| BW | Low | 1-kHz cutoff frequency (–3 dB) |
| | High | 2-kHz cutoff frequency (–3 dB) |
| **TEST OUTPUT** | | |
| **TERMINAL** | **OUTPUT SIGNAL** | |
| EXTS1 | Switched-capacitor filter output (unbuffered)† | |

† The filter output must be buffered externally for testing.

### test mode 2 – peak and valley DAC output test

Test mode 2 allows direct access to the peak and valley comparators and can be used for the pager system debug. The peak and valley comparator outputs are accessible on the EXTS0 and EXTS1 terminals respectively. The peak and valley counters are held at a constant value using the hold mode. Table 8 contains a terminal function summary of this test mode.

**Table 8. Test Mode 2 Selection**

| TEST = HIGH, CON1 = HIGH, CON2 = LOW | |
|---|---|
| **TEST OUTPUTS** | |
| **TERMINAL** | **OUTPUT SIGNAL** |
| EXTS1 | Peak DAC voltage |
| EXTS2 | Valley DAC voltage |

## PRINCIPLES OF OPERATION

### test mode 3 – comparator threshold test

Test mode 3 allows a dc input voltage to be applied to force the peak and valley DAC voltages to settle independently at their nominal output voltages including any effects of the filter dc offsets, gain errors, etc. The input signal can then be set at the comparator switching thresholds and the correct outputs should be decoded. The normal outputs of the ADC are present on EXTS0 and EXTS1. The BW and TRACKINH inputs override the peak and valley DAC counter disables. The switched-capacitor filter is forced into a 1-kHz cut-off mode. Table 9 contains a terminal function summary of this test mode.

**Table 9. Test Mode 3 Selection**

| TEST = HIGH, CON1 = HIGH, CON2 = HIGH | | |
|---|---|---|
| **TEST INPUTS** | | |
| **TERMINAL** | **INPUT** | **RESULT** |
| BW | Low | Peak DAC counter normal operation |
| BW | High | Peak DAC counter disabled |
| TRACKINH | Low | Valley DAC counter normal operation |
| TRACKINH | High | Valley DAC counter disabled |

## APPLICATION INFORMATION

The TLV5590 is optimized for pager applications. The TLV5590 optimizes the filtering and conversion resolution to meet the specific requirements of FLEX pagers. The combination of the TLV5590 and TLV5591 reduce overall system cost by allowing a lower cost microcontroller to be used in the pager system. Figure 5 shows the basic connections between system elements.
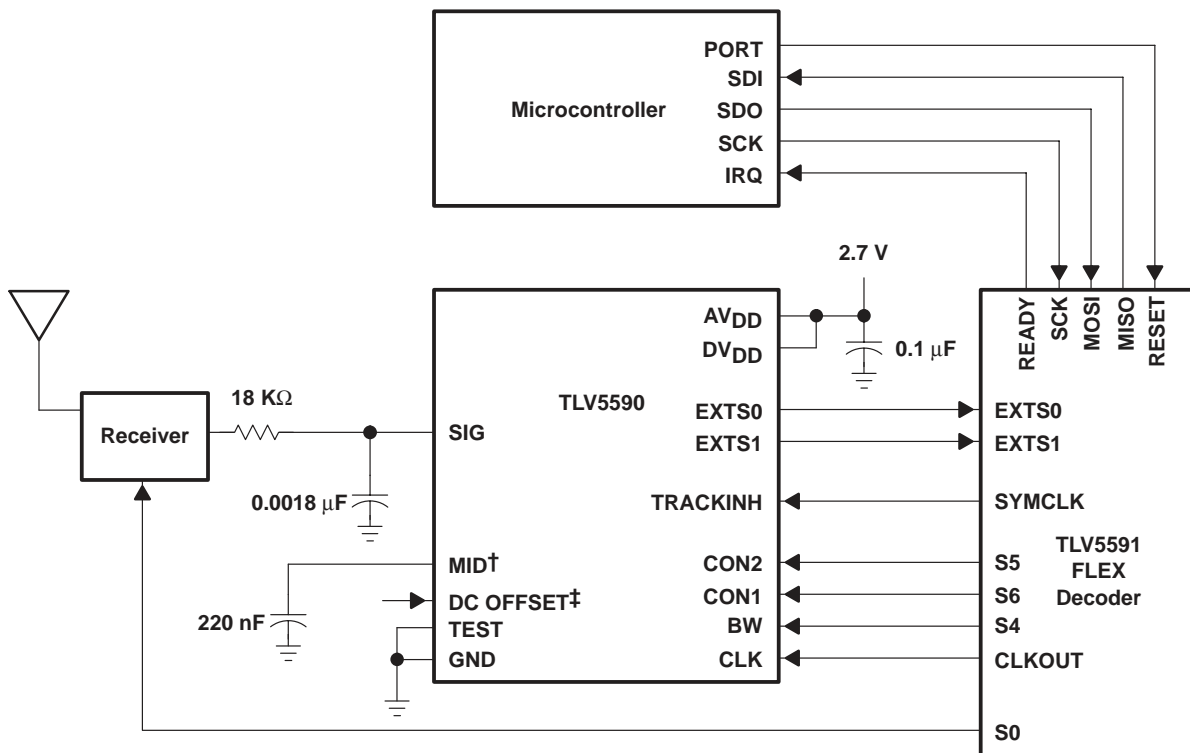


† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG terminal.

**Figure 5. TLV5590 Application Schematic**

At least one bit of warm-up time in fast track mode followed by five bits of warm-up time in slow track mode is necessary before valid data can be present. Hold mode is used during a data transfer, and fast track mode is used for warm-up. Slow track mode is used for tracking during the synchronization portion of the data.