

# Isolated USB Data Transceiver

## FEATURES

- Isolated USB Transceiver: 7500V<sub>RMS</sub> for 1 Minute
- CSA (IEC/UL) Approved, File #255632
- Reinforced Insulation
- USB 2.0 Full Speed and Low Speed Compatible
- Auto-Configuration of Bus Speed
- 4.4V to 36V V<sub>BUS</sub> and V<sub>BUS2</sub> Operating Range
- 3.3V LDO Output Supply Signal References V<sub>LO</sub> and V<sub>LO2</sub>
- 50kV/μs Common Mode Transient Immunity
- ±20kV HBM ESD on USB Interface Pins
- 1414V<sub>PEAK</sub> Maximum Continuous Working Voltage
- 17.4mm Creepage Distance
- 22mm × 6.25mm Surface Mount BGA

## APPLICATIONS

- Isolated USB Interfaces
- Host, Hub, or Device Isolation
- Industrial/Medical Data Acquisition

## DESCRIPTION

The LTM<sup>®</sup>2894 is a complete galvanically-isolated USB 2.0 compatible μModule<sup>®</sup> (micromodule) transceiver.

The LTM2894 is ideal for isolation in host, hub, bus splitter or peripheral device applications. It is compatible with USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) operation. Automatic speed selection configures integrated pull-up resistors on the upstream port to match those sensed on the downstream device.

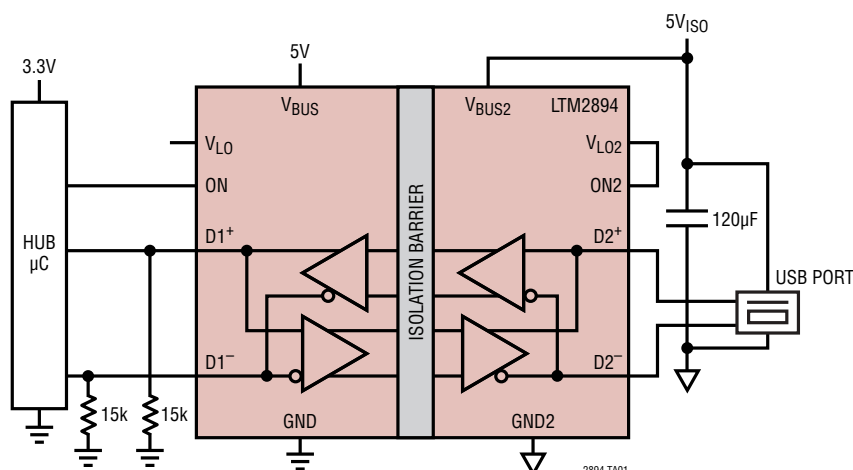
The isolator μModule technology uses coupled inductors to provide 7500V<sub>RMS</sub> of isolation and 17.4mm of creepage between the upstream and downstream USB interface. This device is ideal for systems requiring isolated ground returns or large common mode voltage variations. Uninterrupted communication is guaranteed for common mode transients greater than 50kV/μs.

Enhanced ESD protection allows this part to withstand up to ±20kV (human body model) on the USB transceiver interface pins to local supplies and ±20kV through the isolation barrier to supplies without latchup or damage.

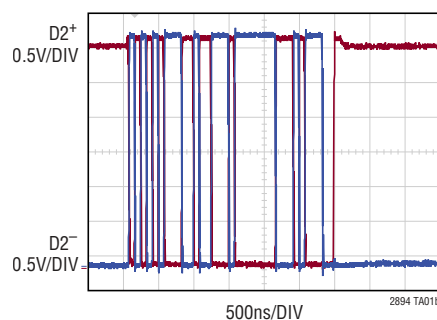
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## TYPICAL APPLICATION

Isolated V2.0 Full Speed Hub Port



Full Speed Data



# LTM2894

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

### Supply Voltages

$V_{BUS}$ to GND .....	–0.3V to 45V
$V_{BUS2}$ to GND2 .....	–0.3V to 45V
$V_{LO}$ to GND .....	–0.3V to 4V
$V_{LO2}$ to GND2 .....	–0.3V to 4V
ON to GND .....	–0.3V to ( $V_{LO} + 0.3$ )
ON2 to GND2 .....	–0.3V to ( $V_{LO2} + 0.3$ )
D1 <sup>+</sup> , D1 <sup>–</sup> to GND .....	–0.3V to 5.3V
D2 <sup>+</sup> , D2 <sup>–</sup> to GND2 .....	–0.3V to 5.3V

### Operating Temperature Range

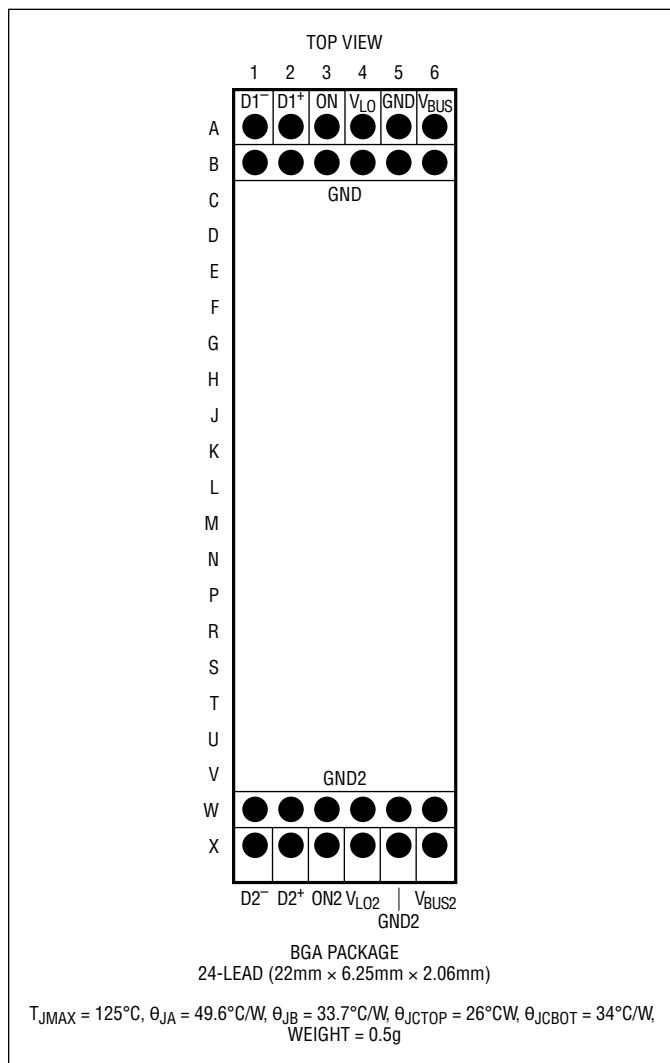
LTM2894C (Notes 1, 3) .....	0 to 70°C
LTM2894I (Notes 1, 3) .....	–40 to 85°C
LTM2894H (Notes 1, 3) .....	–40 to 125°C

### Storage Temperature Range .....

Maximum Internal Operating Temperature..... 125°C

Lead Temperature (Soldering, 10 sec)..... 260°C

## PIN CONFIGURATION



## ORDER INFORMATION

PART NUMBER	PACKAGE TYPE	BALL FINISH	PART MARKING		MSL RATING	TEMPERATURE RANGE
			DEVICE	FINISH CODE		
LTM2894CY#PBF	BGA	SAC305 (RoHS)	LTM2894Y	e1	3	0°C to 70°C
LTM2894IY#PBF						–40°C to 85°C
LTM2894HY#PBF						–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to [Recommended BGA PCB Assembly and Manufacturing Procedures](#).

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{\text{BUS}} = 5\text{V}$ ,  $V_{\text{BUS2}} = 5\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = 3.3\text{V}$ ,  $\text{ON2} = 3.3\text{V}$

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Power Supply</b>							
$V_{\text{BUS}}$	Operating Supply Range (USB Bus Power Input)		●	4.4	5	36	V
$I_{\text{BUSPOFF}}$	$V_{\text{BUS}}$ Supply Current Power Off	$\text{ON} = 0\text{V}$	●		1	20	$\mu\text{A}$
$I_{\text{BUS}}$	$V_{\text{BUS}}$ Supply Current Power On	Figure 1, $V_{\text{BUS}} = 5\text{V}$ , $I_{\text{VLO}} = 0\text{mA}$	●		5	9	mA
$I_{\text{BUSSPND}}$	$V_{\text{BUS}}$ Supply Current Suspend Mode	$V_{\text{BUS}} = 5\text{V}$ , USB Suspend Timeout	●		1.5	2.0	mA
$V_{\text{BUS2}}$	Operating Supply Range (Isolated Power Input)		●	4.4	5	36	V
$I_{\text{BUS2POFF}}$	$V_{\text{BUS2}}$ Supply Current Power Off	$\text{ON2} = 0\text{V}$	●		1	10	$\mu\text{A}$
$I_{\text{BUS2}}$	$V_{\text{BUS2}}$ Supply Current Power On	Figure 1, $V_{\text{BUS2}} = 5\text{V}$ , $I_{\text{VLO2}} = 0\text{mA}$	●		5	9	mA
$I_{\text{BUS2SPND}}$	$V_{\text{BUS2}}$ Supply Current Suspend Mode	$V_{\text{BUS2}} = 5\text{V}$ , USB Suspend Timeout	●		5	9	mA
$V_{\text{LO}}$	$V_{\text{LO}}$ Regulated Output Voltage Signal Reference	Figure 1, $I_{\text{VLO}} = 0\text{mA}$	●	3.05	3.3	3.55	V
	$V_{\text{LO}}$ Output Voltage Maximum Current Source	Figure 1	●			10	mA
$V_{\text{LO2}}$	$V_{\text{LO2}}$ Regulated Output Voltage Signal Reference	Figure 1, $I_{\text{VLO2}} = 0\text{mA}$	●	3.05	3.3	3.55	V
	$V_{\text{LO2}}$ Output Voltage Maximum Current Source	Figure 1	●			10	mA
<b>USB Input Levels (<math>\text{D1}^+</math>, <math>\text{D1}^-</math>, <math>\text{D2}^+</math>, <math>\text{D2}^-</math>)</b>							
	Single-Ended Input High Voltage		●	2.0			V
	Single-Ended Input Low Voltage		●			0.8	V
	Single-Ended Input Hysteresis		●		200		mV
	Differential Input Sensitivity	$ (D1^+ - D1^-) $ or $ (D2^+ - D2^-) $	●	0.2			V
	Common Mode Voltage Range	$(D1^+ + D1^-)/2$ or $(D2^+ + D2^-)/2$	●	0.8		2.5	V
<b>Logic Input Levels (<math>\text{ON}</math>, <math>\text{ON2}</math>)</b>							
	Logic Input High Voltage		●	2.0			V
	Logic Input Low Voltage		●			0.8	V
	Logic Input Current		●			$\pm 1$	$\mu\text{A}$
	Logic Input Hysteresis				200		mV
<b>USB Output Levels (<math>\text{D1}^+</math>, <math>\text{D1}^-</math>, <math>\text{D2}^+</math>, <math>\text{D2}^-</math>)</b>							
	Output Low Voltage	$R_{\text{PU}} = 1.5\text{k}\Omega$ to $3.6\text{V}$ , Figure 2	●	0		0.3	V
	Output High Voltage	$R_{\text{PD}} = 15\text{k}\Omega$ to $0\text{V}$	●	2.8		3.6	V
	Differential Output Signal Cross-Point Voltage		●	1.3		2.0	V
<b>Terminations</b>							
$R_{\text{PU}}$	Bus Pull-Up Resistance on Upstream Facing Port	$\text{D2}^+$ or $\text{D2}^-$ Pull-Up $1.5\text{k}\Omega$ to $3.3\text{V}$	●	1.425		1.575	$\text{k}\Omega$
$R_{\text{PD}}$	Bus Pull-Down Resistance on Downstream Facing Port ( $\text{D2}^+$ and $\text{D2}^-$ )	$\text{D2}^+$ and $\text{D2}^-$ Pull-Down to $\text{GND2}$	●	14.25		15.75	$\text{k}\Omega$
$Z_{\text{DRV}}$	USB Driver Output Resistance		●	28		44	$\Omega$
	USB Transceiver Pad Capacitance to $\text{GND}$	(Note 2)			10		pF

## SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{BUS} = 5\text{V}$ ,  $V_{BUS2} = 5\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = 3.3\text{V}$ ,  $\text{ON2} = 3.3\text{V}$ .

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Low Speed USB</b>							
$t_{LDR}$	Low Speed Data Rate	$C_L = 50\text{pF}$ to $450\text{pF}$ (Note 4)			1.5		Mbps
$t_{LR}$	Rise Time	Figure 2, $C_L = 50\text{pF}$ to $600\text{pF}$	●	75		300	ns
$t_{LF}$	Fall Time	Figure 2, $C_L = 50\text{pF}$ to $600\text{pF}$	●	75		300	ns
$t_{LPRR}, t_{LPFF}$	Propagation Delay	Figure 2, $C_L = 50\text{pF}$ to $600\text{pF}$	●		200	300	ns
	Differential Jitter	To Next Transition (Note 8)				$\pm 45$	ns
	Differential Jitter	To Paired Transitions (Note 8)				$\pm 15$	ns
<b>Full Speed USB</b>							
$t_{FDR}$	Full Speed Data Rate	$C_L = 50\text{pF}$ (Note 4)			12		Mbps
$t_{FR}$	Rise Time	Figure 3, $C_L = 50\text{pF}$	●	4		20	ns
$t_{FF}$	Fall Time	Figure 3, $C_L = 50\text{pF}$	●	4		20	ns
$t_{FPRR}, t_{FPFF}$	Propagation Delay	Figure 3, $C_L = 50\text{pF}$	●	60	80	115	ns
	Differential Jitter	To Next Transition (Note 8)			2		ns
	Differential Jitter	To Paired Transitions (Note 8)			1		ns
<b>Suspend</b>							
	Wake Up from Suspend Mode	Resume Signal	●		0.25	10	$\mu\text{s}$
<b>ESD HBM (Note 8)</b>							
	Isolation Barrier	GND to GND2			$\pm 20$		kV
	D1 <sup>+</sup> , D1 <sup>-</sup> , D2 <sup>+</sup> , D2 <sup>-</sup>	D1 <sup>+</sup> /D1 <sup>-</sup> to GND, $V_{BUS}$ , or $V_{L0}$ D2 <sup>+</sup> /D2 <sup>-</sup> to GND2, $V_{BUS2}$ , or $V_{L02}$			$\pm 20$		kV
	ON or ON2				$\pm 4$		kV

## ISOLATION CHARACTERISTICS

Specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Isolation Barrier: GND to GND2</b>						
$V_{ISO}$	Rated Dielectric Insulation Voltage (Notes 6, 7)	1 Minute (Derived from 1 Second Test)	7500			$V_{RMS}$
		1 Second (Note 5)	9000			$V_{RMS}$
	Common Mode Transient Immunity	(Note 2)	50	75		$\text{kV}/\mu\text{s}$
$V_{IORM}$	Maximum Working Insulation Voltage	(Note 2)	1414			$V_{PEAK}, V_{DC}$
			1000			$V_{RMS}$
	Partial Discharge	$V_{PR} = 2650 V_{PEAK}$ (Note 5)			5	$\text{pC}$
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			$V_{RMS}$
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.2		mm
	Input to Output Resistance	(Notes 2, 5)	1	5		$\text{T}\Omega$
	Input to Output Capacitance	(Notes 2, 5)		2		$\text{pF}$
	Creepage Distance	(Notes 2, 5)		18.1		mm

### CSA (Note 9)

CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1 +A2:

Basic Insulation at  $910V_{RMS}$

Reinforced Insulation at  $455V_{RMS}$

CSA 62368-1-14 and IEC 62368-1-14:2014, second edition:

Basic Insulation at  $600V_{RMS}$

Reinforced Insulation at  $455V_{RMS}$

CSA 60601-1:14 and IEC 60601-1, third edition, +A1:

Two means of patient protection (2 MOPP) at  $287.5V_{RMS}$

UL 1577-2015:

Single Protection,  $6000V_{RMS}$  Isolation Voltage

File 255632

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Guaranteed by design and not subject to test.

**Note 3:** This  $\mu$ Module transceiver includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

**Note 4:** Maximum data rate is guaranteed by other measured parameters and is not directly tested.

**Note 5:** Device considered a 2-terminal device. Measurement between groups of pins A1 through B6 shorted together and pins W1 through X6 shorted together.

**Note 6:** The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

**Note 7:** In accordance with UL1577, each device is proof tested at the  $7500V_{RMS}$  rating by applying an acceleration factor of 1.2,  $9000V_{RMS}$ , for one second.

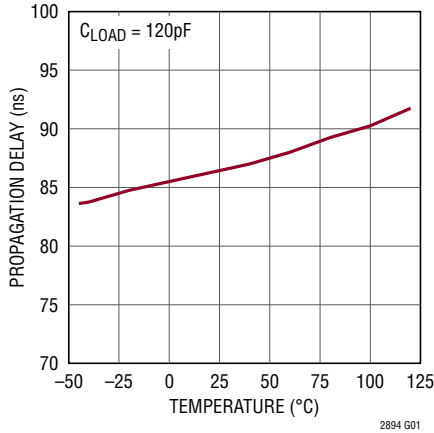
**Note 8:** Evaluated by design, not production tested.

**Note 9:** Ratings are for pollution degree 2, material group 3 and overvoltage category II where applicable. Ratings for other environmental and electrical conditions to be determined from the appropriate safety standard.

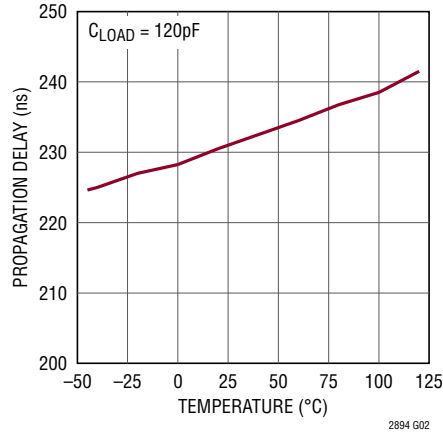
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.  $V_{\text{BUS}} = 5\text{V}$ ,  $V_{\text{BUS2}} = 5\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = 3.3\text{V}$ ,  $\text{ON2} = 3.3\text{V}$ .

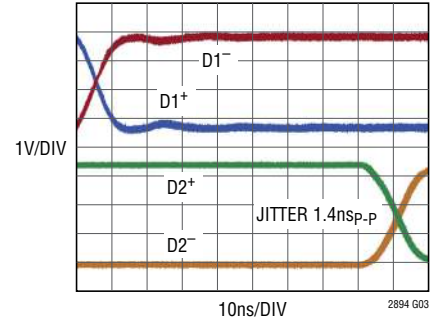
**Full Speed Propagation Delay vs Temperature**



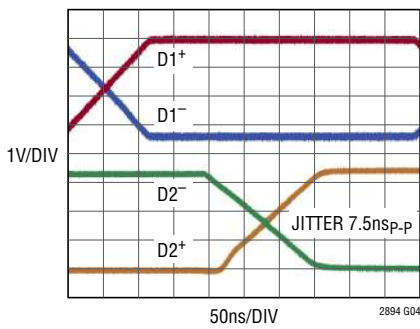
**Low Speed Propagation Delay vs Temperature**



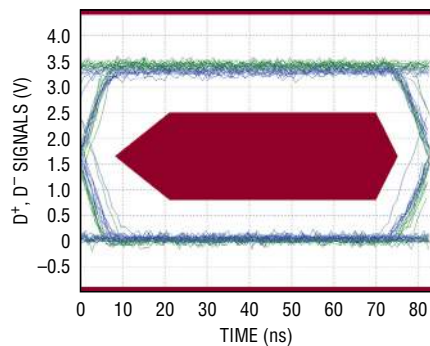
**Full Speed Differential Jitter**



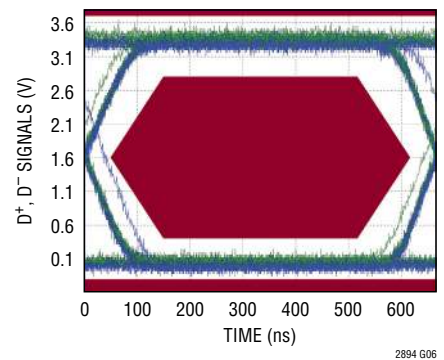
**Low Speed Differential Jitter**



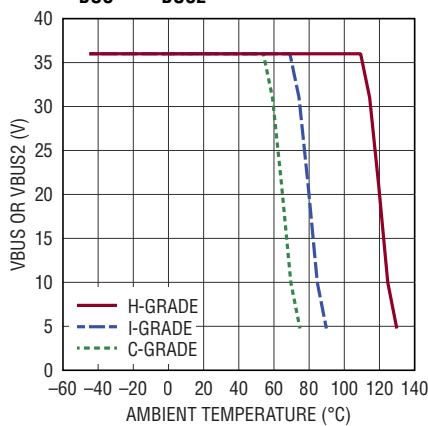
**Full Speed Eye Diagram**



**Low Speed Eye Diagram**

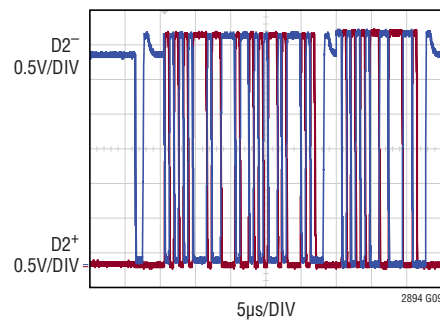


**Thermal Derating for Operating Temperature Range vs  $V_{\text{BUS}}$  or  $V_{\text{BUS2}}$**



LIMITED BY JUNCTION  
TEMPERATURE RISE PER GRADE  
 $\theta_{JA} = 49.6^\circ\text{C/W}$

**Low Speed Data**



## PIN FUNCTIONS

### Upstream Side

**D1<sup>-</sup> (A1):** USB Data Bus Upstream Facing Negative Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D1<sup>-</sup> pin.

**D1<sup>+</sup> (A2):** USB Data Bus Upstream Facing Positive Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D1<sup>+</sup> pin.

**ON (A3):** Enable. Enables data communication through the isolation barrier. If ON is high, the upstream side is enabled. If ON is low, the upstream side is held in reset. The ON pin is referenced between  $V_{LO}$  and GND.

**$V_{LO}$  (A4):** Voltage Supply Output from the Upstream Side 3.3V LDO. The  $V_{LO}$  pin is used as a positive reference for the ON pin and can support up to 10mA of surplus current to controlling devices. This pin contains internal ceramic bypass capacitance of 4.4 $\mu$ F.

**GND (A5, B1 - B6):** Upstream Circuit Ground.

**$V_{BUS}$  (A6):** Voltage Supply Input for Upstream USB Transceiver. Recommended operating range is 4.4V to 36V. Connect to the USB  $V_{BUS}$  supply or an external source. This pin contains internal ceramic bypass capacitance of 0.3 $\mu$ F.

### Downstream Side

**GND2 (W1 - W6, X5):** Downstream Circuit Ground.

**D2<sup>-</sup> (X1):** USB Data Bus Downstream Facing Negative Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

**D2<sup>+</sup> (X2):** USB Data Bus Downstream Facing Positive Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

**ON2 (X3):** Enable. Enables data communication through the isolation barrier. If ON2 is high, the downstream side is enabled. If ON2 is low, the downstream side is held in reset. The ON2 pin is referenced between  $V_{LO2}$  and GND2.

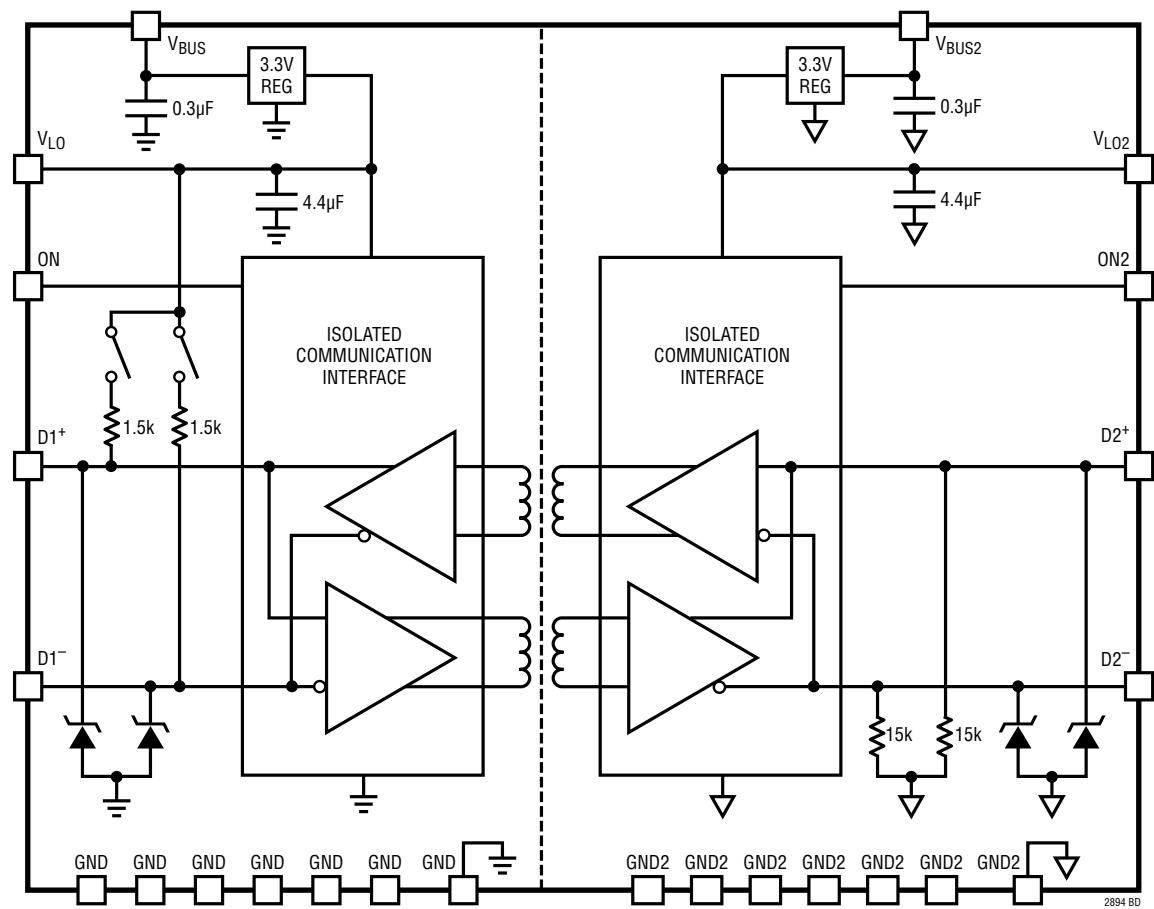
**$V_{LO2}$  (X4):** Voltage Supply Output from the Downstream Side 3.3V LDO. The  $V_{LO2}$  pin can support up to 10mA of surplus current for low voltage devices. This pin contains internal ceramic bypass capacitance of 4.4 $\mu$ F.

**$V_{BUS2}$  (X6):** Voltage Supply Input for the Isolated Downstream USB Transceiver. Recommended operating range is 4.4V to 36V referenced to GND2. This pin contains internal ceramic bypass capacitance of 0.3 $\mu$ F.



**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

BLOCK DIAGRAM



TEST CIRCUITS

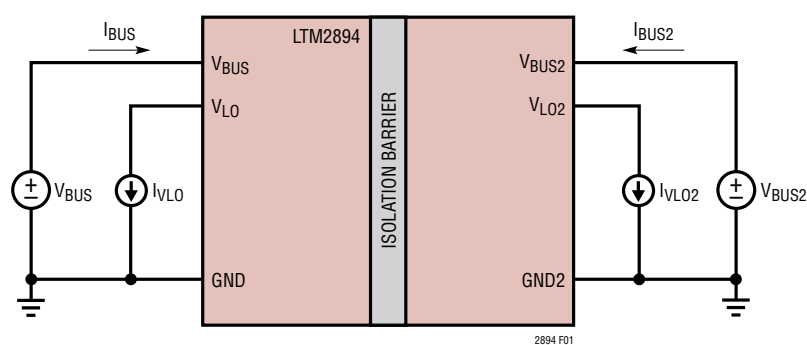


Figure 1. Power Supply Loads



## TEST CIRCUITS

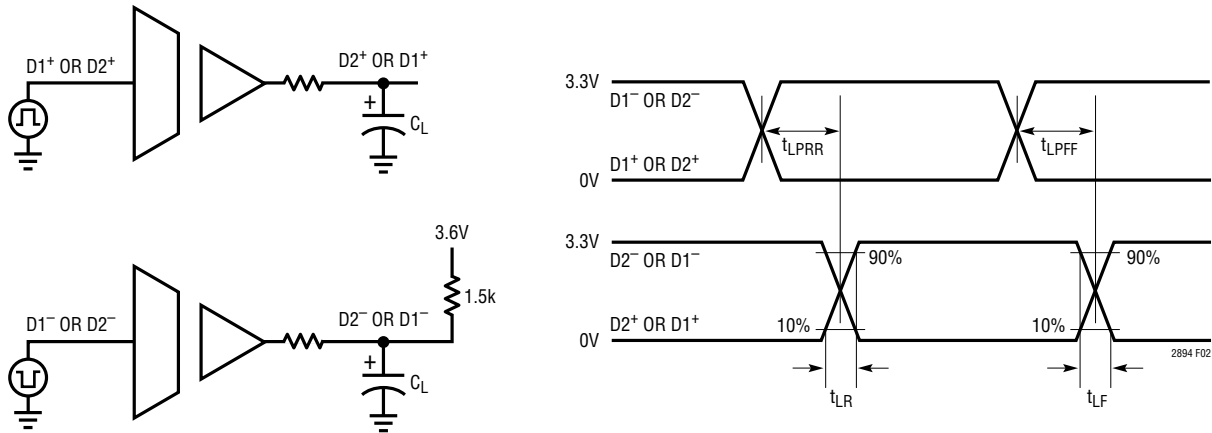


Figure 2. Low Speed Timing Measurements

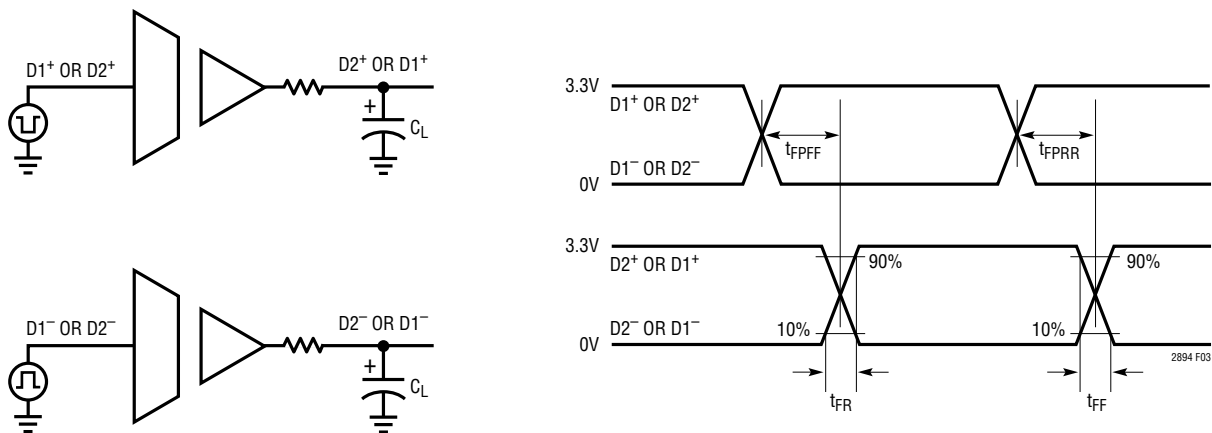


Figure 3. Full Speed Timing Measurements

## FUNCTIONAL TABLE

USB Transceiver Functional Table

Mode	D1 <sup>+</sup>	D1 <sup>-</sup>	Pull-Up Connection	D2 <sup>+</sup>	D2 <sup>-</sup>
Full Speed (Idle)	1.5k $\Omega$ Pull-Up	Host Pull-Down	D1 <sup>+</sup>	Peripheral Pull-Up	15k $\Omega$ Pull-Down
Low Speed (Idle)	Host Pull-Down	1.5k $\Omega$ Pull-Up	D1 <sup>-</sup>	15k $\Omega$ Pull-Down	Peripheral Pull-Up
Disconnected (Idle)	Host Pull-Down	Host Pull-Down	None	15k $\Omega$ Pull-Down	15k $\Omega$ Pull-Down
Suspend (Idle > 3ms)	Set During Idle Time	Set During Idle Time	Set During Idle Time	Peripheral or 15k $\Omega$	Peripheral or 15k $\Omega$
D1 to D2 data	IN <sup>+</sup>	IN <sup>-</sup>	Set During Idle Time	OUT <sup>+</sup>	OUT <sup>-</sup>
D2 to D1 data	OUT <sup>+</sup>	OUT <sup>-</sup>	Set During Idle Time	IN <sup>+</sup>	IN <sup>-</sup>

## OPERATION

The LTM2894  $\mu$ Module transceiver provides a galvanically isolated robust USB interface, complete with decoupling capacitors. An automatically configured pull up resistor is included to represent the condition of the isolated downstream USB bus to the upstream USB bus. The LTM2894 is ideal for use in USB connections where grounds between upstream hub/host and downstream devices can take on different voltages. Isolation in the LTM2894 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained though common mode events exceeding 50kV/ $\mu$ s providing excellent noise isolation.

The integrated USB transceiver on both sides of the isolation barrier supports full and low speed modes defined in the USB 2.0 Specification. The communication through the isolation barrier for USB is bidirectional and as such the LTM2894 determines data flow direction based on which side a start of packet (SOP) begins first. The direction of data is maintained until an end of packet (EOP) pattern is observed or a timeout occurs due to a lack of activity. The USB interface maintains a small consistent propagation delay representative of a single connection or hub delay and transfers all bus state and data information.

Pull-up resistors integrated in the upstream interface automatically indicate device connections and disconnections. A downstream device connection automatically selects the proper pull-up resistor at the upstream facing port after sensing the idle state of the downstream device at connection time. Disconnection of a downstream device automatically releases the pull-up resistor on the

upstream facing port allowing the upstream 15k pull-down resistors to pull the bus signals to a disconnect condition. This function makes the LTM2894 ideal for host, hub, bus splitter, or peripheral device integration.

### $\mu$ Module Technology

The LTM2894 utilizes isolator  $\mu$ Module technology to translate signals across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the  $\mu$ Module substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The  $\mu$ Module technology provides the means to combine the isolated signaling with our USB transceiver in one small package.

### USB Transceiver Pin Protection

The LTM2894 USB transceiver pins D1<sup>+</sup>, D1<sup>-</sup>, D2<sup>+</sup>, and D2<sup>-</sup> have protection from ESD and short-circuit faults. The transceiver pins withstand  $\pm 20$ KV HBM ESD events. Overcurrent circuitry on the transceiver pins monitor fault conditions from D1<sup>+</sup> and D1<sup>-</sup> to GND, V<sub>LO</sub>, or V<sub>BUS</sub> (5.3V MAX) and from D2<sup>+</sup> and D2<sup>-</sup> to GND2, V<sub>LO2</sub>, or V<sub>BUS2</sub> (5.3V MAX). A current detection circuit disables the transceiver pin if the pin sinks about 40mA for greater than 600ns. The V<sub>LO</sub> and V<sub>LO2</sub> output supplies protect the USB transceiver pins from shorts to GND or GND2 respectively with a 40mA current limit.

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## APPLICATIONS INFORMATION

### USB Connectivity

The LTM2894  $\mu$ Module transceiver connects directly to USB ports on the upstream side and the downstream side without the addition of external components. The transceiver passes through all data and does not act as a hub or intelligent device. The bus lines are monitored for idle conditions, start of packet, and end of packet conditions to properly maintain bus speed and data direction. The

series resistance, pull-up, and pull-down resistors are built into the LTM2894. The upstream facing USB port contains automatically configured 1.5k pull-up resistors which are switched in or out based on the downstream side peripheral device configuration. This implementation allows upstream reporting of the downstream bus speed and connection/disconnection conditions. Built-in 15k pull-down resistors are included from the D2<sup>+</sup> and D2<sup>-</sup> signals to GND2 supporting the downstream bus configuration.

## APPLICATIONS INFORMATION

Monitoring the USB data pins, the LTM2894 detects a K-state to begin a data packet and set the data direction. The data is monitored for an end of packet signature and a finishing J-state before the bus is released. The data payload between the K-state and J-state is transferred through the LTM2894 isolator with a delay of approximately 80ns.

### Idle State Communication

The LTM2894  $\mu$ Module transceiver maintains the conditions of the USB bus idle state by monitoring the downstream side bus idle condition and refreshing the state across the isolation barrier at a consistent rate. Furthermore, the LTM2894 monitors the speed of the downstream peripheral once connected and sets its own operation to match. Figure 4 shows the abbreviated circuitry of the automatic monitoring and reporting of the bus speeds. The D2<sup>+</sup> or D2<sup>-</sup> signals are monitored for a connection to pull-ups on D2<sup>+</sup> or D2<sup>-</sup> and the result is processed as full speed or low speed, otherwise disconnect. The idle state is communicated to the upstream side through a refresh transmission. The switches SW1 or SW2 are controlled based on the received information. SW1 is closed if D2<sup>+</sup> is detected to have a pull-up and D2<sup>-</sup> was open. SW2 is closed if D2<sup>-</sup> is detected to have a pull-up and D2<sup>+</sup> was open. Both SW1 and SW2 are opened if the downstream USB bus is disconnected. During a USB suspend, the pull-up resistor will maintain the condition prior to detecting the suspend command.

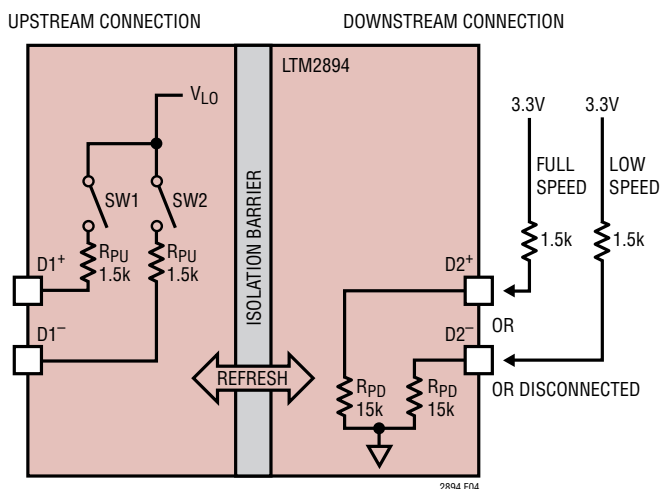


Figure 4. Idle State Automatic Resistor Setting

### Suspend Mode

When the upstream USB bus is idle for greater than 3ms the LTM2894 will enter suspend mode. Once the part enters suspend the  $V_{BUS}$  supply current reduces below 2mA.

The LTM2894 wakes up from suspend due to disconnects, reconnects, and downstream initiated resume signaling when the LTM2894 is in a hub, host, or peripheral device. The upstream transceiver maintains observation and reports downstream transceiver disconnects and reconnects. Recovery from suspend mode occurs when a data state change is detected and may take up to 10 $\mu$ s.

During suspend mode, DC current drawn from  $V_{LO}$  into external circuits will be supplied from  $V_{BUS}$  and may exceed the limits set in the USB specification.

$V_{BUS2}$  current does not reduce in suspend mode.

### $V_{LO}$ and $V_{LO2}$ Supplies

The  $V_{LO}$  and  $V_{LO2}$  output supply pins are available for use as a low current 3.3V supply on both sides of the isolation barrier. They also serve as supplies for the USB interface circuitry. An internal linear regulator maintains 3.3 volts on  $V_{LO}$  from the  $V_{BUS}$  input supply. A separate linear regulator maintains 3.3V on  $V_{LO2}$  from  $V_{BUS2}$ . The current is limited to 10mA for external applications. Exceeding this limit may cause degradation in the  $V_{LO}$  or  $V_{LO2}$  supplies and undesirable operation from the USB isolator. Connection of signals ON to  $V_{LO}$  or ON2 to  $V_{LO2}$  will not cause a significant change in the available current. These supplies are available to support interface logic to the isolated USB port. In order to meet the suspend mode current limit, minimize the DC current of external applications on the  $V_{LO}$  output supply.  $V_{LO}$  and  $V_{LO2}$  are protected from over current and over temperature conditions.

### Supply Current

Loading on the multiple output supply pins of the LTM2894 affect the supply current consumption on  $V_{BUS}$ . The  $V_{BUS}$  input supplies current to the upstream side of the transceiver and to the  $V_{LO}$  pin. The  $V_{BUS2}$  input supplies power to the downstream side of the transceiver and to the  $V_{LO2}$  pin.

## APPLICATIONS INFORMATION

### Supply Current Equations (Typical)

Operating:

$$I_{BUS} = 6\text{mA} + I_{VLO}$$

$$I_{BUS2} = 6\text{mA} + I_{VLO2}$$

Suspend:

$$I_{BUSSPND} = 1.5\text{mA} + I_{VLO}$$

$$I_{BUS2SPND} = 6\text{mA} + I_{VLO2}$$

Off:

$$I_{BUSPOFF} = 10\mu\text{A}$$

$$I_{BUS2POFF} = 10\mu\text{A}$$

### USB 2.0 Compatibility

The LTM2894  $\mu$ Module transceiver is compatible with the USB 2.0 specification of full and low speed operation. Some characteristics of the LTM2894  $\mu$ Module transceiver may not support full compliance with the USB 2.0 specification.

The propagation delay for full speed data of 80ns exceeds the specification for a single hub of 44ns plus the attached cable delay of 26ns. This results from driving the data signal to the 3.3V rail prior to a K-state transition to maintain balanced crossover voltages equivalent to the cross over voltages of the successive data transitions. USB ports commonly drive the idle state bus to the 3.3V rail prior to the K-state start of packet transition. Further, the LTM2894 does not re-time the data transitions, and will propagate the edges as received, with the potential to add additional jitter or pulse width distortion.

### Hot Plug Protection

The  $V_{BUS}$  and  $V_{BUS2}$  inputs are bypassed with low ESR ceramic capacitors. During a hot-plug event, the supply inputs can overshoot the supplied voltage due to cable inductance. When using external power supply sources greater than 24V that can be hot-plugged, add an additional 2.2 $\mu$ F tantalum capacitor with greater than 1 $\Omega$  of ESR, or a ceramic capacitor with a series 1 $\Omega$  resistor to the  $V_{BUS}$  or  $V_{BUS2}$  input to reduce the possibility of exceeding absolute maximum ratings. Refer to Application Note AN88, Ceramic Capacitors Can Cause Overvoltage Transients, for a detailed discussion of this problem.

### PC Board Layout

The high integration of the LTM2894 makes PCB layout simple. However, to optimize its electrical isolation characteristics, and EMI, some layout considerations are necessary. The PCB layout in Figure 5 is a recommended configuration for a low EMI USB application. The following considerations optimize the performance of the LTM2894.

- Do not place copper between the inner columns of pads on the top or bottom on the PCB. This area must remain open to withstand the rated isolation voltage and maintain the creepage distance.
- Route D1<sup>-</sup> and D1<sup>+</sup> and D2<sup>-</sup> and D2<sup>+</sup> as differential pairs with 90 $\Omega$  impedance, matching the USB cable impedance.

### RF, Magnetic Field Immunity

The isolator  $\mu$ Module technology used within the LTM2894 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 2.

**Table 2. Test Frequency Field Strength**

EN 61000-4-3, Annex D, 80MHz to 1GHz	10V/m
1.4MHz to 2GHz	3V/m
2GHz to 2.7GHz	1V/m
EN 61000-4-8, Level 4 50Hz and 60Hz	30A/m
EN 61000-4-8, Level 5 60Hz	100A/m*
EN 61000-4-9, Level 5 Pulse	1000A/m

\*Non-IEC Method

## APPLICATIONS INFORMATION

### EMI

Radiated emissions have been measured for the LTM2894 using a gigahertz transverse electromagnetic (GTEM) cell without a USB cable attached. The performance shown in

Figure 7 EMI Plot was achieved with the layout structure in Figure 6. Results are corrected per IEC 61000-4-20.

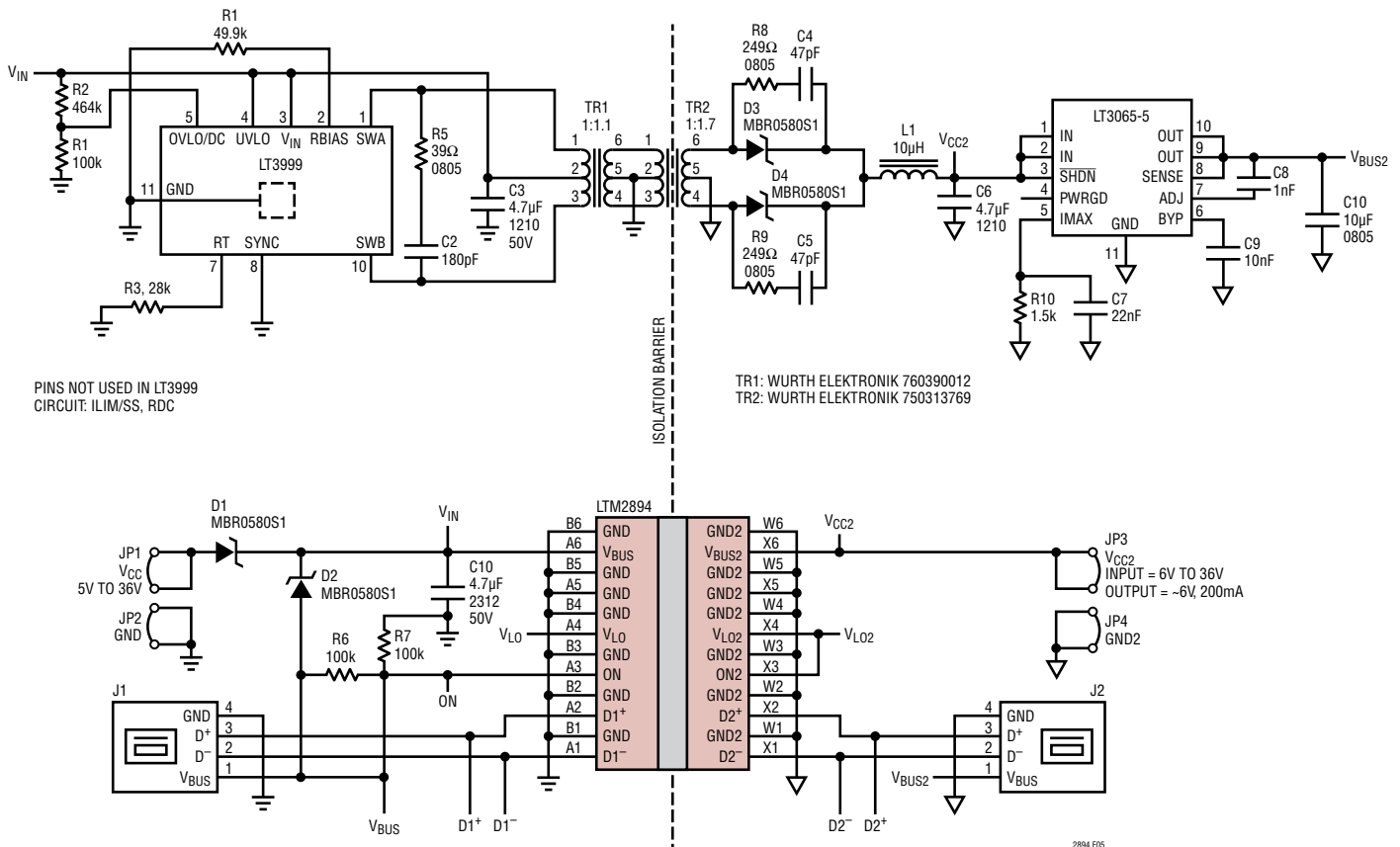


Figure 5. Low Noise, Low EMI, 5kV<sub>RMS</sub>, Reinforced USB Isolator Demo Circuit

APPLICATIONS INFORMATION

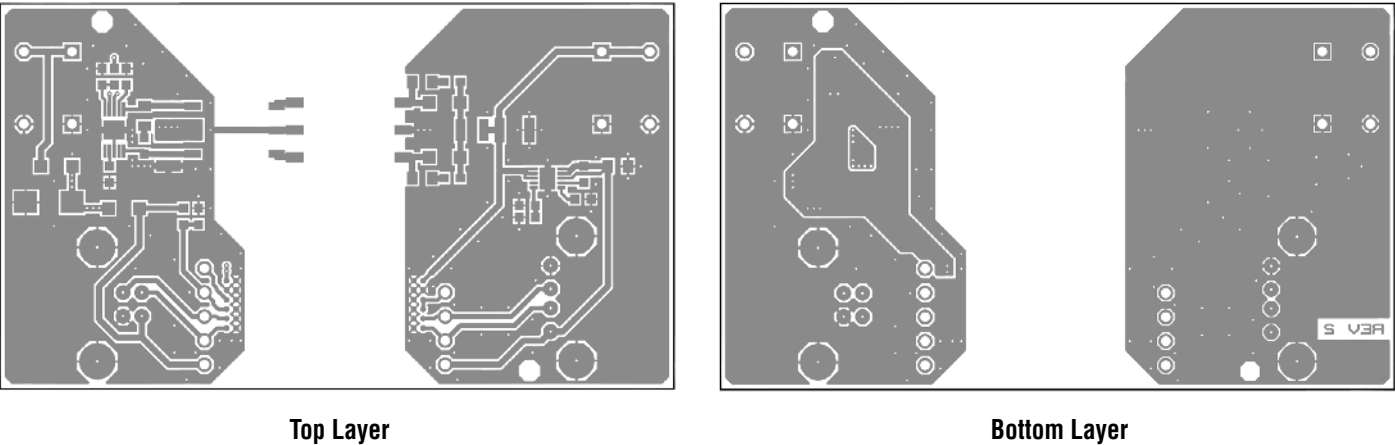


Figure 6. PC Board Layout

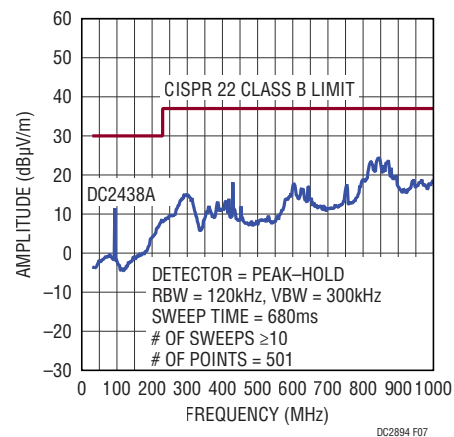


Figure 7. EMI Plot

TYPICAL APPLICATIONS

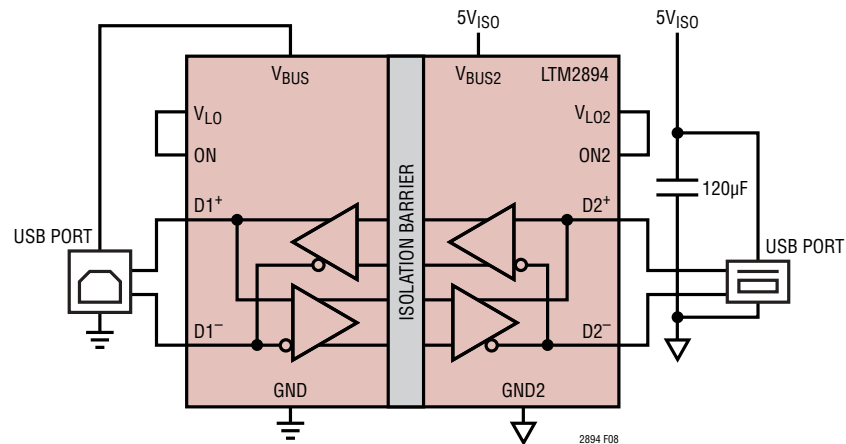


Figure 8. Bus Splitter

## TYPICAL APPLICATIONS

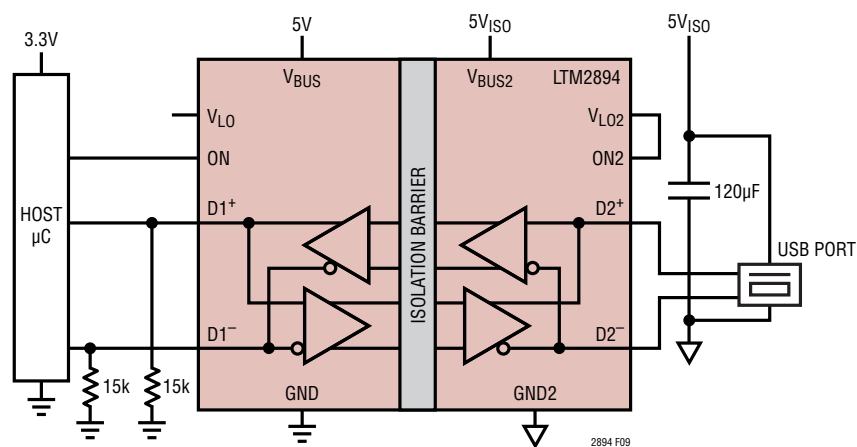


Figure 9. USB Host Integration

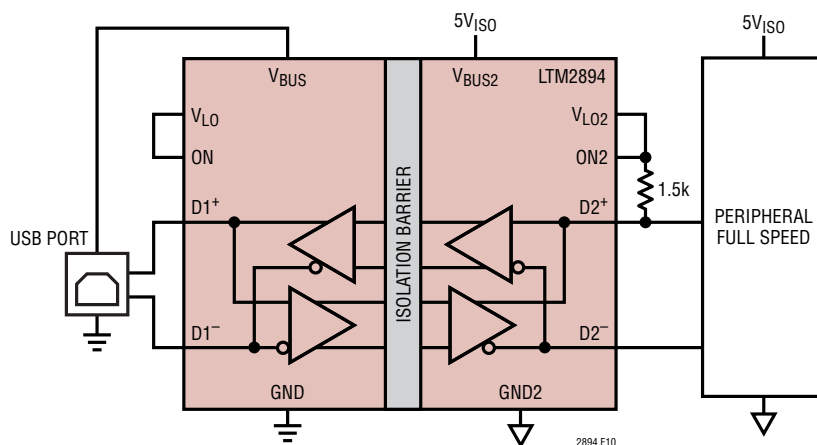


Figure 10. Powered Peripheral Device

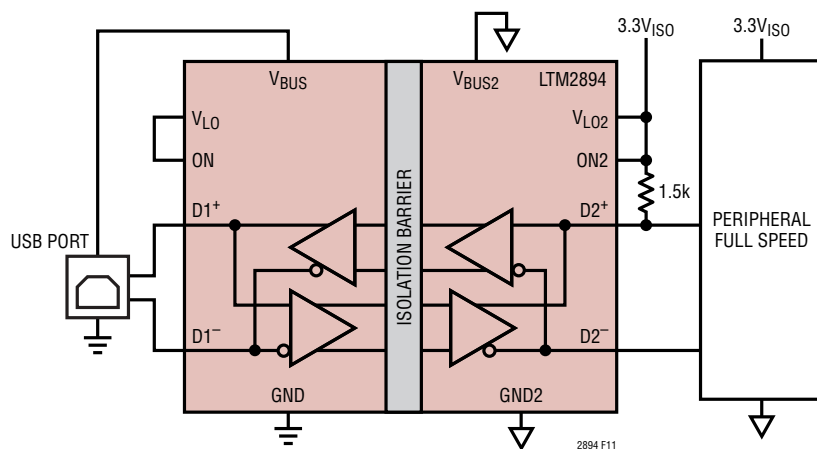
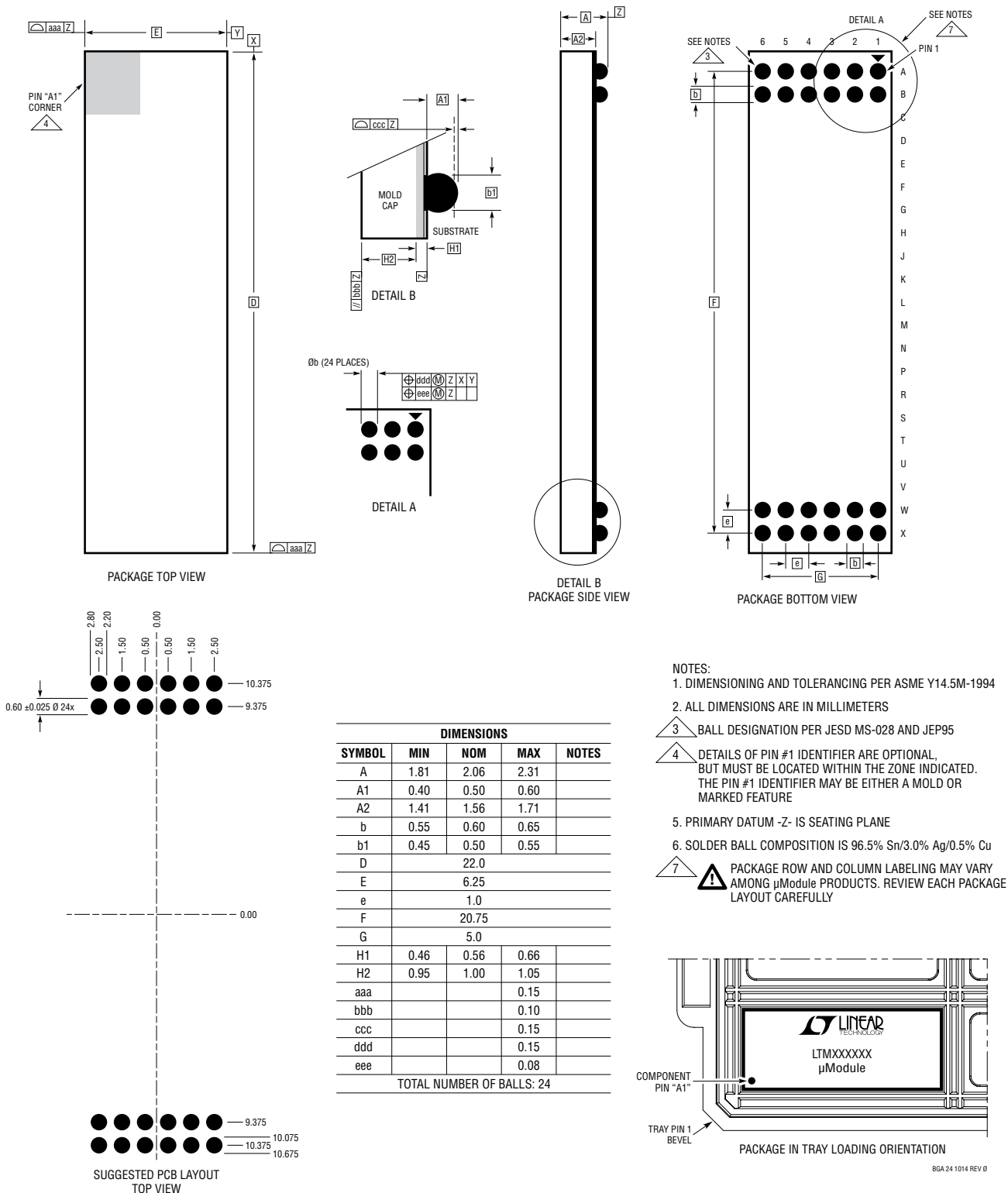


Figure 11. Peripheral Powered with 3.3V Only

PACKAGE DESCRIPTION

**BGA Package**  
**24-Lead (22mm × 6.25mm × 2.06mm)**  
(Reference LTC DWG# 05-08-1991 Rev 0)





## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/18	Added UL/CSA Certifications Increased Typical Creepage Distance	1, 5 5



## RELATED PARTS

Rev A