EN5330

3A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor

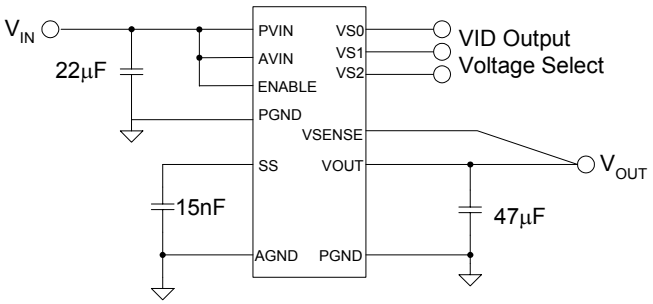
RoHS Compliant
July 2007

Description

The EN5330 is a Power System on a Chip DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires only three external components that include small value input and output ceramic capacitors and a soft-start capacitor.

The EN5330 significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

Typical Application Circuit



Typical application circuit.

Features

- Features Integrated Inductor Technology
- Small solution size; 1/3rd size of competitors
- Output matched to ≤ 90 nm silicon
- Low part count; only 3 external parts required
- Low output ripple; ≤ 20mV typical
- Package optimized for low EMI
- Up to 10W output power (at V_{OUT}=3.3V)
- High switching Frequency; 5MHz
- High Efficiency; greater than 90%
- Very fast transient response
- Wide input voltage range of 2.375V to 5.5V
- Digital voltage selector with options for common output voltages from 0.8V to 3.3V
- External resistor divider and OVP option for output voltages from 0.8V to V_{IN}-600mV
- Output enable pin and Power OK signal
- Programmable soft-start time
- Over-current protection
- Thermal shutdown, short circuit, output over-voltage and input under-voltage protection
- RoHS compliant, MSL3 rated to 260°C

Applications

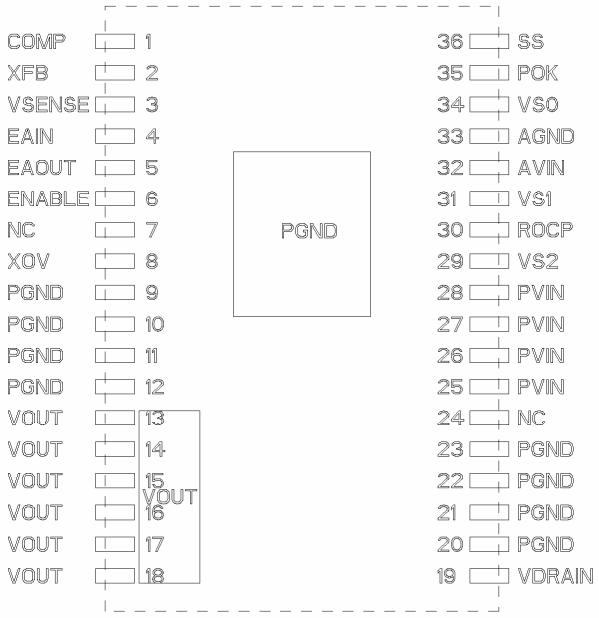
- Space constrained or noise and ripple sensitive applications
- Servers, workstations and PCs
- Broadband, networking, LAN/WAN, optical telecommunications equipment
- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs; ≤ 90 nm silicon
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails

Ordering Information

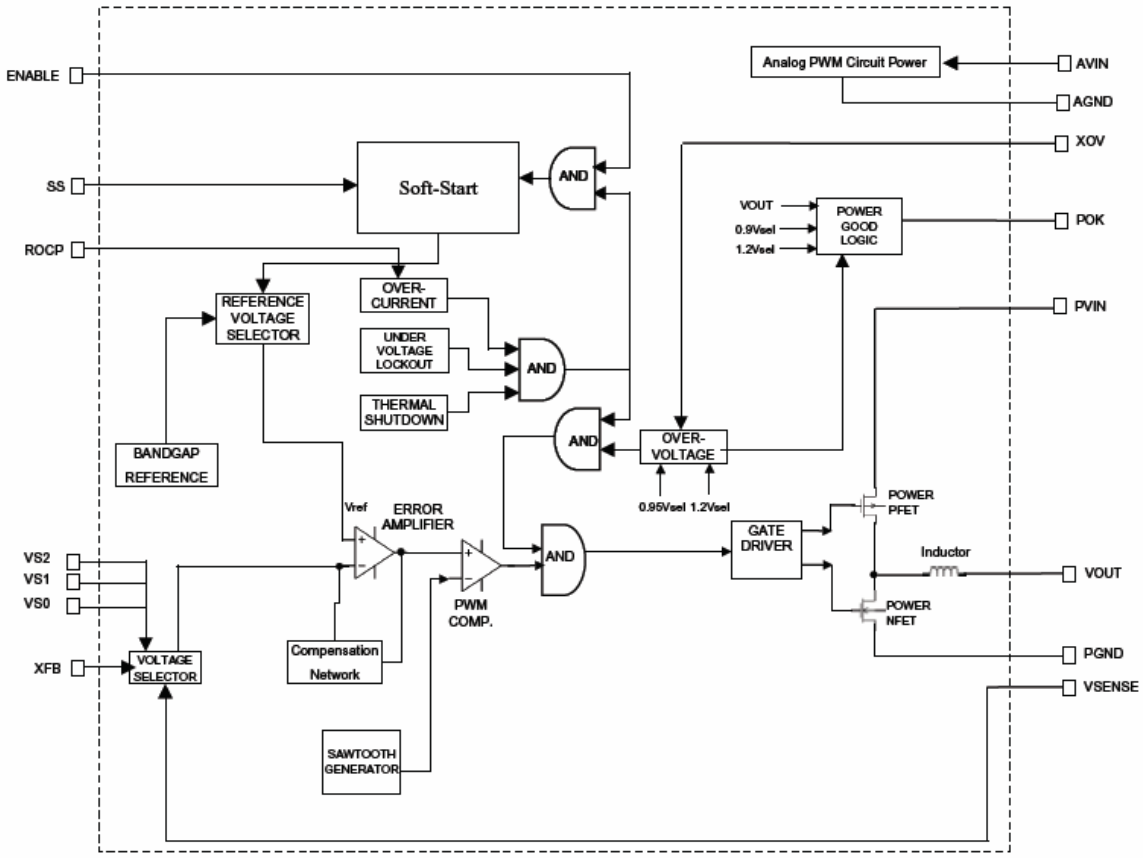
Part Number	Temp Rating (°C)	Package
EN5330DC-T	0 to 70	36-pin DFN T&R
EN5330DI-T	-40 to +85	36-pin DFN T&R
EN5330DC-E	DFN Evaluation Board	

Pin Configuration

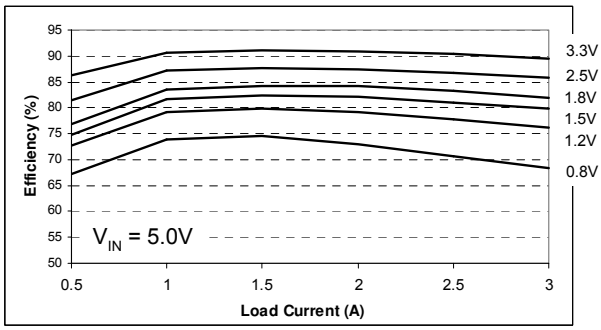
This diagram is a top-view of the component and represents the on-board layout requirements for the landing pads and thermal connection points. Specific dimensions for the pads are presented on page 10. Pin 1 of the device is signified by the white dot marked on the top of the device.



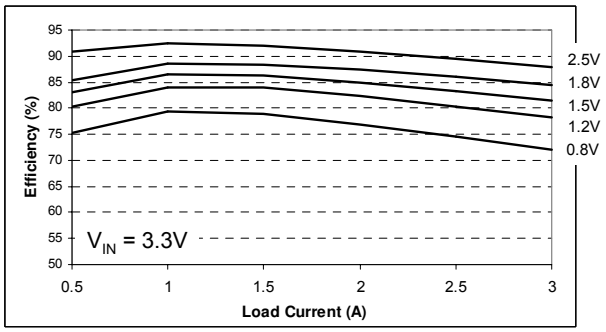
Block Diagram



Typical Efficiency

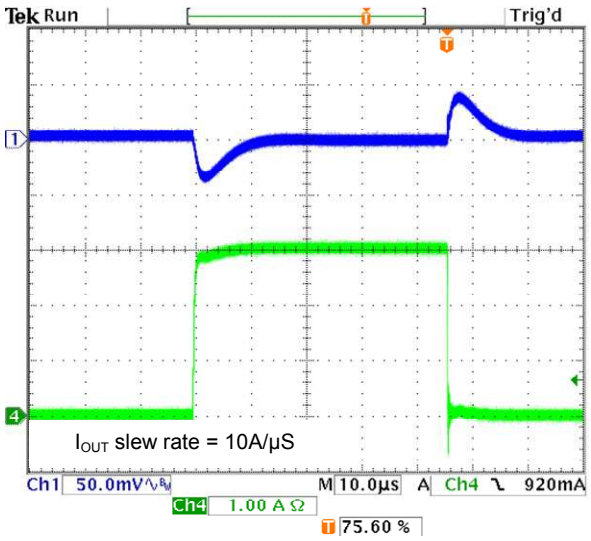


Efficiency versus load, V_{IN} = 5.0V; V_{OUT} = 0.8V – 3.3V.

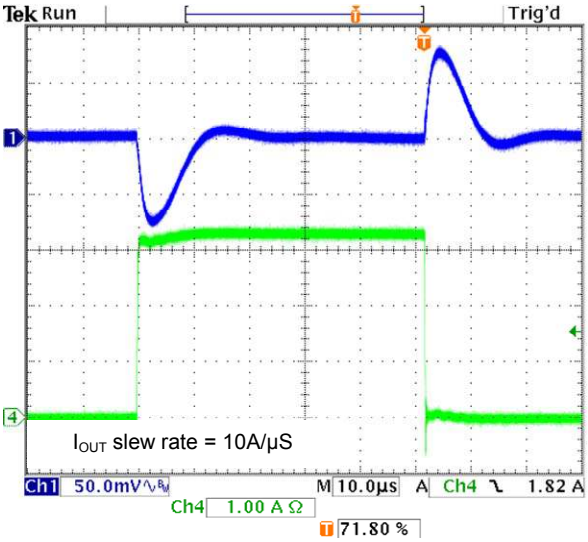


Efficiency versus load, V_{IN} = 3.3V; V_{OUT} = 0.8V – 2.5V.

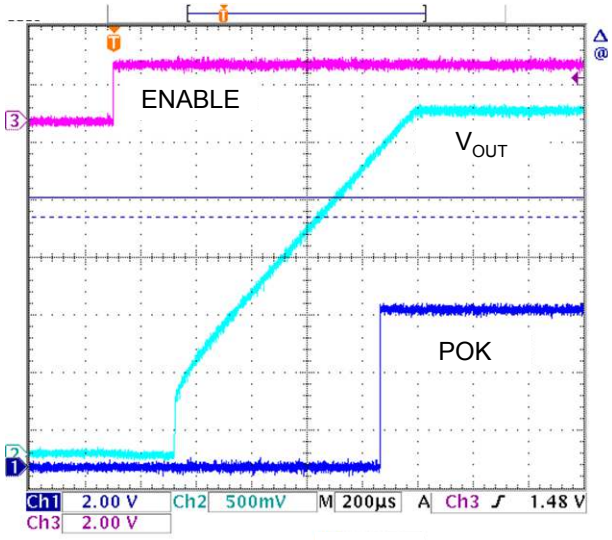
Waveforms



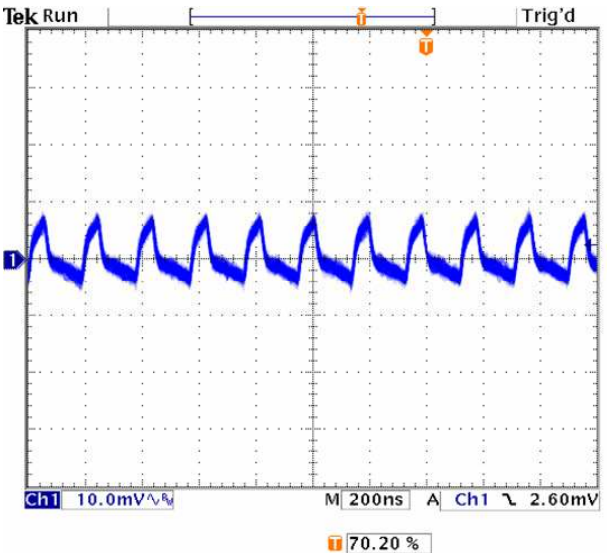
Load Transient, V_{IN} = 5.0V, V_{OUT} = 1.2V, 0 – 3A.



Load Transient, V_{IN} = 5.0V, V_{OUT} = 3.3V, 0 – 3A.



Start up waveform, ENABLE, V_{OUT}, POK Timing.



Output Voltage Ripple, V_{IN} = 5.0V, V_{OUT} = 1.2V.

Absolute Maximum Ratings

CAUTION: Stresses in excess of the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.5	6.5	V
Input Voltage – Enable		-0.5	V_{IN}	V
Input Voltage – VS0, VS1 & VS2 **(Note 1)**		-0.5	V_{IN}	V
Storage Temperature Range	T_{STG}	-65	150	°C
MSL per JEDEC J-STD-020A Level 3			260	°C
ESD Rating (based on Human Body Model)			2000	V

NOTES:

1. VS0, VS1 and VS2 pins have an internal pull-up resistor, only ground potentials should be placed on them as required.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.375	5.5	V
EN5330DC Operating Ambient Temperature	T_A	0	+70	°C
EN5330DI Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) **(Note 2)**	θ_{JA}	28	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	6	°C/W
Thermal Overload Trip Point	T_{J-TP}	+160	°C
Thermal Overload Trip Point Hysteresis		20	°C

NOTES:

2. Based on a four-layer board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

NOTE: V_{IN}=3.3V and over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.375		5.5	V
No-Load Operating Current	I_{NL}	V_{IN} = 3.6V, ENABLE= High; V_{OUT}=1.2V (Includes PWM, gate drive and inductor ripple current.)		42		mA
UVLO Threshold	V_{UVLO}	V_{IN} increasing V_{IN} decreasing		2.2 2.1		V
Switching Frequency	F_{OSC}			5		MHz
V_{OUT}						
Range	V_{OUT}	Using external voltage divider	0.8		V_{IN} – 600mV	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy	V_{OUT}	Over line, load, temperature	-2.0		2.0	%
Line Regulation	V_{OUT}	V_{IN} = 2.5 to 5.0 volts		3		mV
Load Regulation	V_{OUT}	I_{LOAD} = 0 to 3A		3		mV
Temperature Regulation	V_{OUT}	T_A= 0 to 70ºC		+0.25 -0.45		%
	V_{OUT}	T_A= -40 to 85ºC		+0.65 -0.55		%
Transient Response (I_{OUT} = 0% to 100% or 100% to 0% of Rated Load, Slew rate = 10A/µS)						
Peak Deviation	V_{OUT}	V_{IN} = 5V, 1.2V < V_{OUT} < 3.3V C_{OUT} = 47µF		3	5	%
Output Voltage Ripple						
Peak-to-peak	V_{OUT-PP}	V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 3A, C_{OUT} = 50uF, 5 x 10µF X5R or X7R ceramic capacitors		20		mV
Output Current (Note 3)						
Max Continuous Output Current	I_{OUT}				3	A
Over-Current Threshold	I_{OCP}			4.5		A
Short-Circuit Current	I_{SC}			4		A
Enable Operation						
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	Min voltage to ensure the converter is enabled	1.8			V
Enable Pin current	V_{ENABLE}	V_{IN} = 5.5V		50		µA
Voltage Select Pins (VS0, VS1, VS2)						
VSx Logic Low Threshold		(Pin internally pulled high)			0.8	V
VSx Logic High Threshold		(Pin internally pulled high)	1.8			V
VSx Pin Current		(V_{IN} = 5.5V) VSx = GND VSx = V_{IN} VSx = Open		50 0 0		µA
Power OK Operation						
POK low voltage	V_{POK}	I_{POK} = 4mA			0.4	V
Max POK Voltage	V_{POK}	Supply voltage applied to POK			V_{IN}	V

NOTES:

3. Maximum output current may need to be de-rated, based on operating condition, to meet T_J requirements.

Pin Descriptions

PIN	NAME	FUNCTION
1	COMP	Output of the buffer leading to the error amplifier. Used for external modifications of the compensation network.
2	XFB	External feedback voltage input. Option for programming the output voltage with a resistor divider on V_{OUT}.
3	VSENSE	Remote voltage sense input. Connect this pin to the load voltage at the point to be regulated.
4	EAIN	Input of the error amplifier for external modifications of the compensation network.
5	EAOUT	Output of the error amplifier for external modifications of the compensation network.
6	ENABLE	Enable input. An input high enables operation. An input low disables operation.
7	NC	NO CONNECT – Do not electrically connect this pin to PCB. **See Note 4.**
8	XOV	Over-Voltage set-point input. When using an external voltage divider and the XFB pin. When VS0, VS1 and VS2 are left OPEN or pulled high, an additional voltage divider separate from the XFB pin is required to set the OVP set-point. In this mode, the OVP function is disabled if this voltage divider is not present.
9	PGND	Power ground for the power stage circuits.
10		
11		
12		
13	VOUT	Voltage and power output.
14		
15		
16		
17		
18		
19	VDRAIN	Test point between the power FETs and Inductor.
20	PGND	Power ground for the power stage circuits.
21		
22		
23		
24	NC	NO CONNECT – Do not electrically connect this pin to PCB. **See Note 4.**
25	PVIN	Power voltage input for the power stage circuits.
26		
27		
28		
29	VS2	Voltage select line 2 input. See Table 1.
30	ROCP	Over-Current trip point adjust input. Used for adjusting the OCP trip point.
31	VS1	Voltage select line 1 input. See Table 1.
32	AVIN	Analog voltage input for the controller circuits.
33	AGND	Analog ground for the controller circuits.
34	VS0	Voltage select line 0 input. See Table 1.
35	POK	Power OK is an open drain transistor for power system state indication.
36	SS	Soft-Start node. A capacitor is connected between this pin and AGND.

NOTES:

4. This pin is used for engineering test purposes and reserved for future use. Solder, but do not electrically connect this pin to the PCB.

Theory of Operation

Synchronous Buck Converter

The EN5330 is a synchronous, pin programmable power supply with integrated power MOSFET switches and inductor. The nominal input voltage range is 2.5V-5.0V. The output can be set to common voltages by connecting appropriate combinations of 3 voltage selection pins to ground. If different voltage levels are required, provision is also made to allow external programming. The feedback control loop is voltage-mode and the part uses a low-noise PWM topology. Up to 3A of output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size output capacitors.

The power supply also has protection features such as:

- Programmable over-current protection (to protect the IC from excessive load current)
- Thermal shutdown (to protect the converter from getting too hot)
- Over-voltage protection that stops the PWM switching and turns on the lower N-MOSFET at 120% of the programmed output voltage in order to protect the load from an OV condition.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up.
- Power good circuit indicating whether the output voltage is within 90%-120% of the programmed voltage.

Output Voltage Programming

The EN5330 output voltage is programmed using one of two methods. Common output voltages are achieved by tying one or more of the three Voltage Select pins (VS0, VS1 & VS2) to ground (see Table 1). If all three are left floating, the output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOV pins respectively. These voltages should be set by way of resistor dividers between V_{OUT} to AGND with the midpoint going to XFB and XOV (See Figure 1).

It is recommended that Rb1 and Rb2 resistor values be ~2kΩ. Use the following equation to set the resistor Ra1 for the desired output voltage:

$$Ra1 = \frac{(Vout - 0.8V) * Rb1}{0.8V}$$

If over-voltage protection is desired, use the following equation to set the resistor Ra2 for the desired OVP trip-point:

$$Ra2 = \frac{(OVPtrip - 0.96V) * Rb2}{0.96V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.

Figure 1: External output voltage and OVP setting

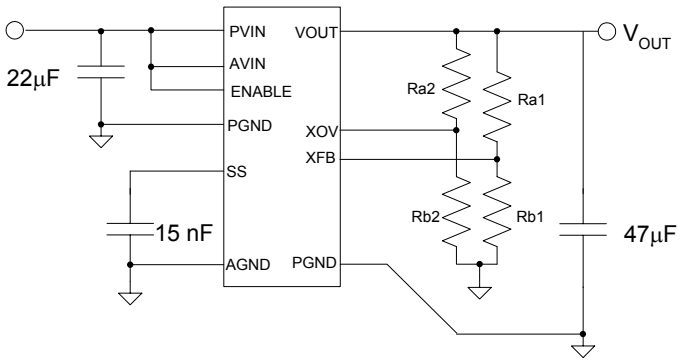


Table 1: Output Voltage Select Table

VS2*	VS1*	VS0*	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V**
1	1	1	User Selectable

** 0.8V ref only, not guaranteed performance

*NOTE The VS0, VS1 and VS2 pins are defaulted to a '1' with an internal pull-up resistor. Only connect these pins to AGND if a '0' is required. If a '1' is required, then leave the pin floating.

Capacitor Selection

The EN5330 needs about 20-40uF of input capacitance. Low-cost, low-ESR ceramic capacitors must be used as input capacitors for this converter and it is required that they be rated X5R or X7R. In some applications, lower value capacitors are needed in parallel with the larger, lossy capacitors in order to provide high frequency decoupling.

The EN5330 has been optimized for use with about 50µF of ceramic output capacitance. It is required that these be low-cost, low-ESR, ceramic capacitors rated X5R or X7R. (See the Enpirion application note on ripple comparison for optimum selection of number and value of these capacitors based on ripple requirements.) In order to eliminate high-frequency switching spikes on the output ripple, usually a low-value, low-ESR ceramic capacitor is used in parallel with the larger capacitors right at the load.

Enable Operation

The ENABLE pin provides a means to shut down the power FET switching or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

Soft-Start Operation

The SS pin in conjunction with a small capacitor between this pin and AGND provides the soft start function to limit the in-rush current during start-up. During start-up of the converter the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA. This capacitor begins to charge when ENAB LE and AVIN cross their turn-on thresholds. The typical soft-start time for the output to reach regulation voltage from when C_{ss} begins to charge is given by:

$$t_{SS} = C_{SS} * 0.080$$

Where the soft-start time t_{SS} is in ms and the soft-start capacitance C_{SS} is in nF. Typically, a capacitor around 15 nF is recommended.

During the soft-start cycle, when the soft-start capacitor reaches 0.8V, the output has reached its programmed regulation range. Note that the soft-start current source will continue to operate and during normal operation, the soft-start capacitor will charge up to a final value of 2.5V.

Power Up Sequencing

The sequencing of AVIN, PVIN and ENABLE should meet the following requirements:

1. ENABLE should not be asserted before PVIN.
2. PVIN should not be applied before AVIN.

Note that tying AVIN, PVIN and ENABLE together and brought up at the same time does meet these requirements.

POK Operation

The POK signal is an open drain signal indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-

voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also Over Voltage Protection).

Over-Current Protection

The cycle-by-cycle current limit function is achieved by sensing the current flowing through the sense P-MOSFET and a signal generated by a differential amplifier with a preset over-current threshold. During a particular cycle, if the over-current threshold is exceeded, the power P-MOSFET and N-MOSFET are turned off. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. If the over-current condition persists, the converter will eventually go through a full soft-start cycle. This circuit is designed to provide high noise immunity.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state. If the condition persists, the device will go through a soft-start cycle.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 160ºC. Once the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Low Input Voltage Operation

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the operation of the converter is controlled and predictable. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5330 is internally compensated through the use of a type 3 compensation network and is optimized for use with about 50µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on required capacitor types.) In some cases modifications to the compensation may be required. For more information, contact Enpirion Applications Engineering support.

Layout Considerations

The EN5330 Layout Guidelines application note provides more details on specific layout recommendations for this part. The following are general layout guidelines to consider.

The CMOS chip inside the EN5330 has two grounds: AGND for the controller, and PGND for the power stage. These two grounds need to be connected outside the package at one point through a low-impedance trace. The connection should be made such that the impedance between the connection point and the AGND pad on the package is minimized. Since the internal voltage sensing circuit is based on AGND, the connection of the two grounds should also be made such that the best voltage regulation can be achieved. The soft-start capacitor, the voltage programming resistors, and any other external control component should be tied to AGND.

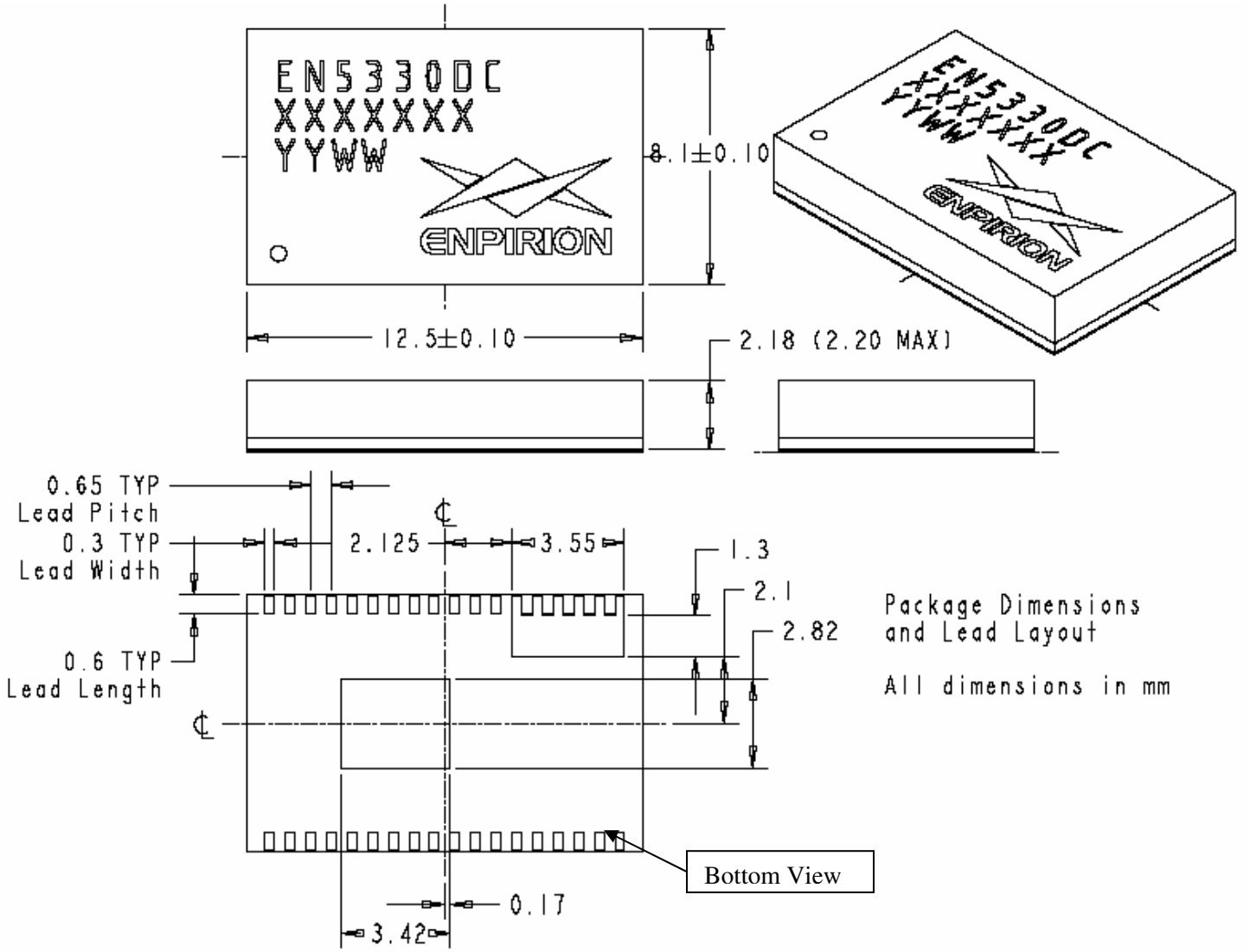
The placement of the input decoupling capacitors between PVIN and PGND is very critical. These components should be placed such that they have the lowest inductance traces to PVIN and PGND.

There are two thermal pads underneath the device. The centrally located pad is PGND, and, depending on the number of layers of the PC board, it needs to be connected to a thermal plane in order to conduct heat away from the device. Note that if any of the thermal planes is also connected to AGND, the impedance

between this point and the GND connection of the load needs to be minimized in order to get the best possible load regulation. The pad opposite the V_{OUT} pins is connected to V_{OUT}. This V_{OUT} pad should be connected to a top layer copper area as large as possible to conduct more heat away from the package. This will also help minimize the trace length to the output filter caps.

Pin 19 is a connected to a noisy internal node and is brought out for test purposes only. Keep all sensitive signal traces as far as possible from this pin. Ideally, on the top layer there should be no traces or vias underneath the package between this pin and the V_{OUT} thermal pad.

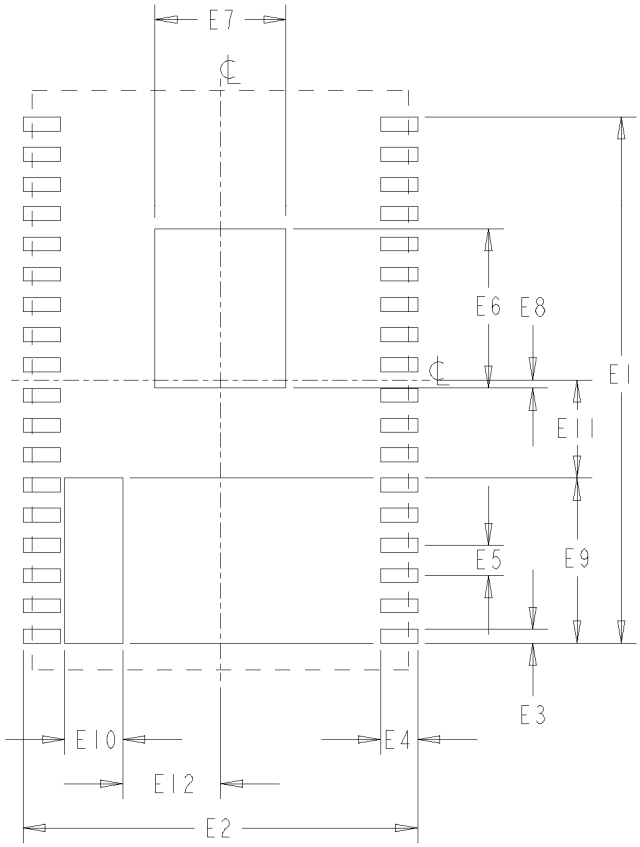
Mechanical Drawing and Nominal Dimensions



Landing Pad Information

The Enpirion DFN package is footprint compatible with the JEDEC standard 36-pin TSSOP package code DD. The reference document and board layout diagram appear below.

NOTE: JEDEC Solid State Technology Association TSSOP (Plastic Thin Shrink Small Outline Package) standardized package code DD. This TSSOP standard package is defined in the JEDEC document MO-153, Issue F, dated 05/01, which defines 57 variations on package size, lead pitch, and lead count.



	Dimension (mm)
E1	11.35 ± 0.05
E2	8.50 ± 0.05
E3	0.30 ± 0.05
E4	0.80 ± 0.05
E5	0.65 ± 0.05
E6	3.42 ± 0.05
E7	2.82 ± 0.05
E8	0.17 ± 0.05
E9	3.55 ± 0.05
E10	1.25 ± 0.05
E11	2.13 ± 0.05
E12	2.10 ± 0.05

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