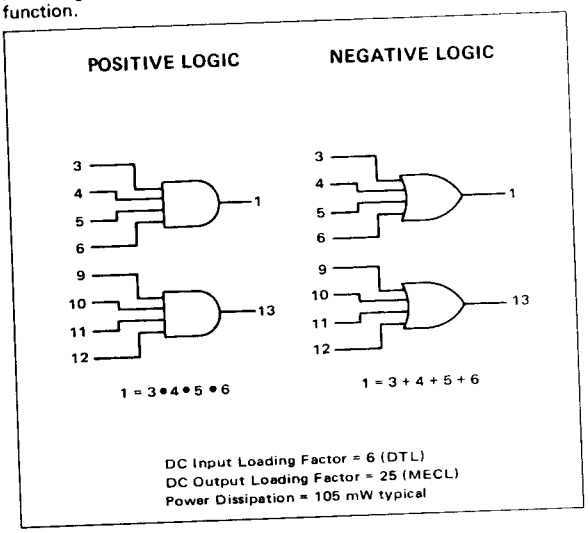
SATURATED LOGIC-TO-MECL DUAL TRANSLATORS

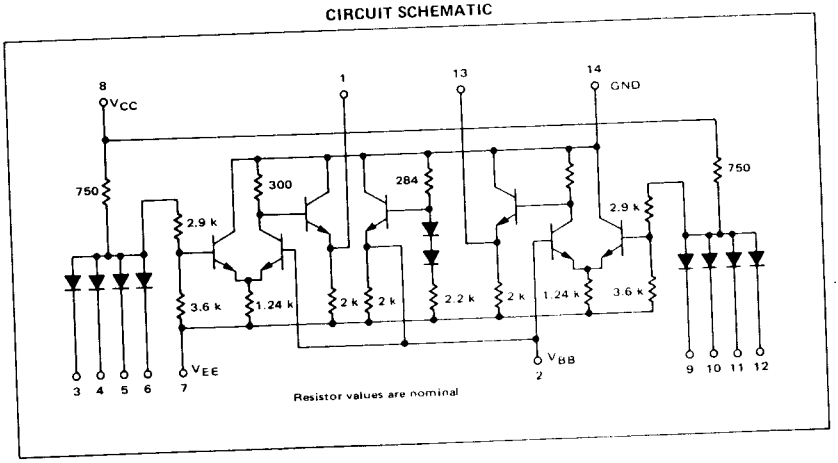
MC1017
MC1217

A dual level translator for converting saturated logic levels to MECL signal levels. The translator provides the positive logic AND function.

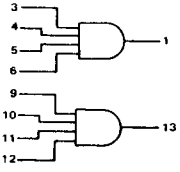


DC Input Loading Factor = 6 (DTL)
DC Output Loading Factor = 25 (MECL)
Power Dissipation = 105 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal



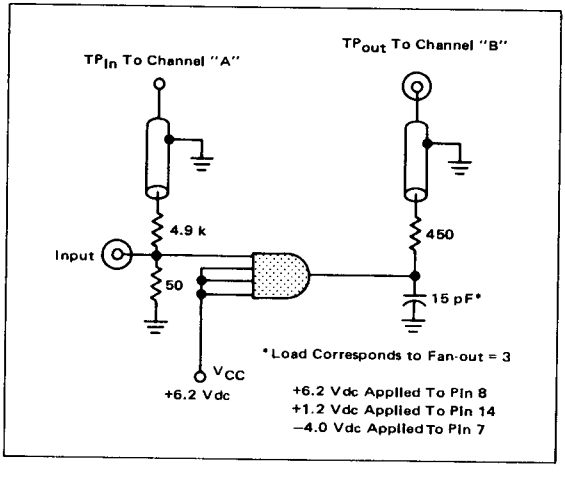
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one translator.
The other translator is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1217 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1017 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Positive Supply Drain Current	I_C	8	-	-	-	4.0	-	-	mAdc	-	-	-	4.0	-	-	mAdc
Negative Supply Drain Current	I_E	7	-	-	-	24	-	-	mAdc	-	-	-	24	-	-	mAdc
Input Diode Reverse Current	I_R	3 4 5 6	- - - -	- - - -	- - - -	0.2 ↓ ↓ ↓	- - - -	2.0 ↓ ↓ ↓	μAdc	- - - -	- - - -	- - - -	0.2 ↓ ↓ ↓	- - - -	2.0 ↓ ↓ ↓	μAdc
Input Diode Forward Current	I_F	3 4 5 6	- - - -	- - - -	- - - -	2.0 ↓ ↓ ↓	- - - -	- - - -	mAdc	- - - -	- - - -	- - - -	2.0 ↓ ↓ ↓	- - - -	- - - -	mAdc
"OR" Logical "1" Output Voltage	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	1 1 1 1	-1.890 ↓ ↓ ↓	-1.580 ↓ ↓ ↓	-1.800 ↓ ↓ ↓	-1.500 ↓ ↓ ↓	-1.720 ↓ ↓ ↓	-1.380 ↓ ↓ ↓	Vdc	-1.830 ↓ ↓ ↓	-1.525 ↓ ↓ ↓	-1.800 ↓ ↓ ↓	-1.500 ↓ ↓ ↓	-1.760 ↓ ↓ ↓	-1.435 ↓ ↓ ↓	Vdc
Bias Driver Output Voltage†	V_{BB}†	2	-1.35	-1.20	-1.26	-1.10	-1.11	-0.98	Vdc	-1.28	-1.14	-1.26	-1.10	-1.19	-1.04	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{3+1-}	1	17	22	15	20	13	18	ns	16	21	15	20	14	19	ns
	t_{3-1-}		13	18	15	20	19	25		14	19	15	20	17	22	
Rise Time	t_{1+}		7.0	10	7.0	10	8.0	12		7.0	10	7.0	10	7.0	11	
Fall Time	t_{1-}	↓	7.0	10	7.0	10	8.0	12	↓	7.0	10	7.0	10	7.0	11	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).
† V_{BB} limits apply from no load (0 mA) to full load (-1.0 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



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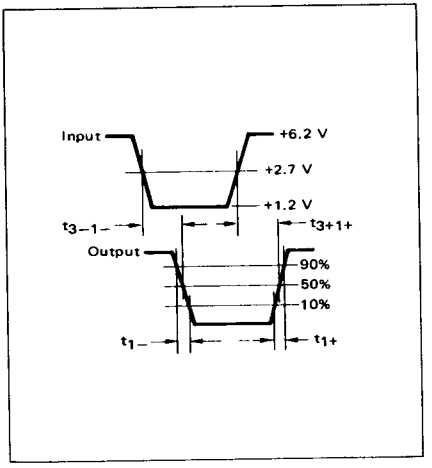
	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	mAdc I_L
MC1217	−55°C	2.1	0.5				
	+25°C	2.0	1.0	8.0			
	+125°C	2.0	0.7	8.0			
MC1017	0°C	2.0	0.85				
	+25°C	1.9	1.00	8.0			
	+75°C	1.8	0.85	8.0			

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	I_L	V_{CC} (Gnd)
Positive Supply Drain Current	I_C	8	-	-	-	8	7		14
Negative Supply Drain Current	I_E	7	-	-	-	8	7		14
Input Diode Reverse Current	I_R	3	-	-	3	-	-	-	4, 5, 6, 14
		4	-	-	4	-	-	-	3, 5, 6, 14
		5	-	-	5	-	-	-	3, 4, 6, 14
		6	-	-	6	-	-	-	3, 4, 5, 14
Input Diode Forward Current	I_F	3	-	-	-	8	7	-	4, 14
		4	-	-	-	↓	↓	-	3, 14
		5	-	-	-			-	6, 14
		6	-	-	-			-	5, 14
"OR" Logical "1" Output Voltage	V_{OH}†	1	3, 4, 5, 6	-	-	8	7	1	14
"OR" Logical "0" Output Voltage	V_{OL}	1	-	3	-	8	7	-	14
		1	-	4	-	↓	↓	-	↑
		1	-	5	-			-	
		1	-	6	-			-	
Bias Driver Output Voltage‡	V_{BB}†	2	-	-	-	8	7	2†	14
Switching Times			Pulse In	Pulse Out		(+6.2 V)	(−4.0 V)		(+1.2 V) 14
Propagation Delay	t_{3+1+}	1	1	3	-	8	7	-	
	t_{3-1-}		↓	↓	-	↓	↓	-	
Rise Time	t_{1+}				-			-	↑
Fall Time	t_{1-}	↓			-			-	



SWITCHING TIME WAVEFORMS