



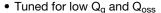
N-Channel 45 V (D-S) MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	45					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00120					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00180					
Q _g typ. (nC)	50.5					
I _D (A) ^a	208					
Configuration	Single					

FEATURES

- TrenchFET® Gen IV power MOSFET
- 45 V Drain-source break-down voltage



• 100 % R_a and UIS tested

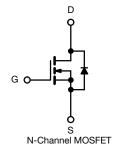
 Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- · Synchronous rectification
- High power density DC/DC
- · Motor drive control



ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR608DP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	45	V	
Gate-source voltage		V_{GS}	+20, -16	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		208		
	T _C = 70 °C	l , [166		
	T _A = 25 °C	I _D	51 ^{b, c}		
	T _A = 70 °C		40.8 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{DM}	400	A	
Continuous source-drain diode current	T _C = 25 °C		94.5		
	T _A = 25 °C	I _S	5.6 ^{b, c}		
Single pulse avalanche current		I _{AS}	50		
Single pulse avalanche Energy L = 0.1 mH		E _{AS}	125	mJ	
Maximum power dissipation	T _C = 25 °C		104	W	
	T _C = 70 °C		66.6		
	T _A = 25 °C	P _D	6.25 ^{b, c}		
	T _A = 70 °C		4 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) d, e		Ĭ	260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b, f	t ≤ 10 s	R _{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	0.9	1.2	C/VV

Notes

- a. Based on T_C = 25 $^{\circ}C$
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 54 °C/W
- g. Package limited

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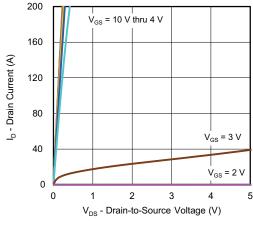
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	<u> </u>					
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	45	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	29	-	1400
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-5.8	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.1	-	2.3	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20, -16 \text{ V}$	-	-	± 100	nA
Zama anto college ducino coment	I _{DSS}	V _{DS} = 45 V, V _{GS} = 0 V	-	-	1	μΑ
Zero gate voltage drain current		V _{DS} = 45 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50	-	-	Α
Duning	Б	V _{GS} = 10 V, I _D = 20 A	-	0.00100	0.00120	
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	0.00136	0.00180	Ω
Forward transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	120	-	S
Dynamic ^b						
Input capacitance	C _{iss}		-	8900	-	
Output capacitance	C _{oss}	V 00 V V 0 V (4 MI)	-	1244	-	pF
Reverse transfer capacitance	C _{rss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	120	-	
C _{rss} /C _{iss} ratio			-	0.0135	0.0270	-
		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	111	167	
Total gate charge	Qg		-	50.5	76	
Gate-source charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	26	-	nC
Gate-drain charge	Q _{gd}		-	7.8	-	
Output charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V	-	59	-	
Gate resistance	R_g	f = 1 MHz	0.3	0.88	1.5	Ω
Turn-on delay time	t _{d(on)}		-	19	38	
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_L = 1 \Omega$	-	10	20	
Turn-off delay time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	50	100	
Fall time	t _f		-	8	16	
Turn-on delay time	t _{d(on)}		-	52	104	ns
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_L = 1 \Omega$	-	86	172	
Turn-off delay time	t _{d(off)}	$I_D\cong 20$ A, $V_{GEN}=4.5$ V, $R_g=1$ Ω	-	50	100	
Fall time	t _f		-	25	50	
Drain-Source Body Diode Characteristic	s					
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	94.5	
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	400	Α
Body diode voltage	V _{SD}	I _S = 10 A	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}		-	52	104	ns
Body diode reverse recovery charge	Q _{rr}	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	71	142	nC
Reverse recovery fall time	ta	$T_J = 25 ^{\circ}C$	-	32	-	
Reverse recovery rise time	t _b		-	20	-	ns

Notes

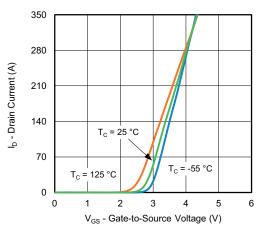
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

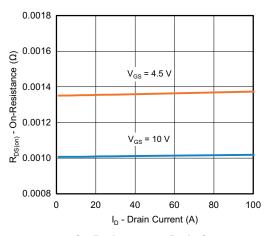




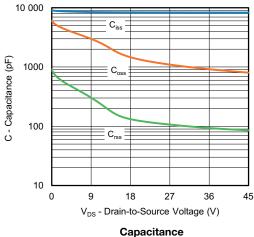
Output Characteristics



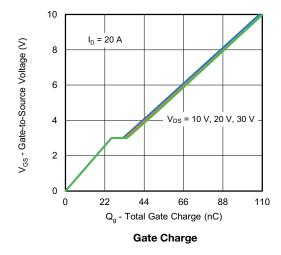
Transfer Characteristics

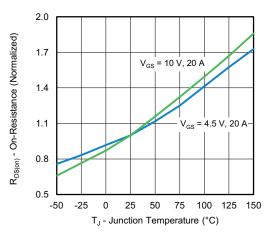


On-Resistance vs. Drain Current



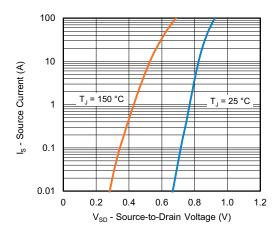
Capacitance



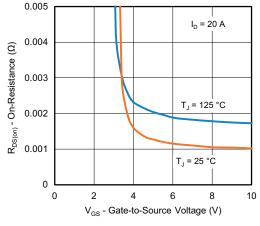


On-Resistance vs. Junction Temperature

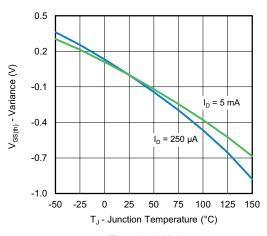




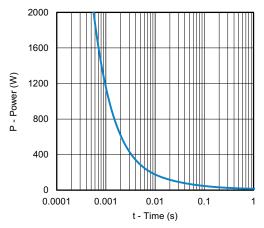
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

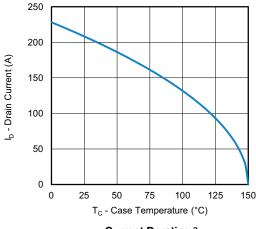


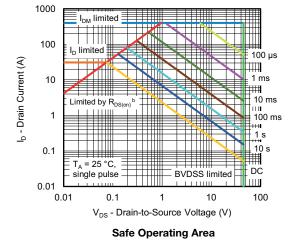
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

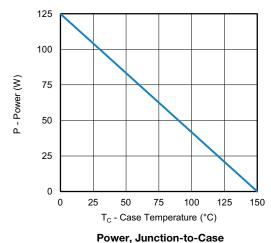


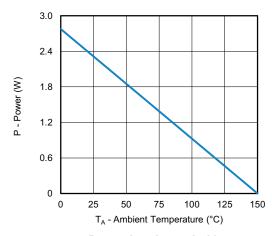










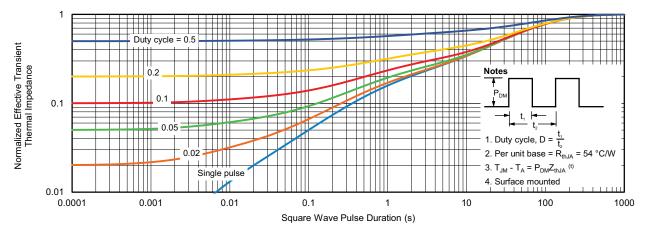


Power, Junction-to-Ambient

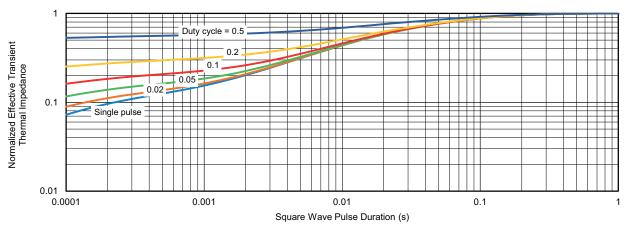
Notes

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.
- b. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified





Normalized Thermal Transient Impedance, Junction-to-Ambient



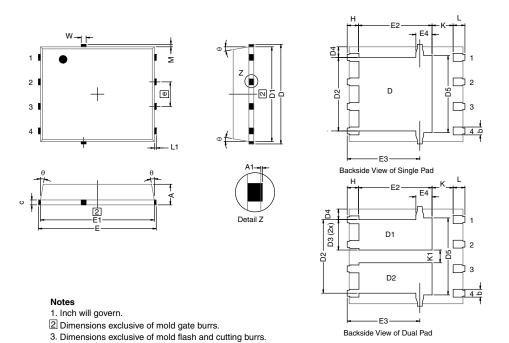
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76807.



DWG: 5881

PowerPAK® SO-8, (Single/Dual)

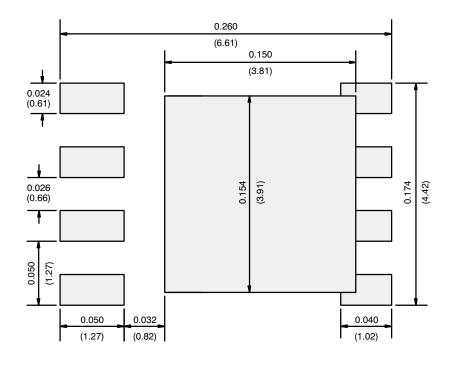


DIM.		MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX		
Α	0.97	1.04	1.12	0.038	0.041	0.044		
A1		-	0.05	0	-	0.002		
b	0.33	0.41	0.51	0.013	0.016	0.020		
С	0.23	0.28	0.33	0.009	0.011	0.013		
D	5.05	5.15	5.26	0.199	0.203	0.20		
D1	4.80	4.90	5.00	0.189	0.193	0.19		
D2	3.56	3.76	3.91	0.140	0.148	0.154		
D3	1.32	1.50	1.68	0.052	0.059	0.066		
D4		0.57 typ.			0.0225 typ.			
D5		3.98 typ.			0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	5.79	5.89	5.99	0.228	0.232	0.236		
E2	3.48	3.66	3.84	0.137	0.144	0.15		
E3	3.68	3.78	3.91	0.145	0.149	0.154		
E4		0.75 typ.			0.030 typ.			
е		1.27 BSC		0.050 BSC				
K		1.27 typ.		0.050 typ.				
K1	0.56	-	=	0.022	=	=		
Н	0.51	0.61	0.71	0.020	0.024	0.028		
L	0.51	0.61	0.71	0.020	0.024	0.028		
L1	0.06	0.13	0.20	0.002	0.005	0.008		
θ	0°	-	12°	0°	-	12°		
W	0.15	0.25	0.36	0.006	0.010	0.014		
М		0.125 typ.			0.005 typ.			

Revison: 13-Feb-17 1 Document Number: 71655



RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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