BLA9H0912L(S)-700; BLA9H0912L(S)-700G Power LDMOS transistor Rev. 1 – 24 May 2019

AMPLEON Product data sheet

Product profile 1.

1.1 General description

700 W LDMOS power transistor for avionics applications in the frequency range from 960 MHz to 1215 MHz.

Typical information Table 1.

Typical RF performance at T_{case} = 25 °C; t_p = 50 μ s; δ = 2 %; I_{Da} = 100 mA; in a class-AB demo circuit.

Test signal	f	V _{DS}	PL	G _p	ησ
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	1030	50	700	20	62

1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Designed for avionics band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

Avionics transmitter applications in the frequency range from 960 MHz to 1215 MHz

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Power LDMOS transistor

2. Pinning information

Table 2. Pir	nning		
Pin	Description	Simplified outline	Graphic symbol
BLA9H0912L	-700 (SOT502A)		
1	drain		
2	gate		1 1
3	source [1]		
			3 sym112
BLA9H0912L	S-700 (SOT502B)		
1	drain		
2	gate		1 1
3	source [1]		
			3 sym112
BLA9H0912L	-700G (SOT502F)		
1	drain		
2	gate		
3	source [1]		
		2	- • 3 sym112
BLA9H0912L	S-700G (SOT502E)		
1	drain		
2	gate		
3	source [1]		
			sym112

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BLA9H0912L-700	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A		
BLA9H0912LS-700	-	earless flanged ceramic package; 2 leads	SOT502B		
BLA9H0912L-700G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F		
BLA9H0912LS-700G	-	earless flanged ceramic package; 2 leads	SOT502E		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage			-	106	V
V _{GS}	gate-source voltage			-6	+11	V
T _{stg}	storage temperature			-65	+150	°C
Tj	junction temperature		<u>[1]</u>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
Z _{th(j-c)}	transient thermal impedance from junction	T _{case} = 85 °C; P _L = 700 W		
	to case	t _p = 32 μs; δ = 2 %	0.055	K/W
		t _p = 10 μs; δ = 10 %	0.068	K/W
		t _p = 64 μs; δ = 1 %	0.076	K/W
		t _p = 2.4 ms; δ = 6.4 %	0.24	K/W

6. Characteristics

Table 6. DC characteristics

$T_i = 25 \ ^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 4 mA	106	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 400 mA	1.5	2.0	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	2.8	μA
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 V;$ $V_{DS} = 10 V$	-	60	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	280	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 400 mA	-	3.7	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I _D = 14 A	-	0.060	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; f = 1030 MHz; t_p = 50 μ s; δ = 2 %; RF performance at V_{DS} = 50 V; I_{Dg} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
G _p	power gain	P _L = 700 W	19	20	-	dB
η _D	drain efficiency	P _L = 700 W	59	62	-	%
RL _{in}	input return loss	P _L = 700 W	-	-15	-	dB
P _{droop(pulse)}	pulse droop power	P _L = 700 W	-	0.2	0.5	dB
P _{L(2dB)}	output power at 2 dB gain compression		-	725	-	W

7. Test information

7.1 Ruggedness in class-AB operation

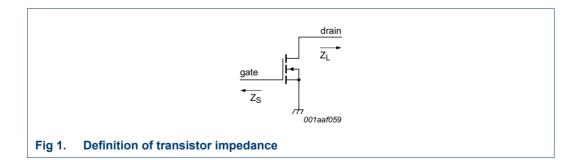
The BLA9H0912L-700, BLA9H0912LS-700, BLA9H0912L-700G and BLA9H0912LS-700G are capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dg} = 100 mA; P_L = 700 W; t_p = 50 µs; δ = 2 %.

7.2 Impedance information

Table 8. Typical impedance

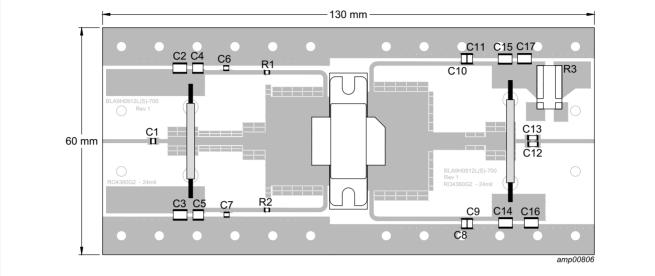
Typical values unless otherwise specified.

• ·	1	
f	Z _S	ZL
(MHz)	(Ω)	(Ω)
950	0.717 – j1.793	0.965 – j1.305
1000	0.953 – j1.886	1.049 – j1.561
1050	1.091 – j1.910	1.032 – j1.780
1100	1.353 – j0.443	1.291 – j1.952
1150	1.962 – j1.061	1.474 – j2.081
1200	0.837 – j0.936	1.514 – j2.413



Power LDMOS transistor

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4360G2; thickness = 0.61 mm; ε_r = 6.15; thickness copper plating = 35 μ m. See Table 9 for a list of components.

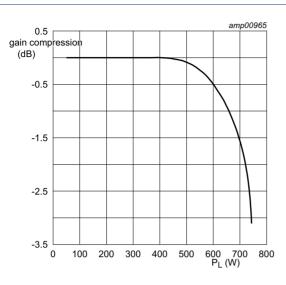
Fig 2. Component layout for class-AB production test circuit

Table 9.Demo test circuit list of componentsSee Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	62 pF	ATC 100A
C2, C3, C16, C17	multilayer ceramic chip capacitor	4.7 μF, 100 V	GMR42 258K7S 475K 100 H53
C4, C5, C14, C15	multilayer ceramic chip capacitor	1 nF	ATC 100B
C6, C7	multilayer ceramic chip capacitor	200 pF	ATC 800B
C8, C9, C10, C11, C12, C13	multilayer ceramic chip capacitor	68 pF	ATC 800B
R1, R2	resistor	5.1 kΩ	SMD 0603
R3	resistor	10 mΩ	FC4L110R010FER

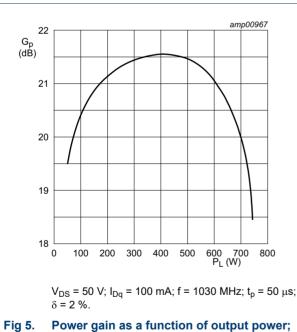
Power LDMOS transistor

amp00966

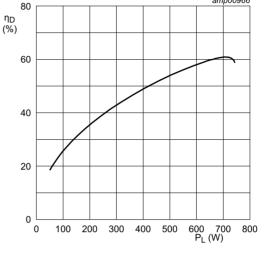


7.4 Graphical data

 V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 $\mu s;$ δ = 2 %.







 V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 $\mu s;$ δ = 2 %.

Fig 4. Drain efficiency as a function of output power; typical values

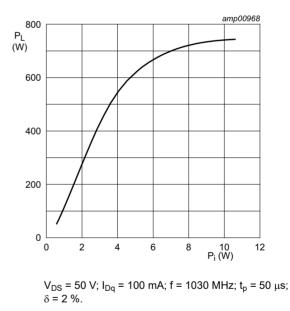


Fig 6. Output power as a function of input power; typical values

typical values

Power LDMOS transistor

8. Package outline

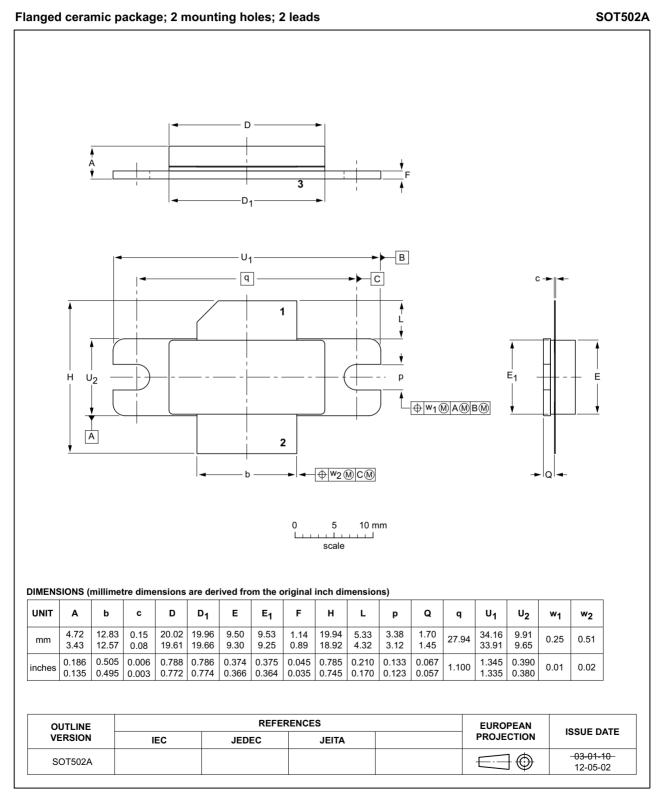


Fig 7. Package outline SOT502A

Power LDMOS transistor

SOT502B

Earless flanged ceramic package; 2 leads

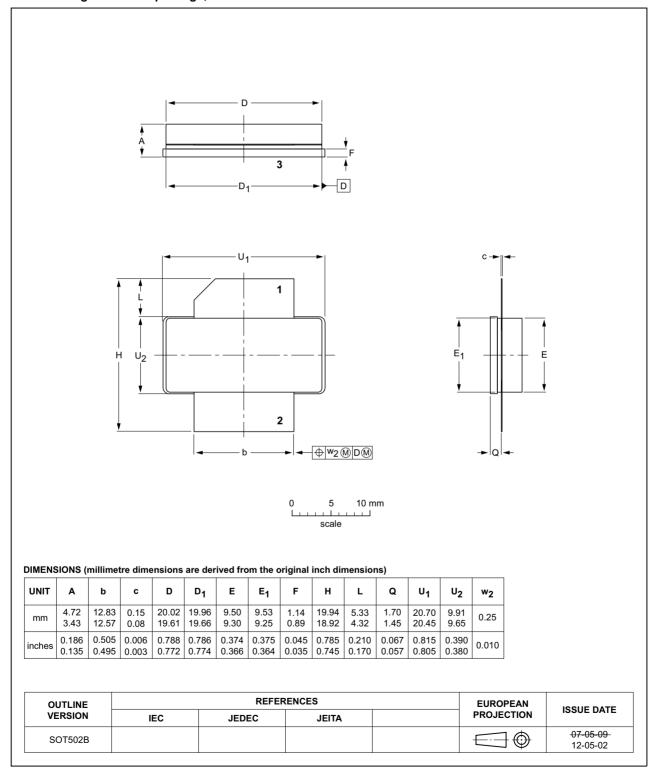


Fig 8. Package outline SOT502B

Power LDMOS transistor

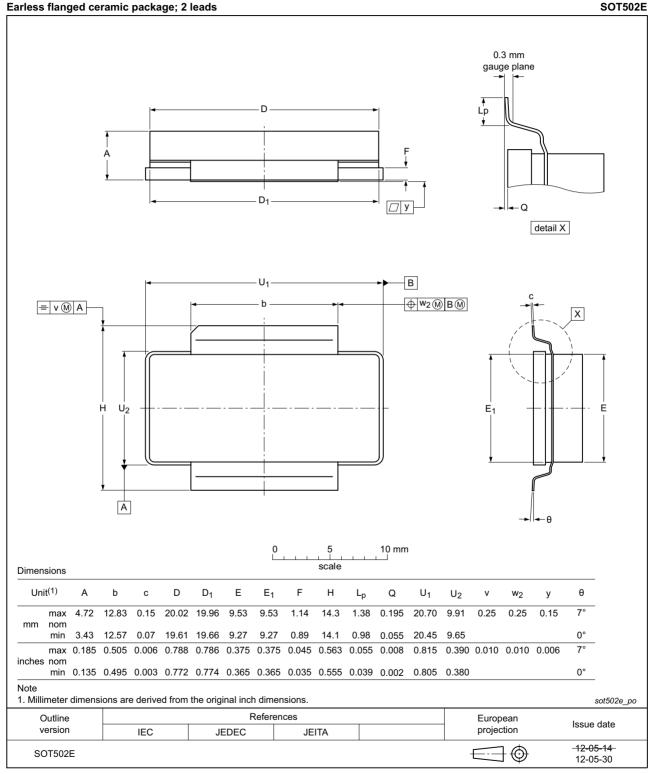


Fig 9. Package outline SOT502E

Power LDMOS transistor

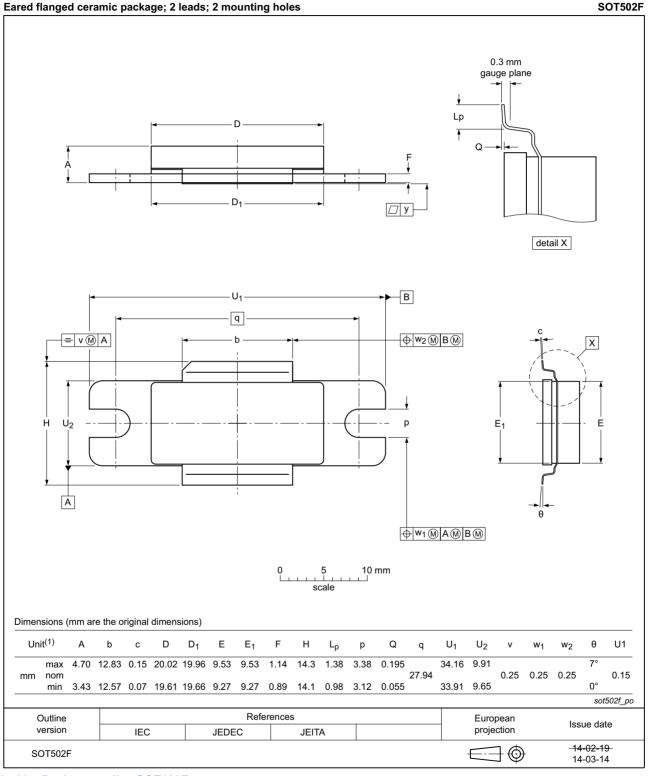


Fig 10. Package outline SOT502F

BLA9H0912L-700_LS-700_L-700G_LS-700G

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 10.ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations			
Acronym	Description		
ESD	ElectroStatic Discharge		
LDMOS	Laterally Diffused Metal-Oxide Semiconductor		
MTF	Median Time to Failure		
RoHS	Restriction of Hazardous Substances		
SMD	Surface Mounted Device		
VSWR	Voltage Standing-Wave Ratio		

11. Revision history

Table 12.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9H0912L-700_LS-700_L-700G_LS-700G v.1	20190524	Product data sheet		-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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