Product Specifications

Customer	**Standard**
Description	**4.2” E-PAPER DISPLAY**
Model Name	**4.2inch e-Paper (B)**
Date	**2020/11/01**
Revision	**1.0**

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Table of Contents

Version	Content	Date	Producer
1.0	New release	2020/11/01	

1. General Description

1.1 Overview

This display is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The4.2” active area contains400×300 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

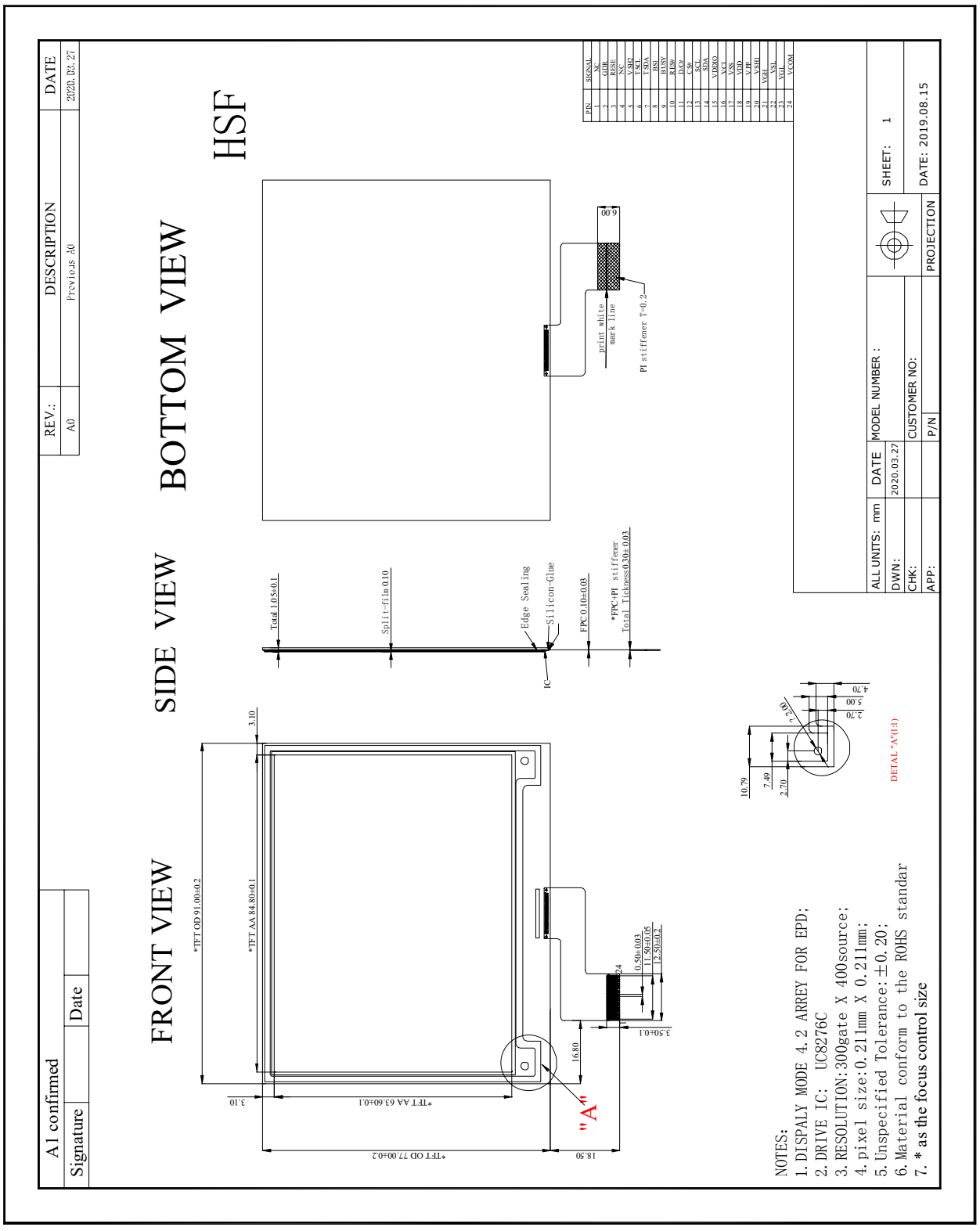
1.2 Features

- 400×300 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor12C / built-in temperature sensor

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:119
Active Area	84.8(H)×63.6 (V)	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91.00(H)× 77.00(V) × 1.25(D)	mm	
Weight	15±0.2	g	

1.4 Mechanical Drawing of EPD module



1.5 Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VDHR	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS	Bus selection pin	Note 1.5-5
9	BUSY_N	Busy state output pin	Note 1.5-4
10	RST_N	Reset	Note 1.5-3
11	DC	Data /Command control pin	Note 1.5-2
12	CSB	Chip Select input pin	Note 1.5-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	GND	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VDH(VSH)	Positive source driver Voltage	
21	VGH	Positive Gate driving voltage	
22	VDL(VSL)	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 1.5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 1.5-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

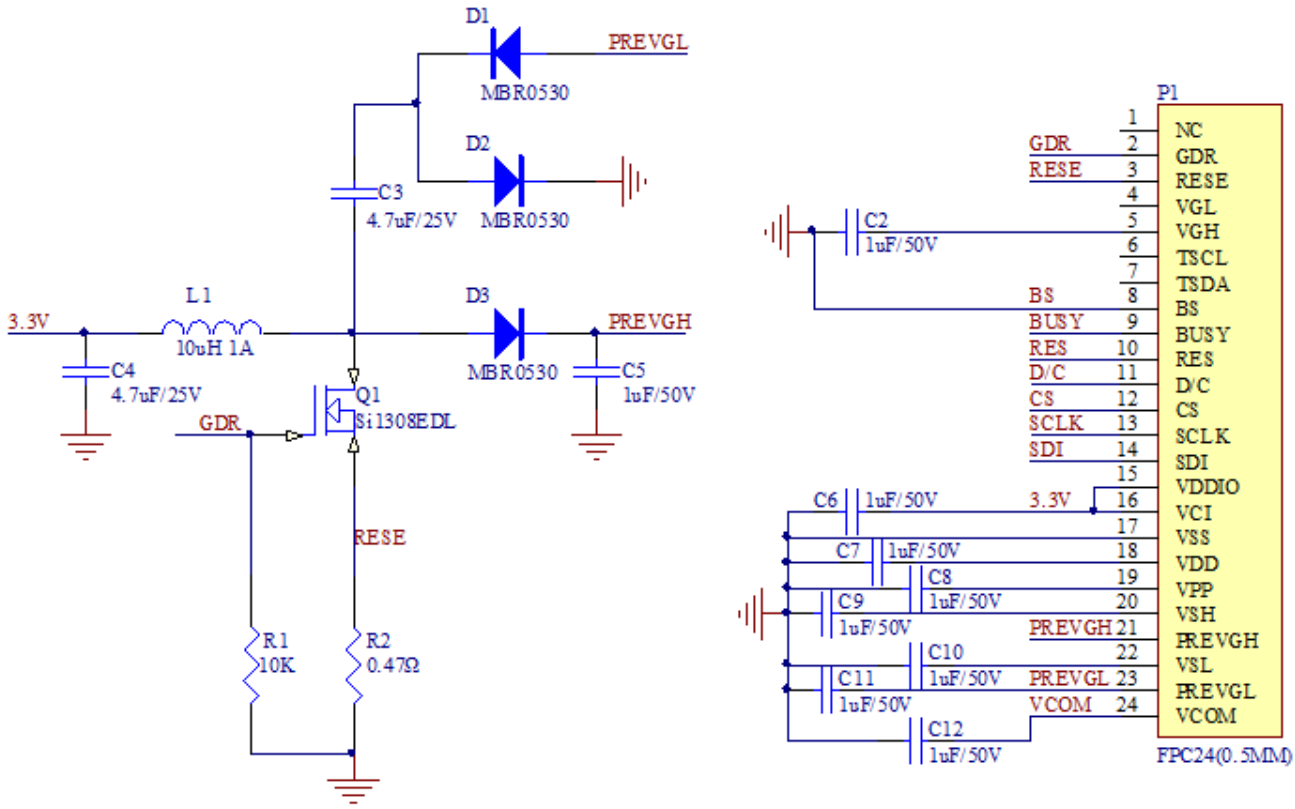
Note 1.5-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 1.5-4: This pin (BUSY_N) is Busy state output pin. When Busy_N is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy_N pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.

1.6 Reference Circuit



2. Environmental

2.1 HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged.

Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions	
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.	
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.	
(3) You should adopt radiation structure to satisfy the temperature specification.	
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.	
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)	
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.	
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=50℃，RH=30%RH，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=70℃ RH=40%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=40℃，RH=90%RH，For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 480Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃(30min)~70℃(30min)，50 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before temperature test.

Note2: Stay white pattern for storage and non-operation test.

3. ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM RATINGS

Table 3.1-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.3 to +6.0	V
T_{OPR}	Operation temperature range	0 to 40	°C
T_{STG}	Storage temperature range	-25 to 60	°C
-	Humidity range	40~70	%RH

Note1: Avoid direct sunlight.

Note2: Tstg is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 30℃~60℃.

3.2 DC CHARACTERISTICS

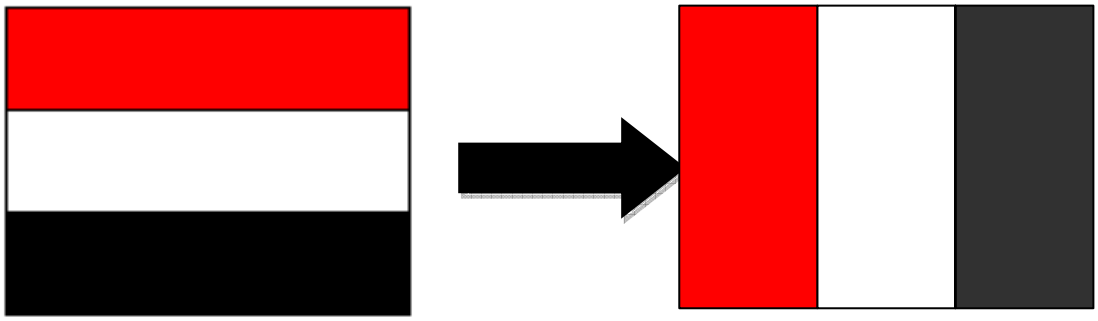
The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃.

Table 3.2-1: DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	2.5	3.3	3.6	V
VIH	High level input voltage	Digital input pins	0.7xVDDIO	-	VDDIO	V
VIL	Low level input voltage	Digital input pins	0	-	0.3xVDD	V
VOH	High level output voltage	IOH = 400uA	VDDIO-0.4	-	-	V
VOL	Low level output voltage	IOL = -400uA	0	-	0.4	V
Iupdate	Module operating current	-	-	2.7	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	0.17	-	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 3.2-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 3.2-1
The Typical power consumption



3.3 AC CHARACTERISTICS

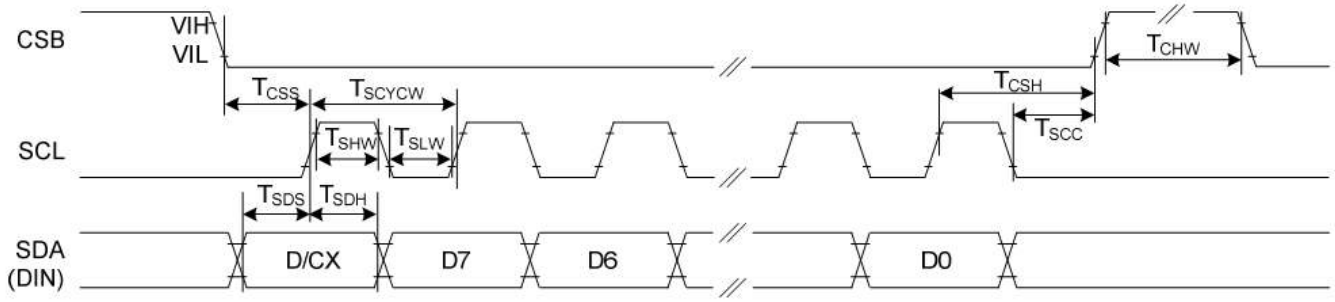


Figure: 3-wire Serial Interface Characteristics (Write mode)

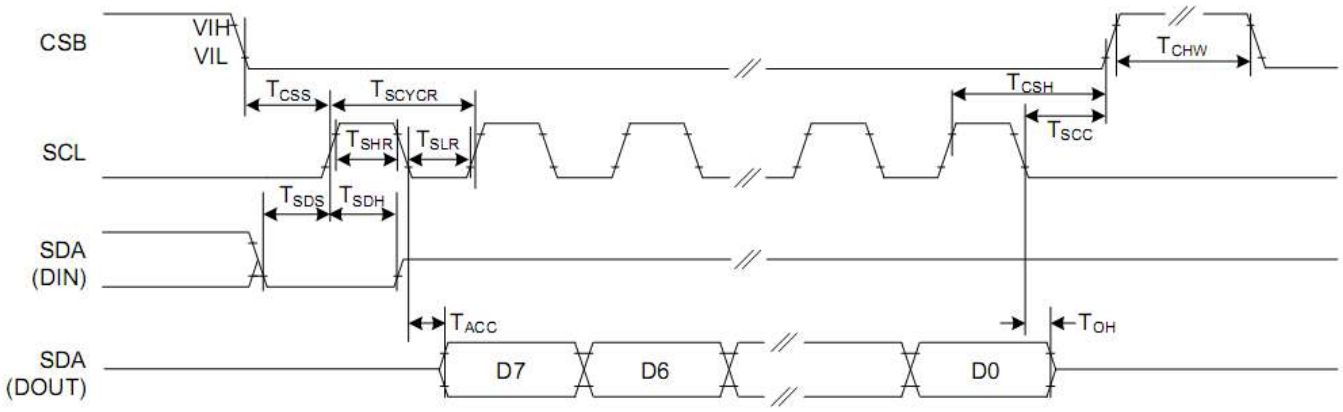


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	MIN	TYP.	MAX.	Unit
TCSS	CSB	Chip select setup time	60			ns
TCSH		Chip select hold time	65			ns
TSCC		Chip select setup time	20			ns
TCHW		Chip select setup time	40			ns
TSCYCW	SCL	Serial clock cycle (Write)	100			ns
TSHW		SCL “H” pulse width (Write)	35			ns
TSLW		SCL “L” pulse width (Write)	35			ns
TSCYCR		Serial clock cycle (Read)	150			ns
TSHR		SCL “H” pulse width (Read)	60			ns
TSLR		SCL “L” pulse width (Read)	60			ns
TSDS	SDA (DIN)	Data setup time	30			ns
TSDH		Data hold time	30			ns
TACC	SDA (DOUT)	Access time			10	ns
TOH		Output disable time	15			ns

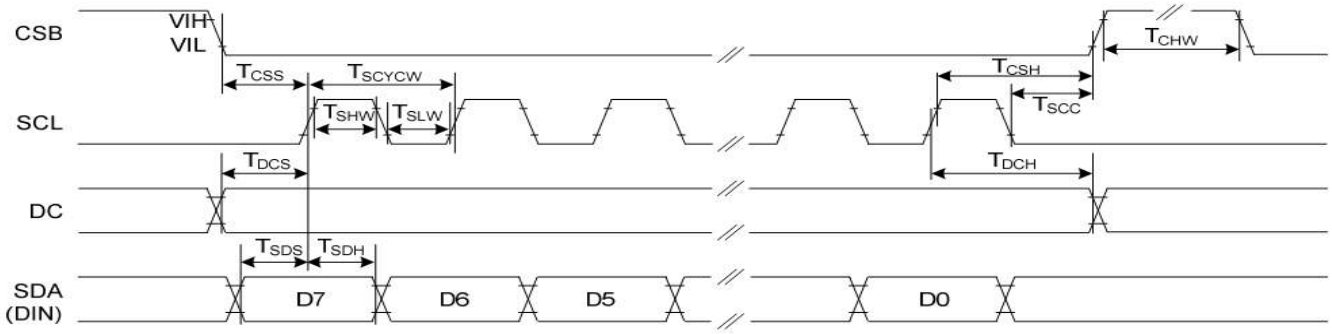


Figure: 4-wire Serial Interface Characteristics (Write mode)

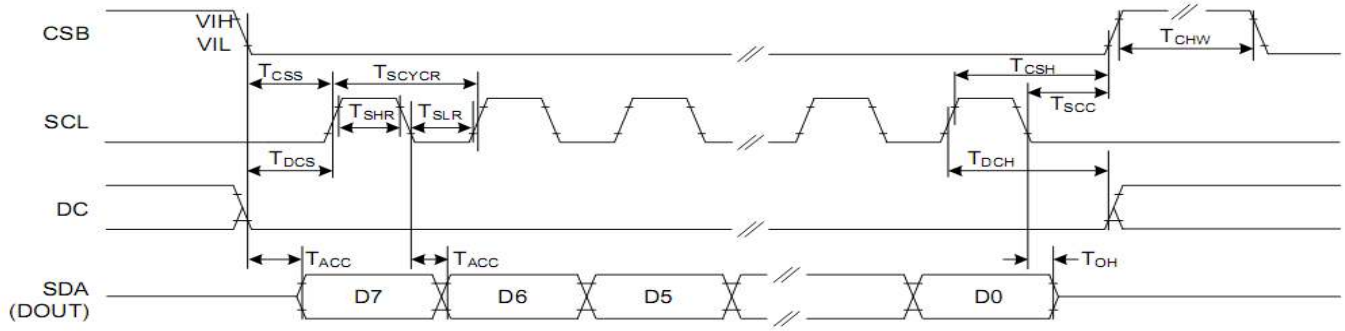


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	MIN	TYP.	MAX.	Unit
TCSS	CSB	Chip select setup time	60			ns
TCSH		Chip select hold time	65			ns
TSCC		Chip select setup time	20			ns
TCHW		Chip select setup time	40			ns
TSCYCW	SCL	Serial clock cycle (Write)	100			ns
TSHW		SCL “H” pulse width (Write)	35			ns
TSLW		SCL “L” pulse width (Write)	35			ns
TSCYCR		Serial clock cycle (Read)	150			ns
TSHR		SCL “H” pulse width (Read)	60			ns
TSLR		SCL “L” pulse width (Read)	60			ns
TDCS	DC	DC setup time	30			ns
TDCH		DC hold time	30			ns
TSDS	SDA (DIN)	Data setup time	30			ns
TSDH		Data hold time	30			ns
TACC	SDA (DOUT)	Access time			10	ns
TOH		utput disable time	15			ns

3.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	10	-	mAs	-
Deep sleep mode	-	25℃	0.17	-	uA	-

mAs=update average current×update time

4. COMMAND TABLE

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel setting(PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R, UD,SHL, SHD_N,RST_N	0Fh
2	Power setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN, VDG_EN	03h
		0	1	-	-	-	#	#	#	#	#	VCOM_HV,VGHL_LV[1:0	00h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W Pixel Data (400x300):	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
		0	1	-	-	-	-	-	-	-	-	-	-
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00h
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	#	#	#	#	#	#	#		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red Pixel Data (400x300):	13h
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00h
		0	1	-	-	-	-	-	-	-	-	-	-
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00h
13	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3CH
#	**Command**	**W/R**	**C/D**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Registers**	**Default**
14	Temperature Sensor	0	0	0	1	0	0	0	0	0	0		40h

	Calibration h (TSC)	1	1	#	#	#	#	#	#	#	#	LM[10:3] / TSR[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	LM[2:0] / -	00h
15	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
16	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
17	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
18	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7
19	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	--	-	-	-	-	-	#	LPD	01h
20	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
21	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	-	-	-	-	-	-	-	#	HRES[8:3]	00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
22	GSST Setting (GSST)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	-	-	-	-	-	-	-	#	HST[8:3]	00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	-	-	-	-	-	-	-	#	VST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
23	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		1	1	#	#	#	#	#	#	#	#	PTL_FLAG ,I2C_ERR, I2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13h
24	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#		00h
25	Auto Measure ment VCOM	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10h
26	Read VCOM Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h
27	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
28	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0	HRST[8:3]	90h
		0	1-	-	-	-	-	-	-	-	#		00h
		0	1	#	#	#	#	#	0	0	0	HRED[8:3] VRST[8:0]	00h
		0	1-	-	-	-	-	-	-	-	#		00h
		0	1	#	#	#	#	#	1	1	1	VRED[8:0] PT_SCAN	07h
		0	1-	-	-	-	-	-	-	-	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1-	-	-	-	-	-	-	-	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1-	-	-	-	-	-	-	-	#		01h
29	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
30	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
31	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	0	0	1	0	0	1	0	1	Check code = A5h	A5h
32	Active Progrmming (APG)	0	0	1	0	1	0	0	0	0	1		A1h
33	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	-	-	-	-	-	-	-	-	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	..	..	..	..	..	..	..	..	..	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
34	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0h
		0	1	-	-	-	-	-	-	#	#	TSFIX, CCEN	00h
35	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h
36	Force Temperauture (TSSET)	0	0	1	1	1	0	0	1	0	1		E5h
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h
37	LPD Selection (LPSEL)	0	0	1	1	1	0	0	1	0	0		E4h
		0	1	-	-	-	-	-	#	#	#	LPMD, LP_SEL[1:0]	03h

Note:

(1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked ‘W/R’ can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

5. COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

1)Panel Setting (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0		0	0	0	0	0	0	0	00h
	1	1	RES1	RES0	REG	-	UD	SHL	SHD_N	RST_N	0Fh

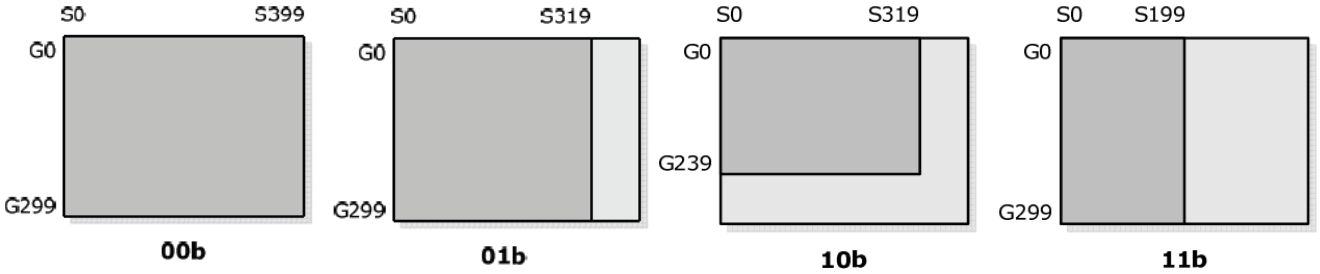
RES[1:0]: Display Resolution setting (source x gate)

00b: 400x300 (Default) Active source channels: S0 ~ S399. Active gate channels: G0 ~ G299.

01b: 320x300 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G299.

10b: 320x240 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G239.

11b: 200x300 Active source channels: S0 ~ S199. Active gate channels: G0 ~ G299.



REG: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red. (Default)

1: Pixel with Black/White.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 →Gn-2→Gn-3 →…→G0

1: Scan up. (Default) First line to Last line: G0 →G1 →G2 →… … . →Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 →Sn-2→Sn-3→…→S0

1: Shift right. (Default) First data to Last data: S0 →S1 →S2 →… … . →Sn-1

SHD_N: Booster Switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.

1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will be kept until VDD OFF, and source driver output and VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, and Source/BD VCOM: 0V. All drivers will be reset, all registers will be reset to their default value, and all functions will be disabled. Source driver, gate driver and VCOM will be released to floating.

1: No effect (Default).

2)Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01h
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00h
	0	1	-	-	VDH[5:0]						26h
	0	1	-	-	VDL[5:0]						26h
	0	1	-	-	VDHR[5:0]						03h

VDS_EN: Source power selection

0 : External source power from VDH/VDL pins

1 : Inetrnal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level

0 : VCOMH=VDH+DC-VCOM, VCOML=VDL+DC-VCOM

1 : VCOMH=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage level
00 (DEFAULT)	VGH=16V, VGL= -16V
01	VGH=15V, VGL= -15V
10	VGH=14V, VGL= -14V
11	VGH=13V, VGL= -13V

VDH[5:0]: Internal VDH power selection for B/W pixel.(Default value: 100110b)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8V	001110	5.2 V	011010	7.6 V	100110	10.0 V
000011	3.0 V	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2 V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

VDL[5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	-2.4 V	001100	-4.8 V	011000	-7.2 V	100100	-9.6 V
000001	-2.6 V	001101	-5.0 V	011001	-7.4 V	100101	-9.8 V
000010	-2.8V	001110	-5.2 V	011010	-7.6 V	100110	-10.0 V
000011	-3.0 V	001111	-5.4 V	011011	-7.8 V	100111	-10.2 V
000100	-3.2 V	010000	-5.6 V	011100	-8.0 V	101000	-10.4 V
000101	-3.4 V	010001	-5.8 V	011101	-8.2 V	101001	-10.6 V
000110	-3.6 V	010010	-6.0 V	011110	-8.4 V	101010	-10.8 V
000111	-3.8 V	010011	-6.2 V	011111	-8.6 V	101011	-11.0 V
001000	-4.0 V	010100	-6.4 V	100000	-8.8 V	(others)	-11.0 V
001001	-4.2 V	010101	-6.6 V	100001	-9.0 V		
001010	-4.4 V	010110	-6.8 V	100010	-9.2 V		
001011	-4.6 V	010111	-7.0 V	100011	-9.4 V		

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8V	001110	5.2 V	011010	7.6 V	100110	10.0 V
000011	3.0 V	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2 V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

3)Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02h

After the Power OFF command, the driver will be powered OFF. The sequence refers to POWER MANAGEMENT register section. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but data will be kept until VDD turned OFF or Deep Sleep Mode. Both source driver outputs and VCOM will be released to floating.

4)Power OFF Sequence Setting(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04h

After the Power ON command, the driver will be powered ON The sequence refers to POWER MANAGEMENT section. This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

6) Power ON MEASURE(PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power ON MEASURE	0	0	0	0	0	0	0	1	0	1	05h

This command enables the internal bandgap, which will be cleared by the next POF.

7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06h
	0	1	BT_PHA 7	BT_PHA 6	BT_PHA 5	BT_PHA 4	BT_PHA 3	BT_PHA 2	BT_PHA 1	BT_PHA 0	17h
	0	1	BT_PHB 7	BT_PHA 6	BT_PHB 5	BT_PHB 4	BT_PHB 3	BT_PHB 2	BT_PHB 1	BT_PHB 0	17h
	0	1	-	-	BT_PHC 5	BT_PHC 4	BT_PHC 3	BT_PHC 2	BT_PHC 1	BT_PHC 0	17h

BTPHA[7:6]: Soft start period of phase A.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS
BTPHA[5:3]: Driving strength of phase A
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)
BTPHA[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS
BTPHB[7:6]: Soft start period of phase B.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS
BTPHB[5:3]: Driving strength of phase B
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)
BTPHB[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS
BTPHC[5:3]: Driving strength of phase C
000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	111b: 6.58uS

8) Deep sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07h
	0	1	1	0	1	0	0	1	0	1	A5h

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	0	1	…	…	…	…	…	…	…	…	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM.
In B/W mode, this command writes “OLD” data to SRAM.
In B/W/Red mode, this command writes “B/W” data to SRAM.
In Program mode, this command writes “OTP” data to SRAM for programming.

10) Data stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11h
	1	1	data_flag	-	-	-	-	-	-	-	00h

Check the completeness of data. If data is complete, start to refresh display.
Data_flag: Data flag of receiving user data.
0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).
After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.
The waiting interval form BUSY_N falling to the first FLG command must be > 200uS.

11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12h

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be > 200uS.

12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13h
	0	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	0	1	…	…	…	…	…	…	…	…	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM.

In B/W mode, this command writes "NEW" data to SRAM.

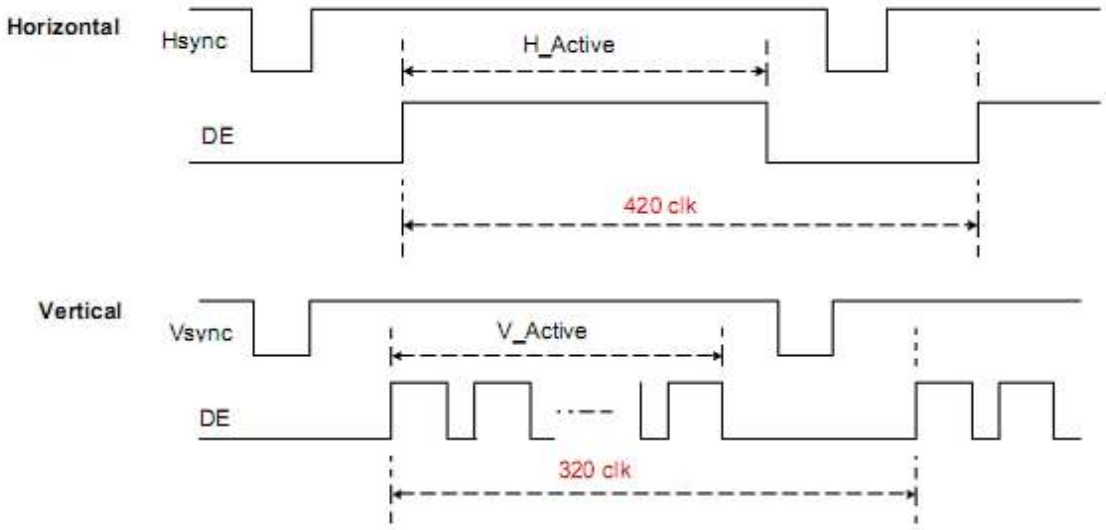
In B/W/Red mode, this command writes "RED" data to SRAM.

13) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30h
	0	1	-	-	M[2:0]			N[2:0]			3Ch

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	FR	M	N	FR	M	N	FR	M	N	FR
1	1	29	3	1	86	5	1	150	7	1	200
	2	14		2	43		2	72		2	100
	3	10		3	29		3	48		3	67
	4	7		4	21		4	36		4	50
	5	6		5	17		5	29		5	40
	6	5		6	14		6	24		6	33
	7	4		7	12		7	20		7	29
2	1	57	4	1	114	6	1	171			
	2	29		2	57		2	86			
	3	19		3	38		3	57			
	4	14		4	29		4	43			
	5	11		5	23		5	34			
	6	10		6	19		6	29			
	7	8		7	16		7	24			



14) Temperature Sensor Calibration(TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	0	1	0	0	0	0	0	0	40h
	1		D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00h
	1	1	D2	D1	D0	-	-	-	-	-	00h

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (℃)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8

TS[7:0]/D[10:3]	Temperature (℃)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17

TS[7:0]/D[10:3]	Temperature (℃)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42

1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

15) Temperature Sensor Internal/External(TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	0	1	0	0	0	0	0	1	41h
	0	1	TSE	-	-	-	TO[3:0]				00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	+0 (Default)
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

16) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42h
	0	1	WATTR[7:0]								00h
	0	1	WMSB[7:0]								00h
	0	1	WLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I2C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

17) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43h
	1	1	RMSB[7:0]								00h
	1	1	RLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.
RMSB[7:0]: MSByte read data from external temperature sensor
RLSB[7:0]: LSByte read data from external temperature sensor

18) VCOM and Data Interval Setting(CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between h VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]			CDI[3:0]			D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).
VBD[1:0]: Border data selection
Under B/W/Red mode (KW/R=0):

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	Floating

Under B/W mode (KW/R=1):

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1→ 0)
	10	LUTWB (0 →1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWB (1→ 0)
	10	LUTBW (0→1)
	11	Floating

DDX[1:0]: Data polality.
Under B/W/Red mode (KW/R=0):
DDX[1] is for RED data.
DDX[0] is for BW data

DDX[0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR

DDX[0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

Under B/W mode (KW/R=1):
DDX[1] is for B/W mode with New/Old,
DDX[0] is for B/W mode without New/Old.

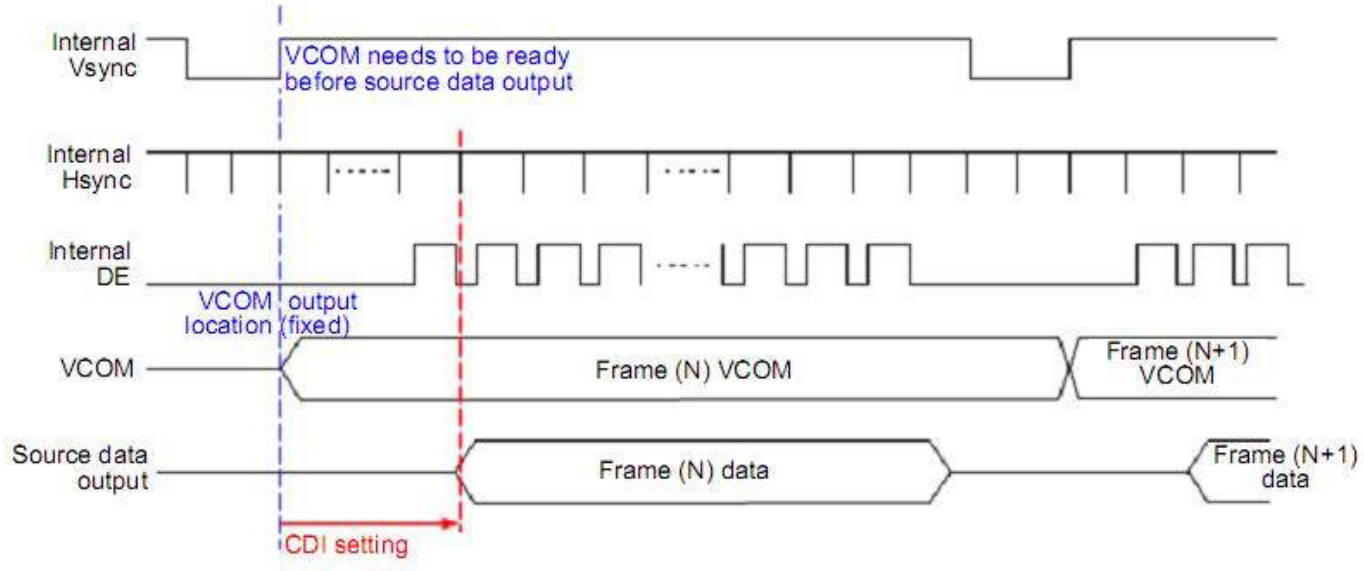
DDX[0]	Data {New, Old}	LUT
00	00	LUTWW (0→0)
	01	LUTBW (1→0)
	10	LUTWB (0→1)
	11	LUTBB (1→1)
01 (Default)	00	LUTBB (0→0)
	01	LUTWB (1→0)
	10	LUTBW (0→1)
	11	LUTWW (1→1)

DDX[0]	Data {New}	LUT
10	0	LUTBW (1→0)
	1	LUTWB (0→1)
11	0	LUTWB (1→0)
	1	LUTBW (0→1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	VCOM and Data Interval
0000b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	VCOM and Data Interval
1000	9
1000	8
1010	7
1010	6
1100	5
1100	4
1110	3
1111	2



19) Low Power Detection(LPD) (R51h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD:

When LPMD=0, LPD is used as Internal Low Power Detection Flag

0: Low power input (VDD<2.5V, selected by LP_SEL) 1: Normal status (default)

When LPMD=1, LPD is used as Panel Break Check Flag

0: Panel check fail (Panel broken) 1: Panel Check pass

20) TCON Setting(TCON) (R60h)

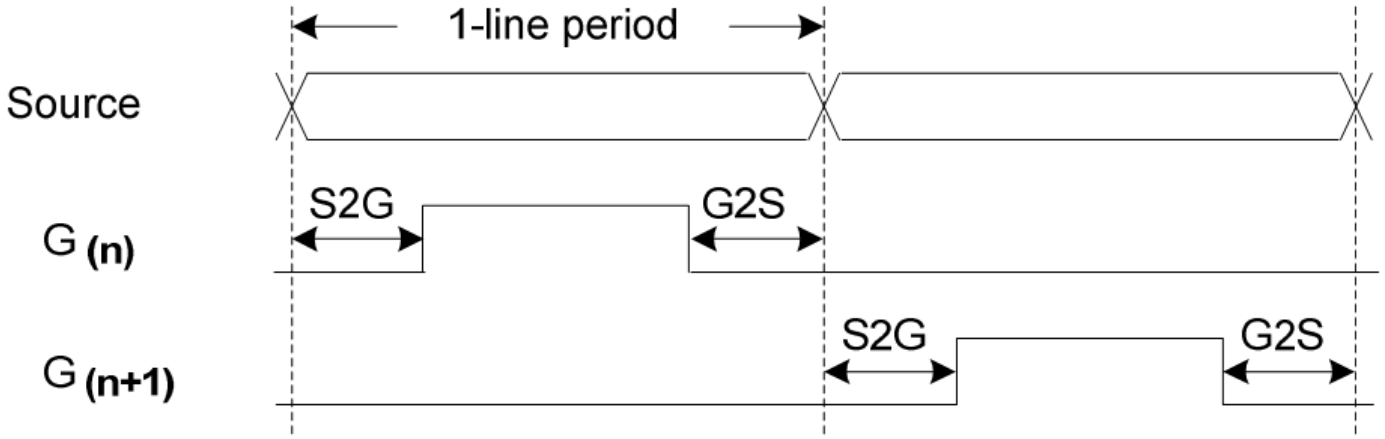
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap h Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		1000 b	36
0001	8		1001	40
0010	12(Default)		1010	44
0011	16		1011	48
0100	20		1100	52
0101	24		1101	56
0110	28		1110	60
0111	32		1111	64

Period = 660 nS.



21) Resolution Setting(TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	-	-	-	-	-	-	-	HRES[8]	00h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[8:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

Source: First active source, defined by HST[8:3] (Refer to the following command GSST). (Default: S0).

LAST active source = HRES[8:3]*8 - 1

Gate: First active gate, defined by VST[8:0] (Refer to the following command GSST). (Default: G0).

LAST active gate = VRES[8:0] - 1

Example: 128x272

Source: First active source = S0 (default start source), LAST active source = 16*8 – 1 = 127; (HRES[8:3]=16, S127)

Gate: First active gate = G0 (default start gate), LAST active gate = 272 - 1= 271; (VRES[8:0] = 272, G271)

22)GSST Setting(GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Gate/Source Start setting	0	0	0	1	1	0	0	1	0	1	65h
	0	1	-	-	-	-	-	-	-	HST8	00h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST8	00h
	0	1	VST[7:0]								00h

This command defines the Fist Active Gate and First Active Source of active channels.

HST[8:3]: First active source. (Default: S0)

VST[8:0]: First active gate. (Default: G0)

23) Revision(REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	LUT_REV								00h

The LUT_REV is read from OTP address = 0x001.

24) Get status(FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_flag	I^2C_ERR	I^2C_BUSYN	date_flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG: Partial display status (high: partial mode)
I2C_ERR: I2C master error status
I2C_BUSYN: I2C master busy status (low active)
data_flag: Driver has already received all the one frame data
PON: Power ON status
POF: Power OFF status
BUSY_N: Driver busy status (low active)

25) Auto measure vcom(AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure vcom	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time
00b: 3s 01b: 5s (default)
10b: 8s 11b: 10s
XON: All Gate ON of AMV
0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.
AMVS: Source output of AMV
0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.
AMV: Analog signal
0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)
AMVE: Auto Measure VCOM Enable (/Disable)
0: No effect
1: Trigger auto VCOM sensing.

26) VCOM Value(VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure vcom	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[5:0]						00h

This command gets the VCOM value.

VV[5:0]: VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

27) VCOM-DC Setting(VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[5:0]						00h

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	others	-3.00

28) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	-	-	-	-	-	-	-	HRST[8]	00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	HRED[8]	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[8:3]: Horizontal start channel bank. (value 00h~31h)

HRED[8:3]: Horizontal end channel bank. (value 00h~31h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~12Bh)

VRED[8:0]: Vertical end line. (value 000h~12Bh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

29) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

30) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

31) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h
	0	1	1	0	1	0	0	1	0	1	A5h

After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leaving program mode.

32) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

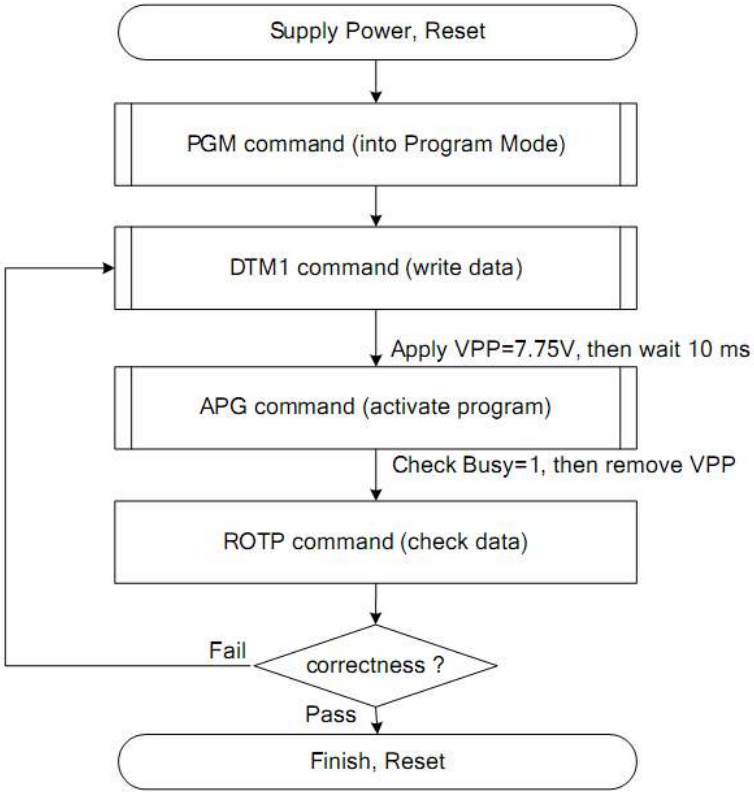
After this command is transmitted, the programming state machine would be activated. The BUSY flag would fall to 0 until the programming is completed.

33) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--h
	1	1	The data of address 0x000 in the OTP								--h
	1	1	The data of address 0x001 in the OTP								--h
	1	1	…								--h
	1	1	The data of address (n-1) in the OTP								--h
	1	1	The data of address (n) in the OTP								--h

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0xFFF.



The sequence of programming OTP.

34) CASCADE SETTING (CCSET) (E0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperuature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

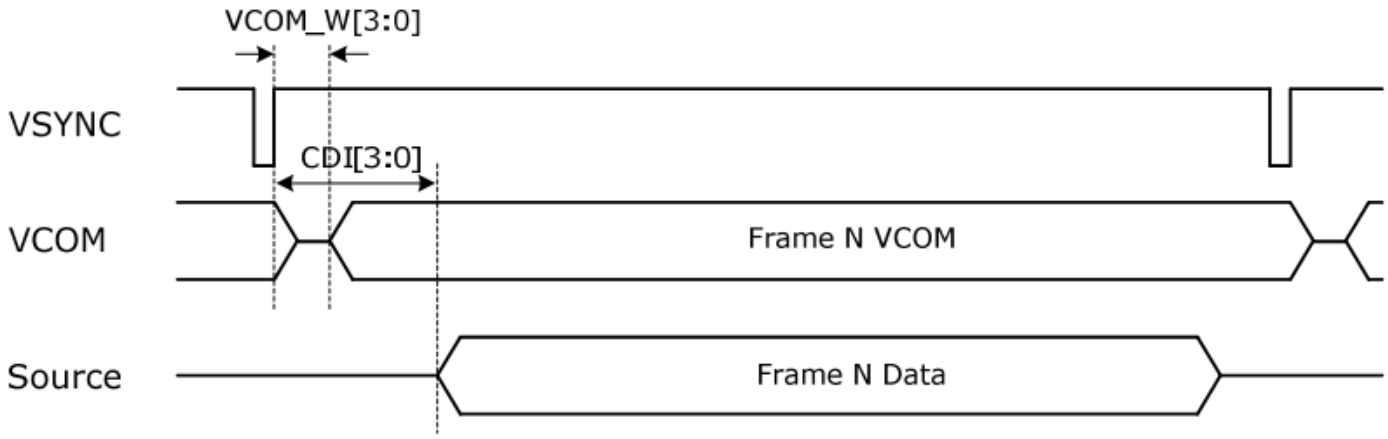
1: Temperature value is defined by TS_SET[7:0] registers.

35) POWER SAVING (PWS) (E3H)

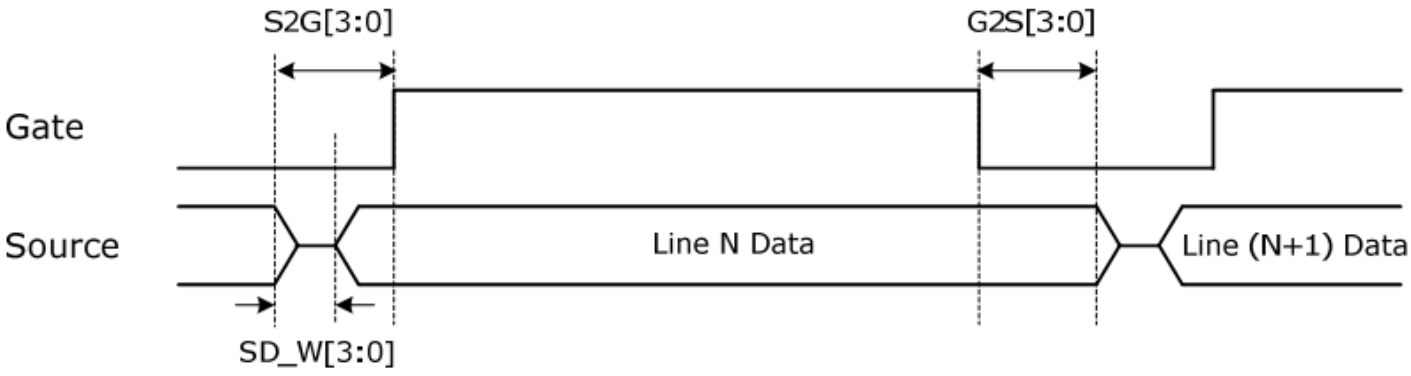
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & 0Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



36) FORCE TEMPERATURE (TSSET) (E5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temeperature	0	0	1	1	1	0	0	1	0	1	E5h
Value for h Cascade	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

37) LPD SELECTION (LPSEL) (E4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temeperature Value for Cascade	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	LPMD	LP_SEL[1:0]		03h

This command is used for cascade to fix the temperature value of master and slave chip.

LP_SEL[1:0]: LPD Level Setting

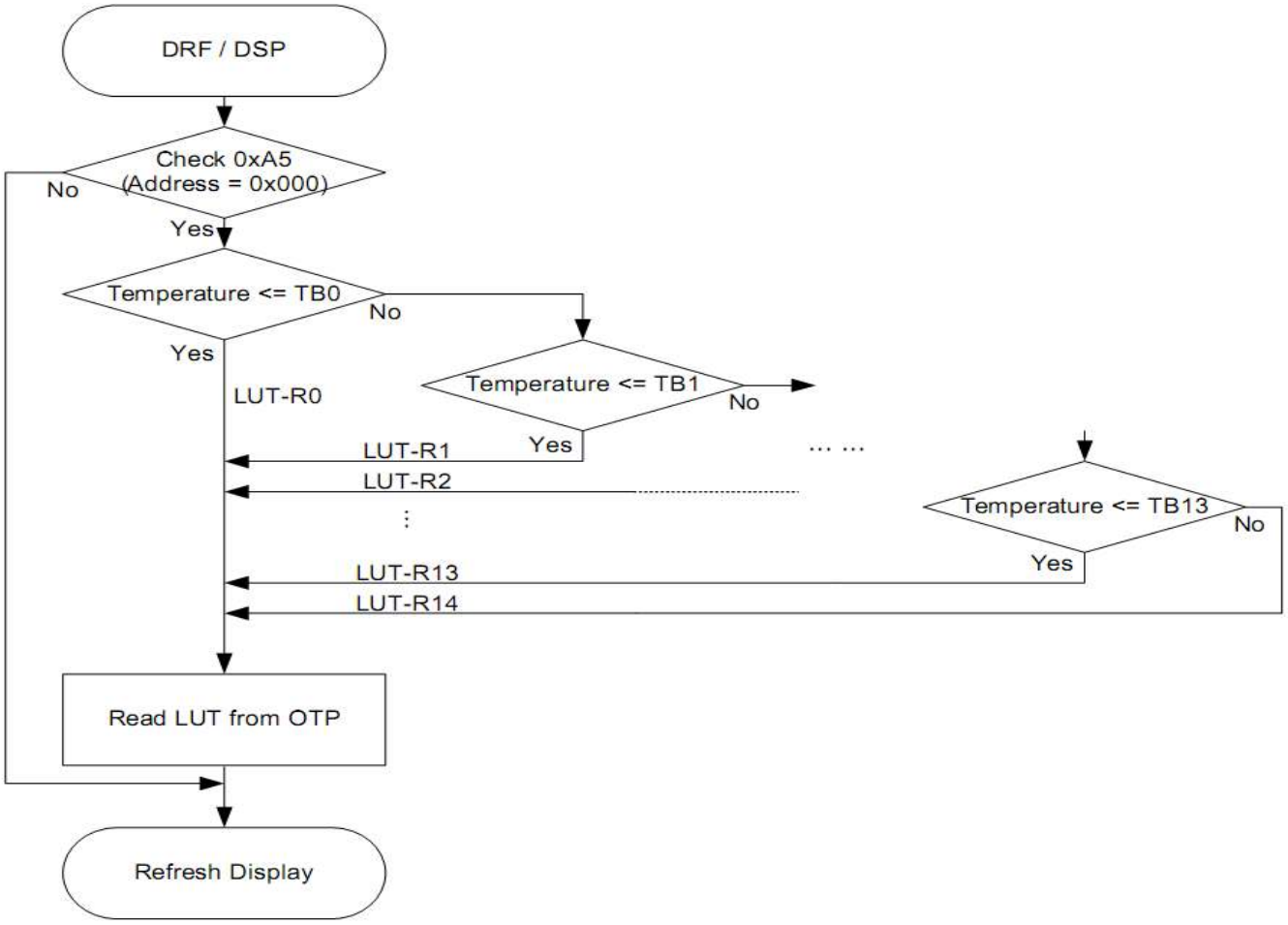
LP_SEL[1:0]	LPD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5V (default)

LPMD: Low Power Detection / Panel Break Check Selection.

0: Low Power Detection. (default)

1: Panel Break Check.

6. TEMPERATURE RANGE



Temperature Selection Mechanism

The temperature selection mechanism consists of a less-than-or-equal-to operator and 14 temperature boundary settings (TBx) to determine 15 temperature ranges. The sequence of mechanism is from TB0 to TB13, as shown below. If less than 15 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Example:

If temperature = -20 oC, LUT-R0 is selected.
If temperature = -10 oC, LUT-R1 is selected.
If temperature = 0 oC, LUT-R2 is selected.
If temperature = 20 oC, LUT-R4 is selected.
If temperature = 40 oC, LUT-R5 is selected.
If temperature > 40 oC, LUT-R5 is selected.

OTP Address	Content	
002h	0xF1	(-15 ℃)
003h	0xFB	(-5 ℃)
004h	0x00	(0 ℃)
005h	0x0A	(10 ℃)
006h	0x1E	(30 ℃)
007h	0x7F	

Table 2: Temperature Boundary (TBx) Setting in OTP

OTP Address (Hex)	Content	Description
002h	TB0	If temperature ⩽ TB0, LUT-R0 is selected. (start address=0x100)
003h	TB1	If temperature ⩽ TB1, LUT-R1 is selected. (start address=0x200)
004h	TB2	If temperature ⩽ TB2, LUT-R2 is selected. (start address=0x300)
005h	TB3	If temperature ⩽ TB3, LUT-R3 is selected. (start address=0x400)
006h	TB4	If temperature ⩽ TB4, LUT-R4 is selected. (start address=0x500)
007h	TB5	If temperature ⩽ TB5, LUT-R5 is selected. (start address=0x600)
008h	TB6	If temperature ⩽ TB6, LUT-R6 is selected. (start address=0x700)
009h	TB7	If temperature ⩽ TB7, LUT-R7 is selected. (start address=0x800)
00Ah	TB8	If temperature ⩽ TB8, LUT-R8 is selected. (start address=0x900)
00Bh	TB9	If temperature ⩽ TB9, LUT-R9 is selected. (start address=0xA00)
00Ch	TB10	If temperature ⩽ TB10, LUT-R10 is selected. (start address=0xB00)
00Dh	TB11	If temperature ⩽ TB11, LUT-R11 is selected. (start address=0xC00)
00Eh	TB12	If temperature ⩽ TB12, LUT-R12 is selected. (start address=0xD00)
00Fh	TB13	If temperature ⩽ TB13, LUT-R13 is selected. (start address=0xE00)
-	-	If temperature > TB13, LUT-R14 is selected. (start address=0xF00)

7. Optical characteristics

7.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	ARAMETER	CONDITIONS	MIN	TYPE	M X	UNIT	Note
R	Reflecta ce	White	30	35	-	%	Note 7.1-1
Gn	2 ey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	℃～40℃		5years	-	-	Note 7.2-2

WS: White state, DS : Dark state

Note 7.1-1: Luminance meter : Eye - One Pro Spectrophotometer

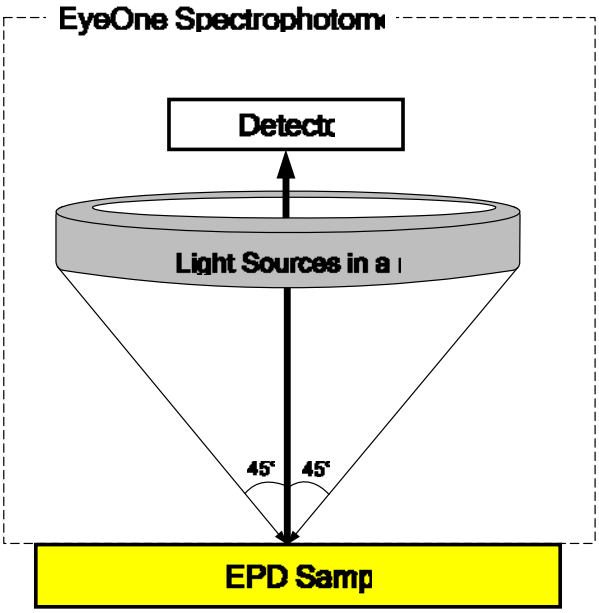
Note 7.1-2: We guarantee display quality from 0℃～40℃ generally,If operation ambient temperature from 0℃～40℃, will Offer special waveform by Waveshare.

Note 7.1-3: We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH；at least update 1 time per day.

7.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd

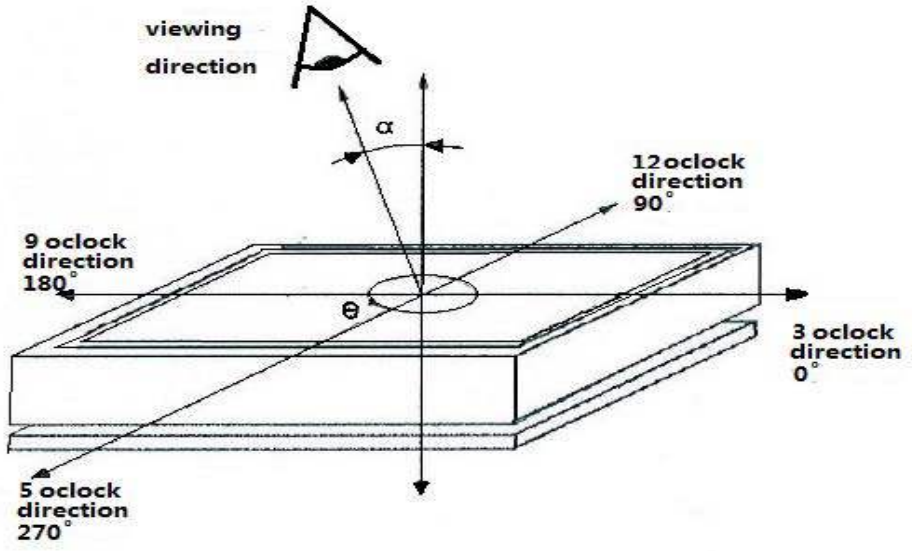


7.3 Reflection Ratio

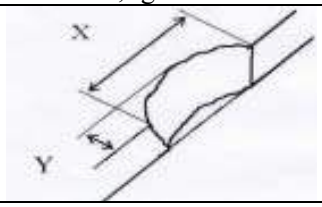
The reflection ratio is expressed as:

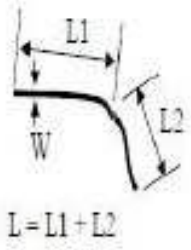
R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

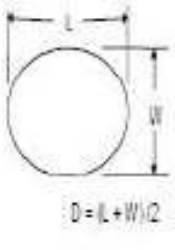


8. Point and line standard

<table>
<tr><th colspan="7">Shipment Inspection Standard</th></tr>
<tr><td colspan="7">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>91 (H) × 77(V) × 1.25(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5%RH</td><td>800～1300Lux</td><td>300 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td>Defet type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="4">Spot</td><td rowspan="4">Electric Display</td><td colspan="2">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">0.40 ㎜＜D≤0.5 ㎜</td><td colspan="2">N≤1</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.5 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">L≤2 ㎜，W≤0.2 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">2.0mm＜L≤8.0mm，0.2＜W≤0.5mm,</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">L＞8.0 ㎜，W＞0.5 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.25mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25mm≤D≤0.40mm</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.40 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤6mm，Y≤0.5mm, Do not affect the electrode circuit , Ignore</td></tr>
<tr><td colspan="5"> 
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="6">1.Cannot be defect & failure cause by appearance defect；</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearance defect；</td></tr>
<tr><td colspan="6">L=long W=wide D=point size N=Defects NO</td></tr>
</table>



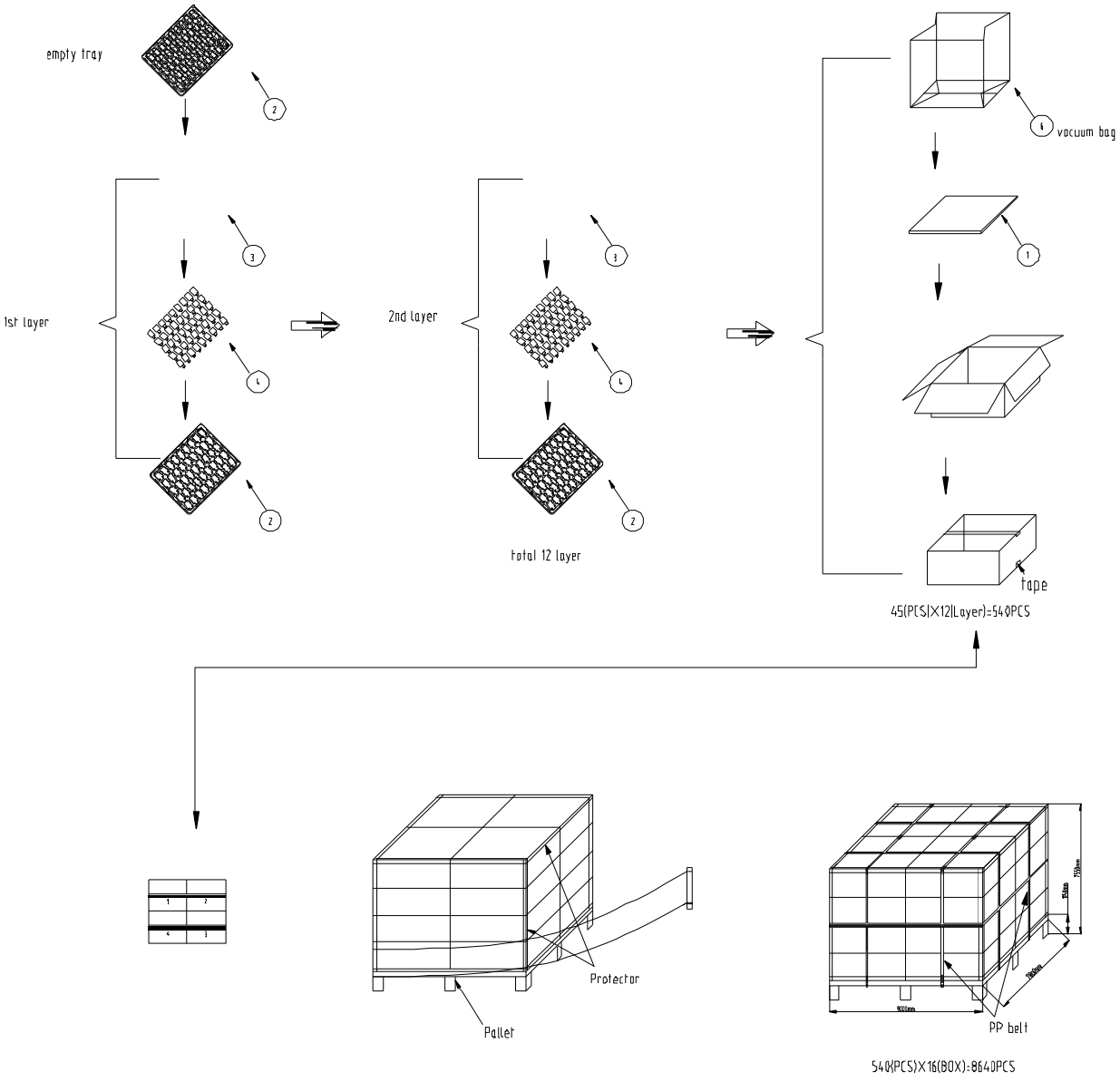
Line Defect



Spot Defect

L=long W=wide D=point size

9. Packing


empty tray
2
1st layer
3
4
2
2nd layer
3
4
2
Total 12 layer
4
vacuum bag
1
tape
45(PCS)X12(Layer)=540PCS
Protector
Pallet
PP belt
540(PCS)X16(BOX)=8640PCS

10. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.