User's Guide

TPS62110 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS62110EVM evaluation module (EVM). This EVM is designed to help the user easily evaluate and test the operation and functionality of the TPS62110. This User's Guide includes setup instructions for the hardware, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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Trademarks

1 Introduction

The Texas Instruments TPS62110 is a 1.5-A synchronous step-down converter in a 16-pin QFN package. Both fixed and adjustable output voltage units are available.

1.1 Background

The TPS62110EVM-101 uses the TPS62110 adjustable version and is set to 3.3 V output. The EVM operates with full rated performance with an input voltage between 3.6 V and 17 V.

1.2 Performance Specification

Table 1-1 provides a summary of the TPS62110EVM-101 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1-1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input Voltage		3.6		17	V
Output Voltage	Iout = 10 mA to 1500 mA	3.267	3.3	3.333	V
Output Current		0		1500	mA
Low Battery Output (LBO)	VIN	5.8	6.0	6.2	V
Power Good (PG)	VOUT		3.25		V

1.3 Modifications

The PWB for this EVM is designed to accommodate both the fixed and adjustable versions of this IC. If the fixed version is installed, replace R1 with a 0-Ω resistor; R1 and C3 are open. If additional filtering is desired, C5 can be added.

1.3.1 Adjustable Output IC U1 Operation

U1 is configured for evaluation of the adjustable output version. This unit is configured for 3.3 V. Resistors R1 and R2 are used to set the output voltage between 1.2 V and 16 V. See the TPS62110 datasheet (SLVS585) for recommended values. The feedforward capacitor C3 may also need to be changed. For more information see the data sheet.

1.3.2 Fixed Output Operation

U1 can be replaced with the fixed version for evaluation. For fixed-version operation, replace R1 with a 0-Ω resistor; R2 and C3 positions remain unpopulated.

2 Setup

This section describes how to properly use the TPS62110EVM-101.

2.1 Input / Output Connector Descriptions

J1–VIN	Positive input connection from the input supply for U1
J2–GND	Return connection from the input supply for U1, common with J4.
J3–VOUT	Output voltage connection
J4–GND	Output return connection, common with J2
J5–LBO/PG	Low battery output (LBO) pulled up to Vout; low indicates LBI is below its threshold. Power good (PG), low indicates output voltage is less than 98.4% of the normal value.
J**P1–SYNC PFM/PWM**	Input for synchronization to external clock signal. High forces low-noise PWM mode, low enables power save PFM/PWM mode.
JP2–EN	Enable pin, low on the EN turns unit off.

2.2 Setup

To operate the EVM, simply connect an input supply to the appropriate pins, and then connect a load to the appropriate pins. Maximum recommended load is 1.5 A or 2.2 Ω. Input supply of 6 V to 17 V is recommended.

3 Board Layout

This section provides the TPS62110EVM-101 board layout and illustrations.

3.1 Layout

Figure 3-1 shows the board layout for the TPS62110EVM-101 PWB.

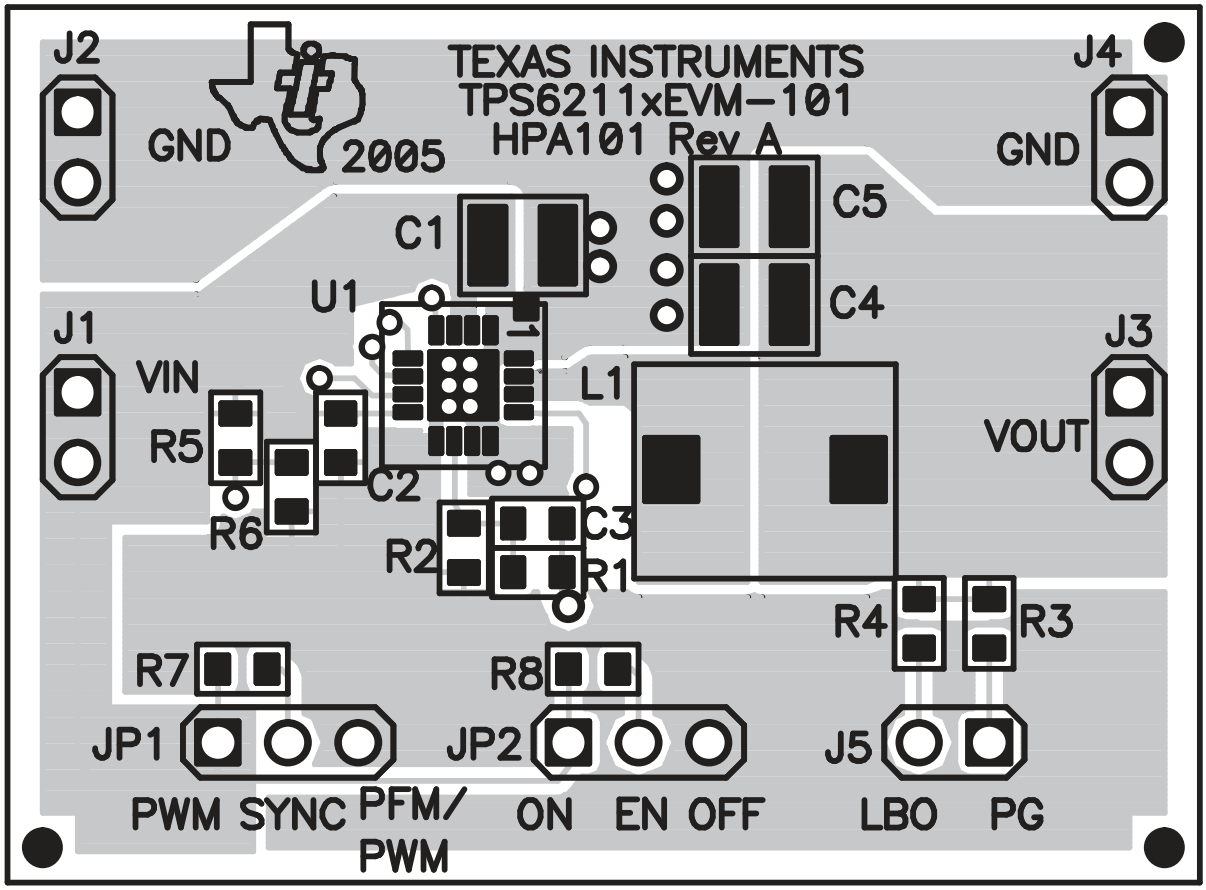

Figure 3-1. Assembly Layer

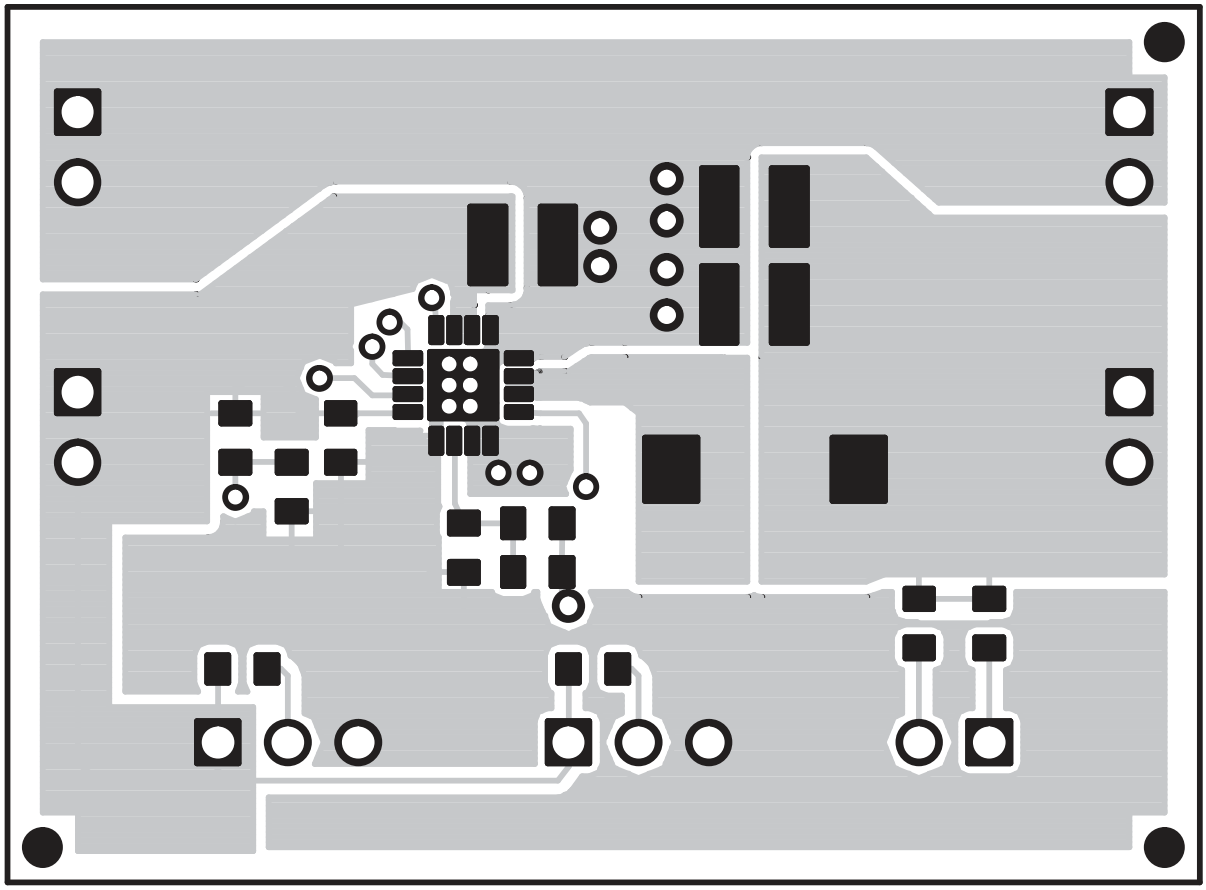

Figure 3-2. Top Layer Routing

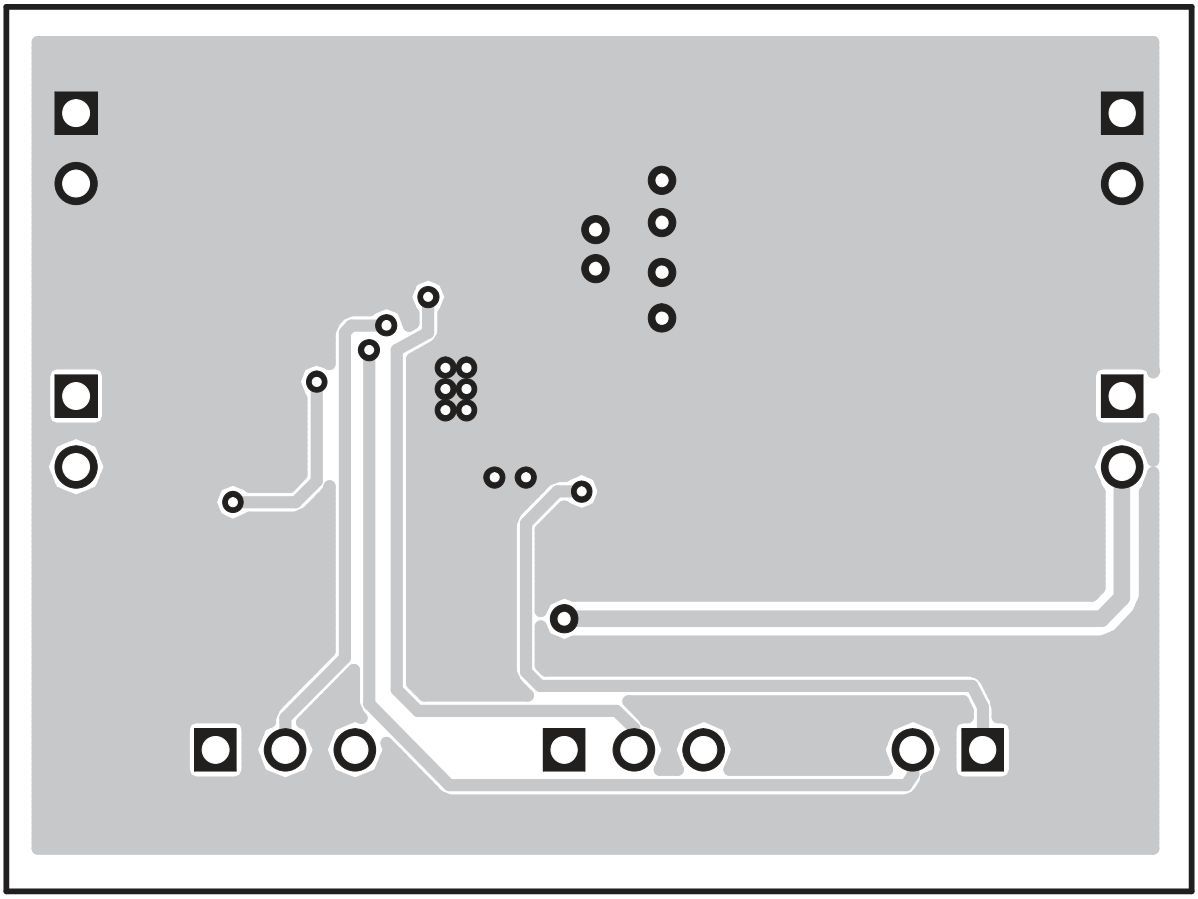

Figure 3-3. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the TPS62110EVM-101 schematic and bill of materials.

4.1 Schematic

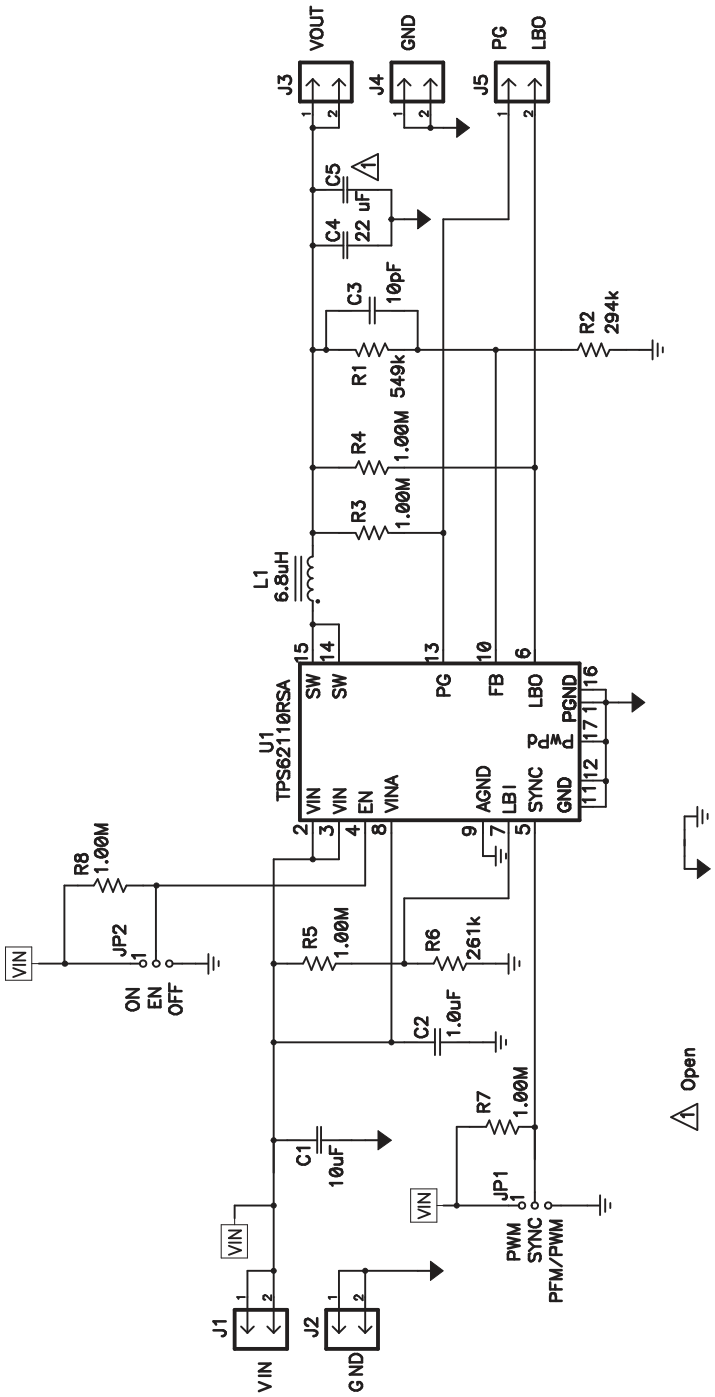

Figure 4-1. TPS62110EVM-101 Schematic

4.2 Bill of Materials

Table 4-1. TPS62110EVM-101 Bill of Materials

COUNT	Ref Des	DESCRIPTION	SIZE	PART NUMBER	MFR
1	C1	Capacitor, Ceramic, 10-µF, 25-V, X5R, 10%	1210	C3225X5R1E106K	TDK
1	C2	Capacitor, Ceramic, 1.0-µF, 16-V, X7R, 10%	0603	C1608X7R1C105K	TDK
1	C3	Capacitor, Ceramic, 10-pF, 50-V, C0G, 5%	0603	C1608C0G1H100DB	TDK
1	C4	Capacitor, Ceramic, 22-µF, 16-V, X7R, 20%	1210	C3225X7R1C226M	TDK
0	C5	Capacitor, Ceramic, xx-µF, xx-V	0805		
5	J1–J5	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
2	JP1, JP2	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
1	L1	Inductor, SMT, 6.8-µH, 1.6-A, 49.2-mΩ	0.276 sq	SLF7032T-6R8M1R6	TDK
1	R1	Resistor, Chip, 549 kΩ, 1/16-W, 1%	0603	Std	Std
1	R2	Resistor, Chip, 294 kΩ, 1/16-W, 1%	0603	Std	Std
5	R3–R8	Resistor, Chip, 1.00 MΩ, 1/16-W, 1%	0603	Std	Std
1	R6	Resistor, Chip, 261 kΩ, 1/16-W, 1%	0603	Std	Std
1	U1	IC, Synchronous Step-Down Converter, 17V, 1.5A	QFN-16	TPS62110RSA	TI
1	–	PCB, 1.7-Inch × 1.25-Inch × 0.062-Inch		HPA101	Any
2	–	Shunt, 100-mil, black	0.100	929950-00	3M

5 Related Documentation From Texas Instruments

1. TPS62110 data sheet (SLVS585)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2005) to Revision A (June 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated user's guide title	2

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