

Using the *TPSM53604EVM*, *TPSM53603EVM*, and *TPSM53602EVM*

These evaluation boards (EVMs) feature the TPSM53604 (4 A), TPSM53603 (3 A), or TPSM53602 (2 A) synchronous-buck power module configured for operation with typical 3.8-V to 36-V input bus applications. The output voltage is set to one of five popular values by using a configuration jumper. The EVM supplies the full output current rating of the device. Input and output capacitors are included on the board to accommodate the entire range of input voltage and the selectable output voltages on the EVM. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points and jumpers are provided for use of the enable (EN) and power-good (PGOOD) features of the device. The recommended PCB layout of the EVM maximizes thermal performance and minimizes output ripple and noise.

NOTE: This EVM user's guide applies to all 3 devices. The only differences in the EVMs are the U1 IC and the silk screen labeling.

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1 Getting Started

Figure 1 highlights the user interface items associated with the EVM. The *VIN Power* terminal block (J1) is used for connection to the host input supply and the *VOUT Power* terminal block (J4) is used for connection to the load. These terminal blocks accept up to 16-AWG wire.

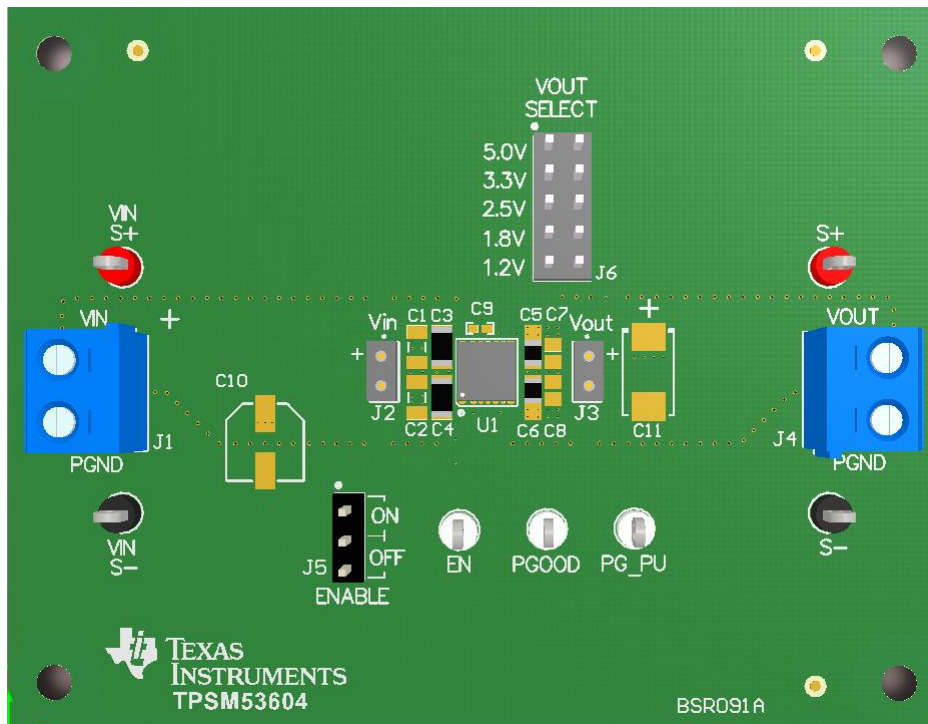


Figure 1. EVM User Interface

- Use the VIN S+ and VIN S- test points along with the VOUT S+ and VOUT S- test points located near the power terminal blocks as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.
- Use the VIN scope (J2) and VOUT scope (J3) test points to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended to use un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. Connect the scope probe tip to the top socket labeled "+" and connect the scope ground lead to the bottom socket.
- The control test points located near the bottom of the EVM test the features of the device. Refer to the [Test Points Descriptions](#) section of this user's guide for more information on the individual control test points.
- The VOUT SELECT jumper (J6) is provided to select the desired output voltage: 1.2 V, 1.8 V, 2.5 V, 3.3 V, 5.0 V. Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.
- The device can be turned on or off using the Enable jumper (J5). Place the jumper in the ON position to enable the device. Place the jumper in the OFF position to disable the device. The undervoltage lockout (UVLO) can be set by populating resistors R1 and R2 located on the bottom side of the EVM. Refer to the [TPSM53604 3.8-V to 36-V Input, 1-V to 7-V Output, 4-A Power Module Data Sheet](#), [TPSM53603 3.8-V to 36-V Input, 1-V to 6-V Output, 3-A Power Module Data Sheet](#), or [TPSM53602, 3.8 V to 36 V Input, 1 V to 6 V Output, 2-A Power Module Data Sheet](#) for recommended UVLO resistor values. The power good (PGOOD) test point is available to monitor when a valid output voltage is present on the EVM. Additionally, the PG_PU pin is present as a convenient point to connect a pullup voltage for the PGOOD signal.

2 Test Point Descriptions

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. [Table 1](#) describes each test point.

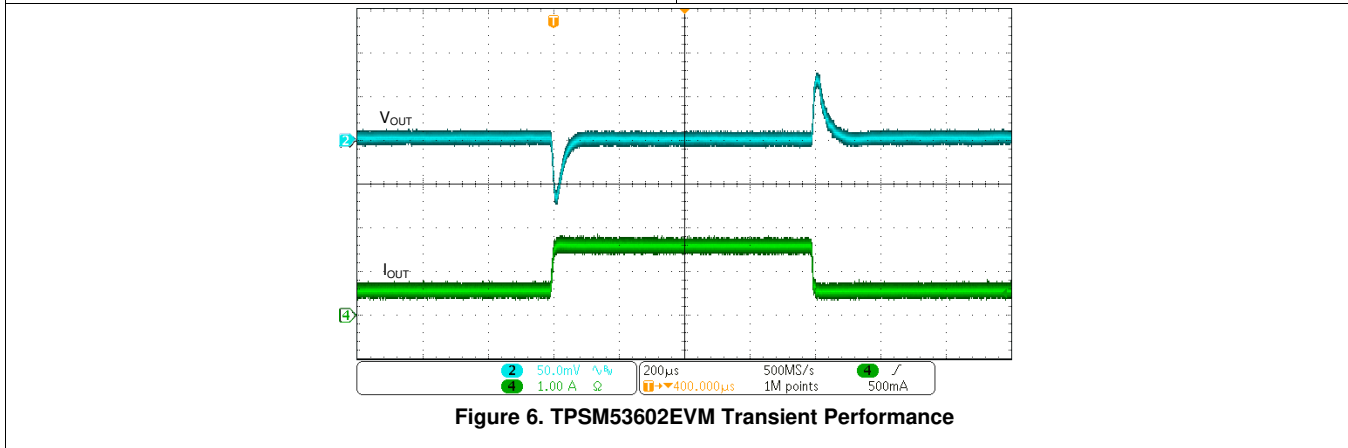
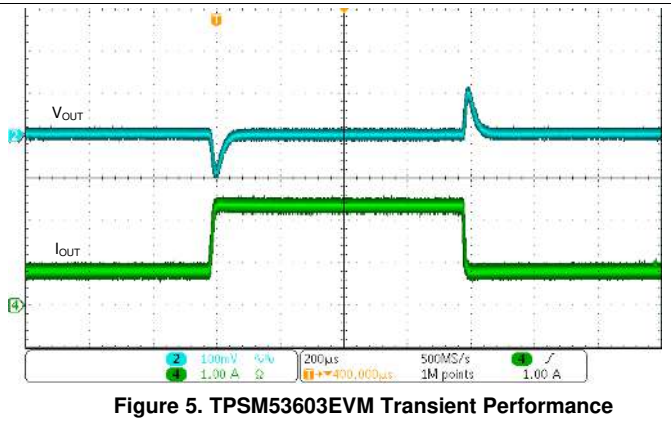
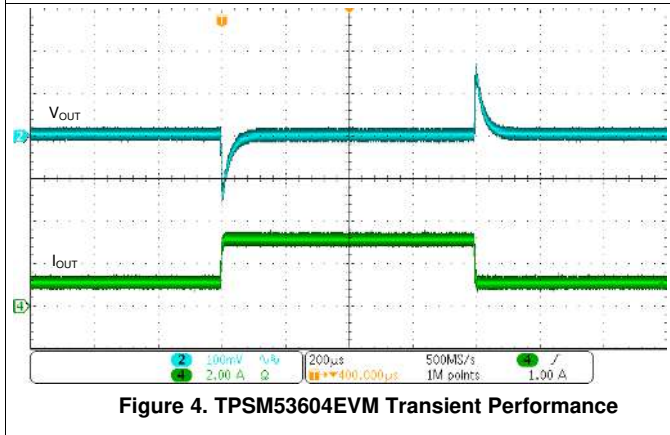
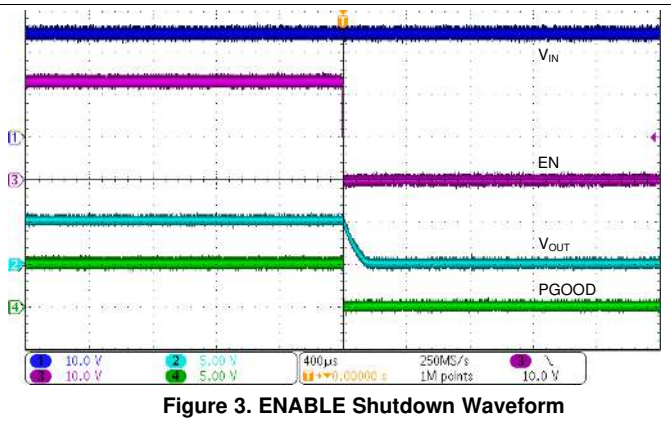
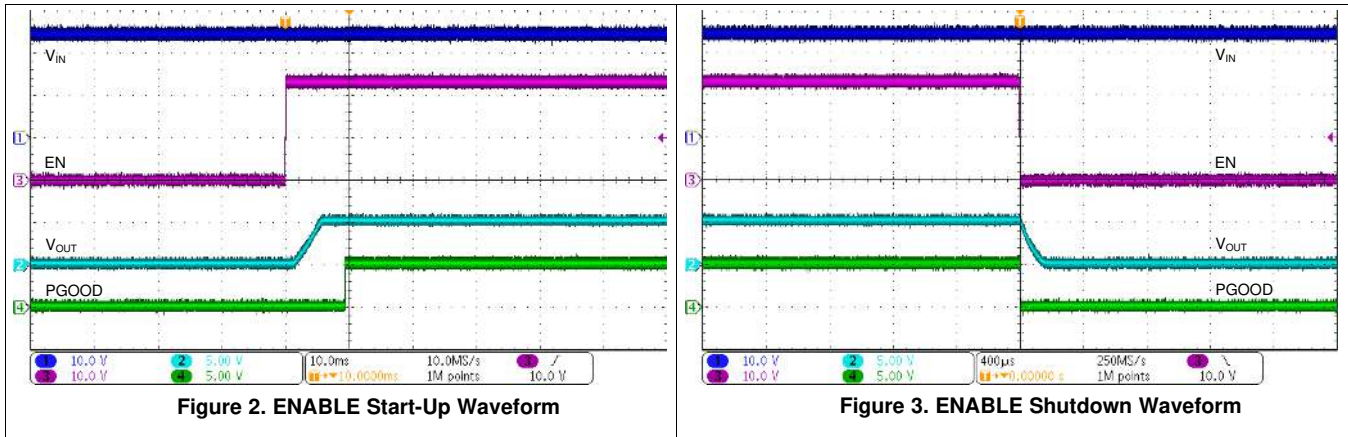
Table 1. Test Point Descriptions⁽¹⁾

VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S-	Input ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT S+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT S-	Output ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
AGND	Ground test point. Connect the negative lead of a DVM to this point when measuring efficiency, line regulation, and load regulation.
VIN Scope (J2)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT Scope (J3)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output voltage ripple and transient response.
EN	Enable test point. Monitor or control the Enable signal using this test point.
ENABLE Control (J5)	Enable select jumper. Enable or disable the device using a jumper.
PGOOD	Power-good test point. Monitors the power good signal of the device. This is an open-drain signal. A 49.9-k Ω resistor is connected to this pin and the PG_PU pin on the EVM.
PG_PU	PGOOD pullup test point. Apply a voltage to this pin to use as a pullup voltage for the PGOOD signal. A 49.9-k Ω resistor is connected to this pin and the PGOOD pin on the EVM.

⁽¹⁾ Refer to the product data sheet for absolute maximum ratings associated with the above features.

3 Performance Data

Figure 2 and Figure 3 demonstrate the enable ON/OFF performance of the EVM. See Figure 4 through Figure 6 for transient response waveforms (25% to 75% load step) associated with each EVM. The default output capacitance configured on the EVM is optimized for an output voltage of 5.0 V and 3.3 V. The additional output capacitor footprints, C7, C8, and C11, are available on the EVM if an improved load transient response or output voltage ripple is needed. See the [TPSM53604 3.8-V to 36-V Input, 1-V to 7-V Output, 4-A Power Module Data Sheet](#), [TPSM53603 3.8-V to 36-V Input, 1-V to 6-V Output, 3-A Power Module Data Sheet](#), or [TPSM53602, 3.8 V to 36 V Input, 1 V to 6 V Output, 2-A Power Module Data Sheet](#) for more information on the respective devices.



4 EVM Board Physical Specifications

This section describes the physical layout of the EVM board, the schematic, and the bill of materials (BOM).

4.1 Board Layout

The EVM board dimensions are 64 mm × 83 mm. [Figure 7](#) through [Figure 12](#) show the EVM board layers.

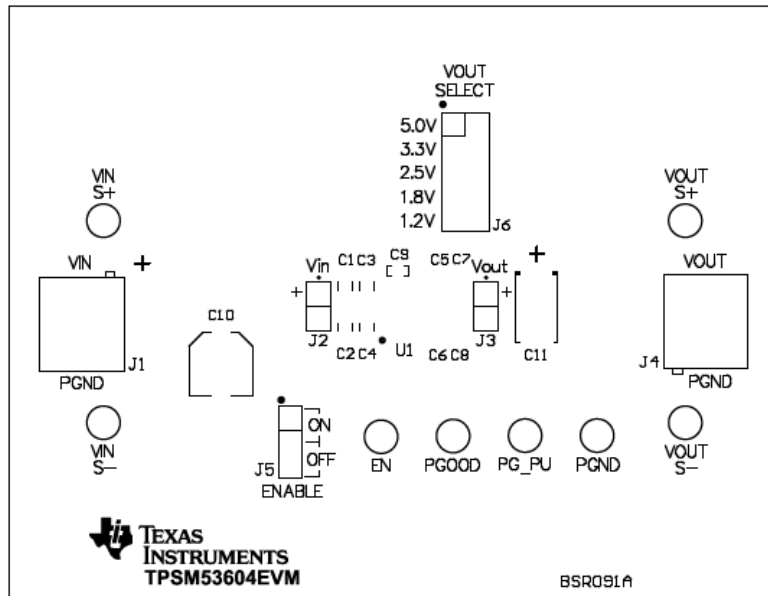


Figure 7. Top Silk Screen (Top View)

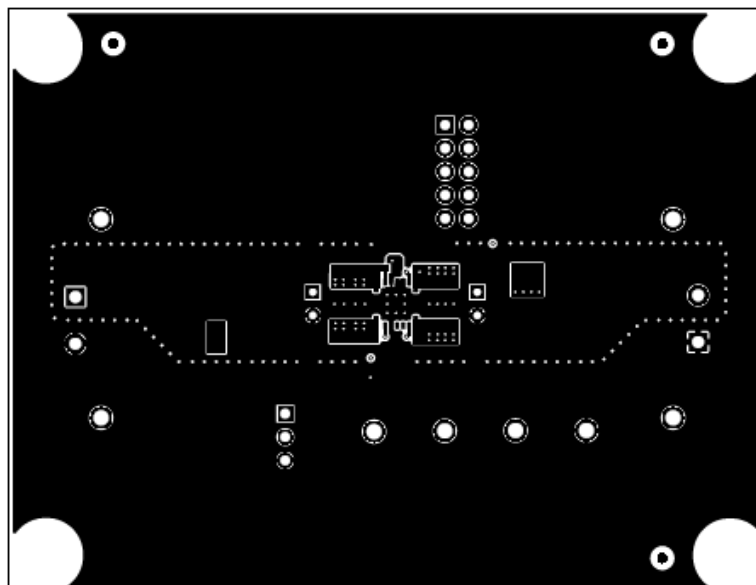


Figure 8. Top Copper Layer

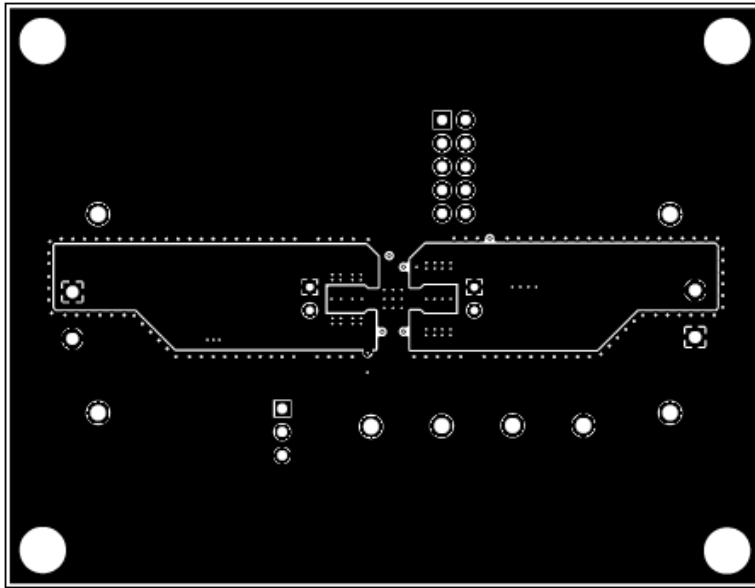


Figure 9. Signal Layer 1

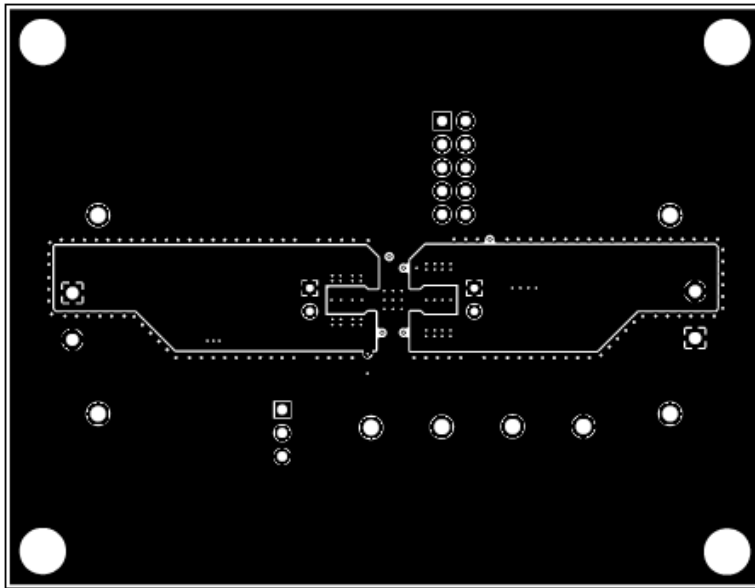


Figure 10. Signal Layer 2

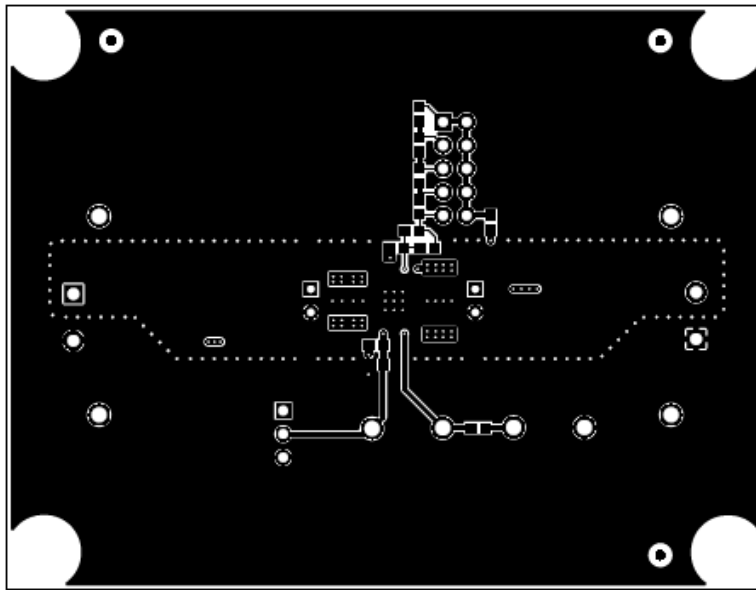


Figure 11. Signal Layer 3

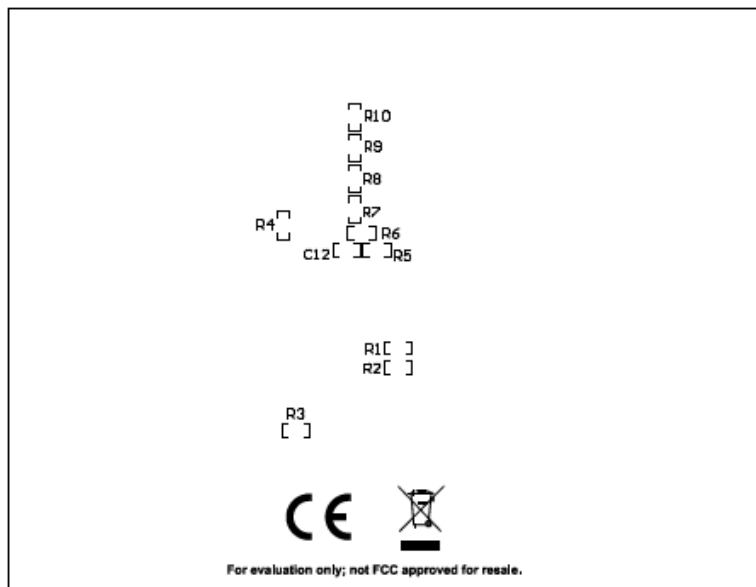


Figure 12. Bottom Layer Silk Screen (Bottom View)

4.2 EVM Schematic

Figure 13 shows the TPSM53604EVM schematic. The schematic for the TPSM53603EVM and TPSM53602EVM is identical with the only difference being the U1 IC.

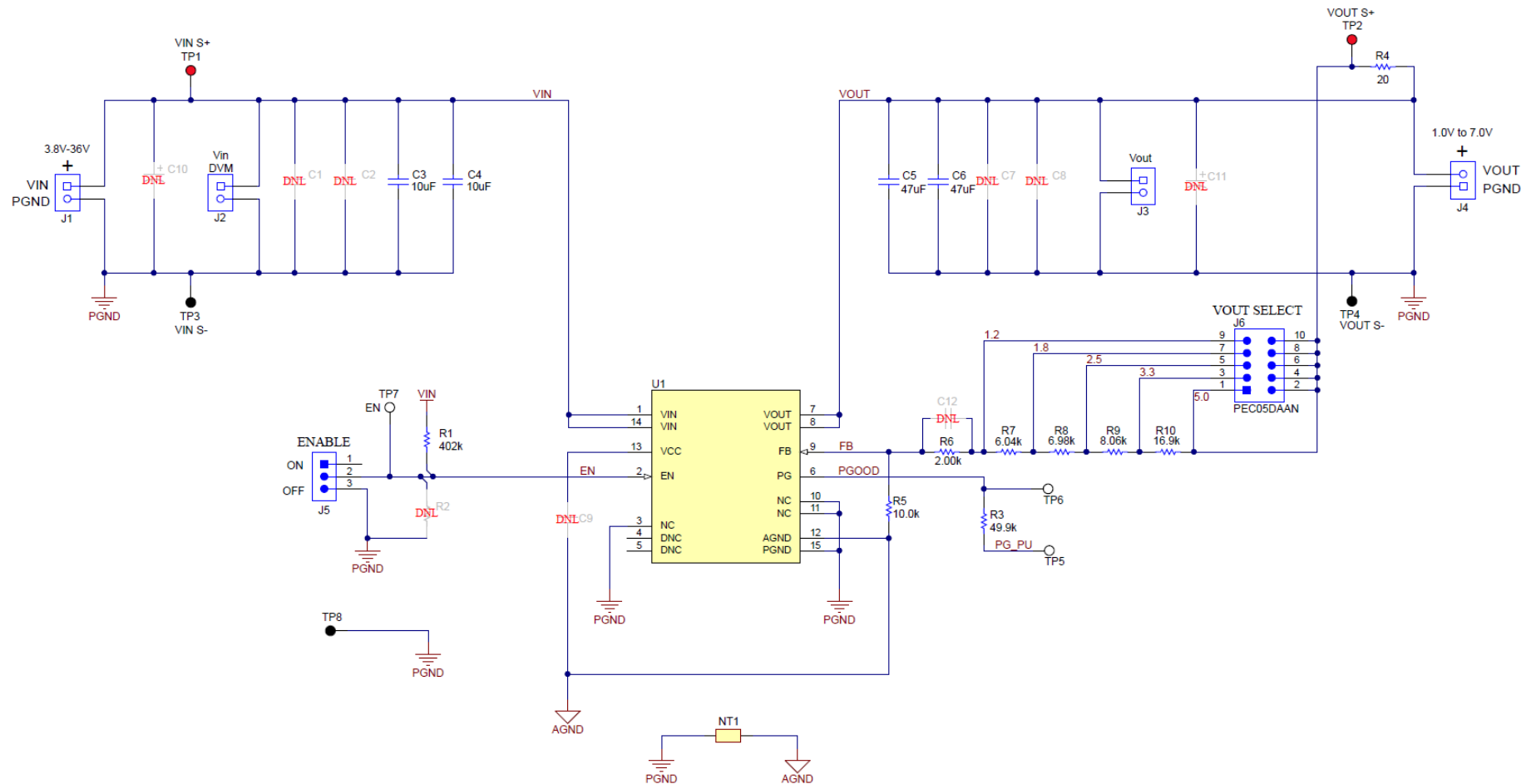


Figure 13. TPSM53604EVM Schematic

4.3 Bill of Materials (BOM)

Table 2 shows the EVM BOM.

Table 2. EVM BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER
C3, C4	2	10 μ F	CAP, CERM, 10 μ F, 50 V	1206	CGA5L3X5R1H106M160AB
C5, C6	2	47 μ F	CAP, CERM, 47 μ F, 10 V	0805	C2012X5R1A476M125AC
J1, J4	2		Terminal Block, 5.08 mm, 2x1	2x1 5.08 mm	ED120/2DS
J2, J3	2		Socket Strip, 2x1, 100 mil, Black, Tin, TH	Socket Strip, 100 mil, 2pin	310-43-102-41-001000
J5	1		Header, 100 mil, 3x1, Tin, TH	Header, 3 PIN, 100 mil	PEC03SAAN
J6	1		Header, 100 mil, 5x2, Tin, TH	Header, 5x2, 100 mil	PEC05DAAN
R1	1	402 k	RES, 402 k, 1%, 0.1 W	0603	CRCW0603402KFKEA
R3	1	49.9 k	RES, 49.9 k, 1%, 0.1 W	0603	CRCW060349K9FKEA
R4	1	20	RES, 20, 5%, 0.1 W	0603	CRCW060320R0JNEA
R5	1	10.0 k	RES, 10.0 k, 1%, 0.1 W	0603	CRCW060310K0FKEA
R6	1	2.00 k	RES, 2.00 k, 1%, 0.1 W	0603	CRCW06032K00FKEA
R7	1	6.04 k	RES, 6.04 k, 1%, 0.1 W	0603	CRCW06036K04FKEA
R8	1	6.98 k	RES, 6.98 k, 1%, 0.1 W	0603	CRCW06036K98FKEA
R9	1	8.06 k	RES, 8.06 k, 1%, 0.1 W	0603	CRCW06038K06FKEA
R10	1	16.9 k	RES, 16.9 k, 1%, 0.1 W	0603	CRCW060316K9FKEA
TP1, TP2	2		Test Point, Multipurpose, Red		5010
TP3, TP4, TP8	3		Test Point, Multipurpose, Black		5011
TP5, TP6, TP7	3		Test Point, Multipurpose, White		5012
U1	1		36-V, 4-A, Power Module	RDA0015A	TPSM53604RDA
			36-V, 3-A, Power Module		TPSM53603RDA
			36-V, 2-A, Power Module		TPSM53602RDA
Not Loaded					
C1, C2	0			1206	
C7, C8, C10	0			0805	
C9	0			0402	
C11	0			7343-40	
C12	0			0603	
R2	0			0603	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2019) to B Revision Page

- Added information on additional output capacitor footprints C7, C8, and C11..... 5
-

Changes from Original (November 2019) to A Revision Page

- Added the TPSM53603 and TPSM53602 to the user's guide..... 1
 - Added [Figure 5](#) and [Figure 6](#) 5
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