General Description

The DA16200 is a highly integrated ultra-low power Wi-Fi system on a chip (SoC), which contains an 802.11b/g/n radio (PHY), a baseband processor, a media access controller (MAC), on-chip memory, and a host networking application processor, all on a single silicon die.

The SoC enables full offload capabilities, running the entire networking stack on chip so that no external network processor, CPU, or microcontroller is required, while many other SoCs optionally use a microcontroller.

DA16200 is a synthesis of breakthrough ultra-low power technologies that enables extremely low power operation in the SoC. DA16200 shuts down every micro element of the chip that is not in use, which allows a near zero level of power consumption when not actively transmitting or receiving data. Such low power operation can extend the battery life up to a year or more depending on the application. DA16200 also enables ultra-low power transmitting and receiving modes when the SoC needs to be awake to exchange information with other devices. Advanced algorithms enable staying asleep until the exact moment required to wake up to transmit or receive.

The SoC is built from the ground up for the Internet of Things (IoT) and is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video doorbells, wearables, and other IoT devices.

Key Features

- Highly integrated ultra-low power Wi-Fi® system on chip
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
  - IEEE 802.11b/g/n, 1×1, 20 MHz channel bandwidth, 2.4 GHz
  - IEEE 802.11s Wi-Fi mesh
  - On-chip PA, LNA, and RF switch
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station, Soft AP, and Wi-Fi Direct® Modes (GO, GC, GO fixed)
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Connection manager for autonomous and fast Wi-Fi connections
  - Bluetooth coexistence
  - Antenna switching diversity
- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: single-ended four channels
- Direct code execution from the external serial flash memory (XIP)
  - Provides dynamic auto switching function
- Supports various interfaces
  - eMMC/SD expanded memory
  - SDIO Host/Slave function
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- Wi-Fi Alliance certifications:
  - Wi-Fi CERTIFIED™ b, g, n
  - WPA™ - Enterprise, Personal
  - WPA2™ - Enterprise, Personal
  - WPA3™ - Enterprise, Personal
  - Wi-Fi Direct
  - Wi-Fi Enhanced Open™
  - WMM
  - WMM - Power Save
  - Wi-Fi Protected Setup™
- CPU core subsystem
  - Arm® Cortex®-M4F core w/ clock frequency of 30~160 MHz
  - ROM: 256 kB

- Hardware accelerators
  - General HW CRC engine
  - HW zeroing function for fast booting
  - Pseudo random number generator (PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provides TCP/IP stack: in the form of network socket APIs
- Advanced security
  - Secure booting
  - Secure debugging using JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES (128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG
  - SRAM: 512 kB
  - OTP: 2 kB
  - Retention Memory: 48 kB
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Integrated DC-DC and LDOs
  - Supports three ultra-low power Sleep modes
- Clock source
  - 40 MHz crystal (± 20 ppm) for master clock (initial + temp + aging)
  - 32.768 kHz crystal (± 250 ppm) for RTC clock
  - Integrated 32 kHz RC oscillator
- Supply
  - Single operating voltage: 2.1 V to 3.6 V (typical: 3.3 V)
  - Digital I/O Supply Voltage: 1.8 V / 3.3 V
  - Black-out and brown-out detector
- Package type
  - 6 mm × 6 mm, 0.4 mm pitch, 48-Pin, QFN
  - 3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP
- Operating temperature range
  - -40 °C to 85 °C

Applications

- Security systems
- Door locks
- Thermostats
- Garage door openers
- Blinds
- Lighting control
- Sprinkler systems
- Video camera security systems
- Smart appliances
- Video doorbell
- Asset tracker

System Diagram

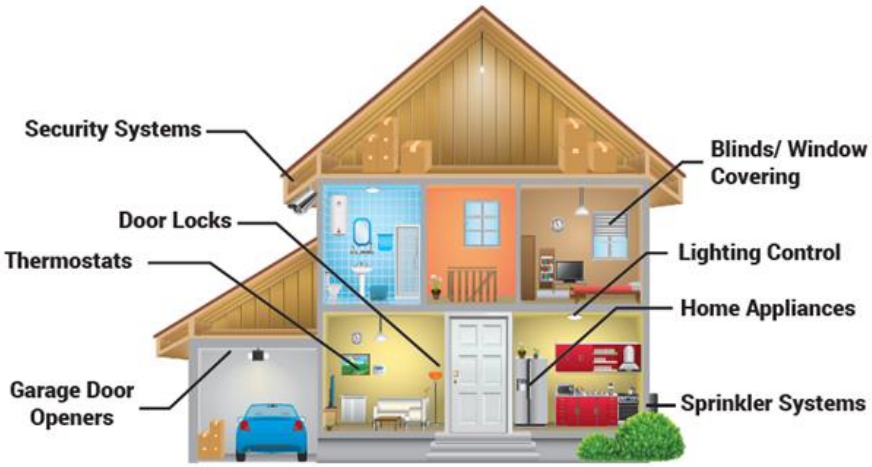

Figure 1: System Diagram

Contents

Figures

Tables

1 Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
HW	Hardware
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-Dropout Regulator
LLI	Linked-List Item
NVIC	Nested Vectored Interrupt Controller
NVRAM	Non-Volatile RAM
PLL	Phase-Locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-Lane SPI
RTC	Real-Time Clock
SAR ADC	Successive Approximation Analog-to-Digital Converter
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
TAP	Test Access Port
UART	Universal Asynchronous Receivers and Transmitter
XIP	eXecute in Place

2 References

[1] ARM Cortex M4 Processor Technical Reference Manual

[2] UM-WI-046, DA16200 DA16600, FreeRTOS SDK Programmer Guide, User Manual, Renesas Electronics

[3] ITU-T O.150,General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996

[4] Arm TrustZone® CryptoCell-312, Software Integrators Manual, Revision r1p1.

[5] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture

[6] AMBA AHB Bus Specification, Revision 3.0
https://developer.arm.com/documentation/ihi0033/bb

3 Block Diagram

Figure 2 shows the DA16200 hardware (HW) block diagram.

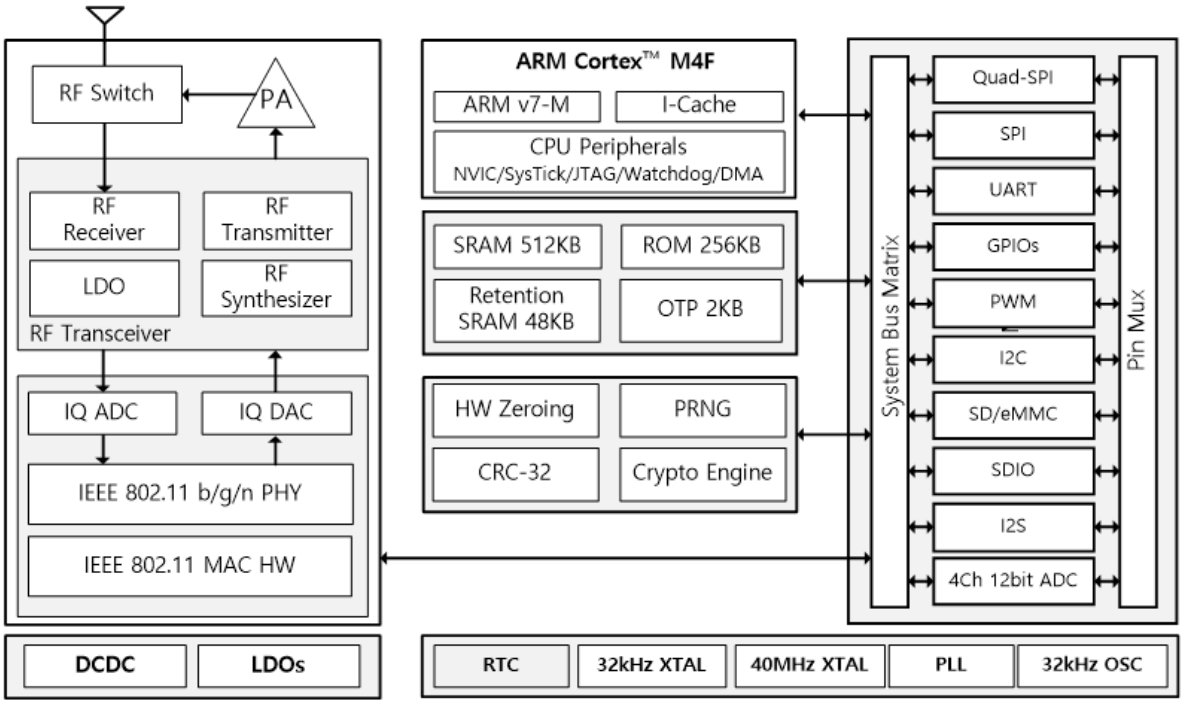

Figure 2: Hardware Block Diagram

Figure 3 shows the DA16200 software (SW) block diagram.

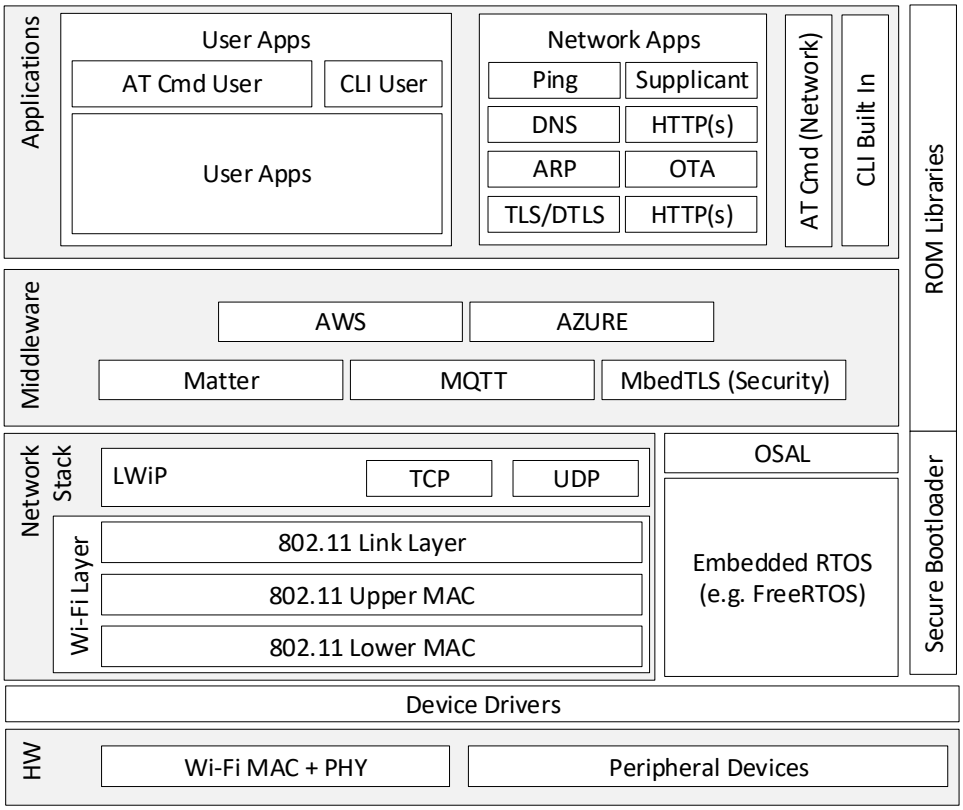

Figure 3: Software Block Diagram

The following descriptions are about the SW block diagrams:

- Kernel layer
  - Real Time Operating System
- The Network Stack layer is divided into four layers:
  - Lower MAC
    - SW module to control/handle HW Wi-Fi MAC/PHY and interfaces with Upper MAC layer
  - Upper MAC
    - SW module to control/handle Wi-Fi control/handle to interface with supplicant
    - Wi-Fi Link layer: Interface layer between Upper MAC and supplicant
    - Supplicant: SW module to control/management to operate Wi-Fi operation
  - Network subsystem layer
    - Used to control/handle network operation
    - Main protocols are IP, TCP, and UDP
    - Other necessary protocols are supported
  - Security layer
    - Crypto operation engine is ported to use crypto HW engine
- TLS/TCP and DTLS/UDP APIs are supported to handle security operation:
  - User application layer
    - Various sample code is available in the SDK – the sample code shows how to use the supported APIs
    - TCP Client/Server, UDP Client/Server, TLS Client/Server
    - HTTP/HTTPs download, OTA Update usage, and MQTT usage

Customer applications can be included and implemented easily in the SDK.

4 Pinout

4.1 48-Pin QFN

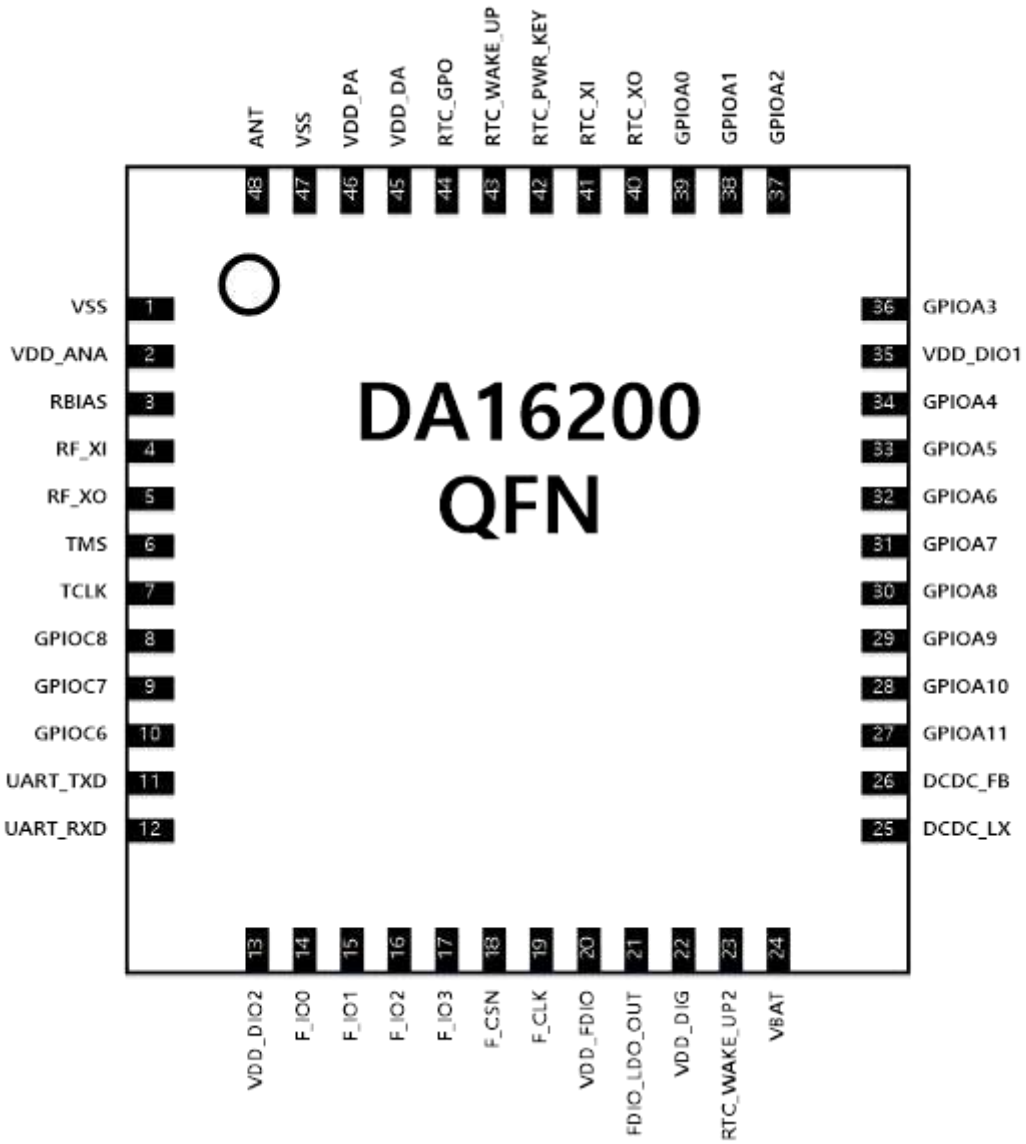

Figure 4: DA16200 QFN48 Pinout Diagram (Top View)

4.2 72-Pin fcCSP

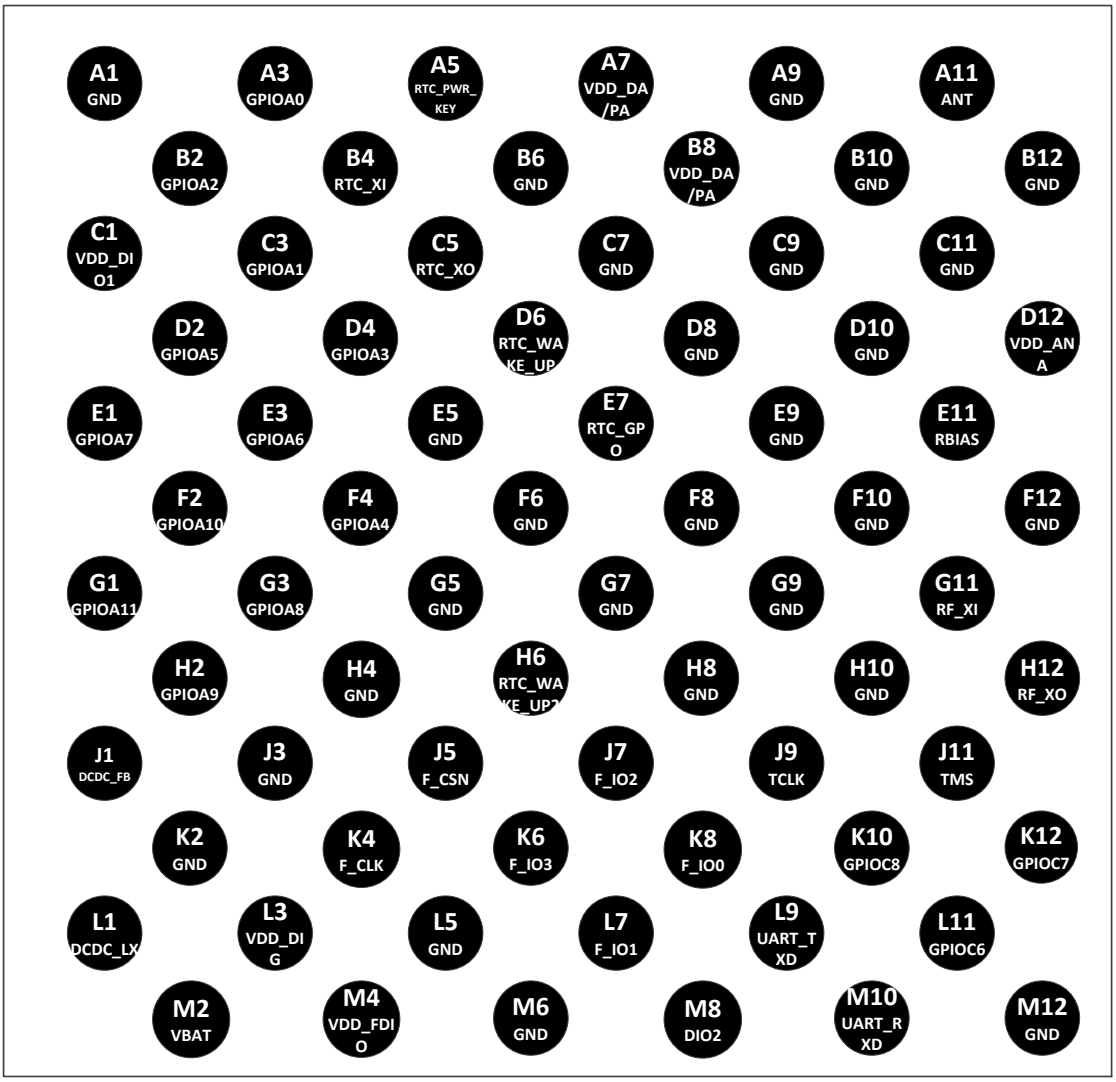

Figure 5: DA16200 fcCSP72 Pinout Diagram (Top View)

Table 1: Pin Description

QFN #Pin	fcCSP #Pin	Pin Name	Type (Table 2)	Drive (mA)	Initial State (Note 1)	Description
1		GND	GND			Ground
2	D12	VDD_ANA	VDD			RF VDD
3	E11	RBIAS	AIO			External reference resistor pin
4	G11	RF_XI	AI			40 MHz crystal clock input
5	H12	RF_XO	AO			40 MHz crystal clock output
6	J11	TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
7	J9	TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
8	K10	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
9	K12	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
10	L11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
11	L9	UART_TXD	DO	2/4/8/12	O	UART transmit data
12	M10	UART_RXD	DI	2/4/8/12	I	UART receive data
13	M8	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
14	K8	F_IO0	DIO			External Flash Memory I/F
15	L7	F_IO1	DIO			External Flash Memory I/F
16	J7	F_IO2	DIO			External Flash Memory I/F
17	K6	F_IO3	DIO			External Flash Memory I/F
18	J5	F_CSN	DIO			External Flash Memory I/F
19	K4	F_CLK	DIO			External Flash Memory I/F
20	M4	VDD_FDIO	VDD			Flash IO Power
21		FDIO_LDO_OUT	AIO			Flash and IO LDO output and connect to external cap. For flash LDO
22	L3	VDD_DIG	VDD			Digital power and connect to external cap. For DIG LDO
23	H6	RTC_WAKE_UP2	DI		DI (Note 2)	RTC block wake-up signal
24	M2	VBAT	VDD			Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO			Connection from power MOSFETs to the Inductor in internal DCDC
26	J1	DCDC_FB	AIO			Feedback voltage from the output of the power supply in internal DCDC
27	G1	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
28	F2	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
29	H2	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
30	G3	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
31	E1	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O

QFN #Pin	fcCSP #Pin	Pin Name	Type (Table 2)	Drive (mA)	Initial State (Note 1)	Description
32	E3	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
33	D2	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
34	F4	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
35	C1	VDD_DIO1	VDD			Supply power for digital I/O GPIOA0~GPIOA11
36	D4	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
37	B2	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
38	C3	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
39	A3	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
40	C5	RTC_XO	AO		AO	32.768 kHz crystal clock output
41	B4	RTC_XI	AI		AI	32.768 kHz crystal clock input
42	A5	RTC_PWR_KEY	DI		DI	RTC block enable signal
43	D6	RTC_WAKE_UP	DI		DI (Note 2)	RTC block wake-up signal
44	E7	RTC_GPO	DO		DO	General Purpose Output
45	A7, B8	VDD_DA	VDD			Tx DA power and RTC block power
46		VDD_PA	VDD			Supply power for integrated power amplifier
47		GND	GND			Ground
48	A11	ANT	AI			ANT
fcCSP GND Pin A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, E5, E9, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12						

Note 1 Status of RTC_PWR_KEY is asserted and digital power (VDD_DIG) is stable.

Note 2 In the case where this pin is used, an external pull-down resistor is needed and if the pin is not used it should remain open.

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PU	Pull-up resistor (fixed)	GND	Ground
PU	Pull-up resistor (fixed)	PD	Pull-down resistor (fixed)

4.3 Pin Multiplexing

The DA16200 provides various IO interfaces to support many kinds of applications. To reduce the number of external pins required, the DA16200 uses pin multiplexing to assign these IO interfaces to specific pins as shown in Table 3 and Table 4. There are 16 general purpose pins, each of which can be assigned alternate functions. There are four GPIO pins, GPIOA0 to GPIOA3, which support multiplexing with analog signals. See Table 131 and Table 132 for details on how to configure the pin functions.

Table 3: DA16200 Pin Multiplexing

Pin	JTAG	Analog	SPI Master	SPI Slave	I2C Master	I2C Slave	SDIO Slave	SDeMMC
GPIOA0		CH0		SPI_MISO	I2C_SDA	I2C_SDA		Note 1
GPIOA1		CH1		SPI_MOSI	I2C_CLK	I2C_CLK		SD/eMMC_WRP
GPIOA2		CH2		SPI_CSB		I2C_SDA		
GPIOA3		CH3		SPI_CLK		I2C_CLK		
GPIOA4					I2C_SDA	I2C_SDA	SDIO_CMD	SD/eMMC_CMD
GPIOA5					I2C_CLK	I2C_CLK	SDIO_CLK	SD/eMMC_CLK
GPIOA6			E_SPI_CSB	SPI_CSB		I2C_SDA	SDIO_D3	SD/eMMC_D3
GPIOA7			E_SPI_CLK	SPI_CLK		I2C_CLK	SDIO_D2	SD/eMMC _D2
GPIOA8			E_SPI_DIO0 / E_SPI_MOSI	SPI_MISO	I2C_SDA		SDIO_D1	SD/eMMC _D1
GPIOA9			E_SPI_DIO1 / E_SPI_MISO	SPI_MOSI	I2C_CLK		SDIO_D0	SD/eMMC _D0
GPIOA10			E_SPI_DIO2	SPI_MISO				SD/eMMC_WRP
GPIOA11			E_SPI_DIO3	SPI_MOSI				
TCLK/GPIOA15	TCLK							
TMS	TMS							
UART_TXD								
UART_RXD								
GPIOC8	TDI							
GPIOC7	TDO							
GPIOC6	NTRST							

Note 1 Analog input pin function

Table 4: DA16200 Pin Multiplexing (Continued)

Pin	BT Coex.	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin State (nRESET=0)	Driving Strength (Default: 8mA)
GPIOA0		I2S_BCLK		UART1_TXD		Yes	I-PD	2/4/8/12mA
GPIOA1		I2S_MCLK		UART1_RXD		Yes	I-PD	2/4/8/12mA
GPIOA2		I2S_SDO	Note 1	UART1_TXD		Yes	I-PD	2/4/8/12mA
GPIOA3		I2S_LRCK	I2S_CLK_IN	UART1_RXD		Yes	I-PD	2/4/8/12mA
GPIOA4		I2S_BCLK		UART1_TXD / UART1_RTS		No	I-PD	2/4/8/12mA
GPIOA5		I2S_MCLK		UART1_RXD / UART1_CTS		No	I-PD	2/4/8/12mA
GPIOA6		I2S_SDO		UART1_TXD		No	I-PD	2/4/8/12mA
GPIOA7		I2S_LRCK		UART1_RXD		No	I-PD	2/4/8/12mA
GPIOA8	BT_SIG0	I2S_BCLK				No	I-PD	2/4/8/12mA
GPIOA9	BT_SIG1	I2S_MCLK				No	I-PD	2/4/8/12mA
GPIOA10	BT_SIG2		I2S_CLK_IN		UART2_TXD	No	I-PD	2/4/8/12mA
GPIOA11					UART2_RXD	No	I-PD	2/4/8/12mA
TCLK/GPIOA15						No	I-PD	2/4/8/12mA
TMS						No	I-PU	2/4/8/12mA

Pin	BT Coex.	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin State (nRESET=0)	Driving Strength (Default: 8mA)
UART_TXD						No	O	2/4/8/12mA
UART_RXD						No	I	2/4/8/12mA
GPIOC8						No	I-PD	2/4/8/12mA
GPIOC7					UART2_RXD	No	I-PD	2/4/8/12mA
GPIOC6					UART2_TXD	No	I-PD	2/4/8/12mA

Note 1 Analog input pin function

5 Electrical Specification

5.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Parameter	QFN Pins	fcCSP Pins	Min	Max	Units
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2, A7, B8	-0.2	3.7	V
VDD_DIO1	35	C1	-0.2	3.7	V
VDD_DIO2	13	M8	-0.2	3.7	V
VDD_FDIO	20	M4	-0.2	3.7	V
FDIO_LDO_OUT	21	-	-0.2	3.7	V
VDD_DIG	22	L3	-0.1	1.22	V
VDD_ANA	2	D12	-0.1	1.55	V
Operating temperature range (TA)			-40	+85	°C
Storage temperature range			-40	+150	°C

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	QFN Pins	fcCSP Pins	Min	Typ	Max	Units
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2, A7, B8 (Note 1)	2.1		3.6	V
VDD_DA, VDD_PA	-	A7, B8 (Note 2)		1.45		V
VDD_DIO1	35	C1	1.62		3.6	V
VDD_DIO2	13	M8	1.62		3.6	V
VDD_FDIO	20	M4	1.62		3.6	V
FDIO_LDO_OUT	21	-	1.62		1.92	V
VDD_DIG	22	L3		1.1		V
VDD_ANA	2	D12		1.37 (Note 2)		V
Operating temperature range (TA)			-40		+85	°C

Note 1 QFN, fcCSP Normal power mode.

Note 2 fcCSP Low power mode.

5.3 Electrical Characteristics

5.3.1 DC Parameters for Normal GPIOs

Table 7: DC Parameters for Normal GPIOs, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic High level	0.7 × DVDD		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.2 × DVDD	V
Output High Voltage	V_{OH}	DVDD=Min.	0.8 × DVDD		DVDD	V
Pull-up Resistor	R_{PU}	$V_{PAD}=V_{IH}$, DIO=Min.			32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=VIL, DIO=Min.			32.4	

(DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level)

Table 8: DC Parameters for Normal GPIOs, 3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.8	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.0		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.4	V
Output High Voltage	V_{OH}	DVDD=Min.	2.4		DVDD	V
Pull-up Resistor	R_{PU}	VPAD=VIH, DIO=Min.			19.4	kΩ
Pull-down Resistor	R_{PD}	$V_{PAD}=V_{IL}$, DIO=Min.			16.0	

(DVDD= 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level)

5.3.2 DC Parameters for RTC Block

There are several control pins in the RTC block. For details, see Section 7.4.

Table 9: DC Parameters for RTC Block, 3.3 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.6	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.3		VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

Table 10: DC Parameters for RTC Block, 2.1 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.6		VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

5.3.3 DC Parameters for Digital Wake-Up

Several GPIOs can be used for wake-up. For details, see Section 7.4.1.

To use Digital Wake-up, the IO voltage should not be higher than the VBAT value.

Table 11: DC Parameters for Digital Wake-Up, 3.3 V VBAT and 1.8/3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.5	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.4		DVDD	V

(DVDD= 1.8/3.3 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be higher than the VBAT value)

Table 12: DC Parameters for Digital Wake-Up, 2.1 V VBAT and 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.3		DVDD	V

(DVDD= 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be higher than the VBAT value)

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

TA = +25 °C, VBAT = 3.3 V. Parameters are measured at ANT pin on CH1 (2412 MHz).

Table 13: WLAN Receiver Characteristics – QFN

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	1 Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2 Mbps DSSS	-96	-95	-93	
	11 Mbps CCK	-91	-90	-88	
	6 Mbps OFDM	-92	-91	-89	
	9 Mbps OFDM	-92	-91	-89	
	18 Mbps OFDM	-90	-89	-87	
	36 Mbps OFDM	-83	-82	-80	
	54 Mbps OFDM	-77	-76	-74	
	MCS0(GF)	-92	-91	-89	
	MCS7(GF)	-74	-73	-71	
Maximum input level (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

Table 14: WLAN Receiver Characteristics – fcCSP

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	1Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2Mbps DSSS	-96	-95	-93	
	11Mbps CCK	-91	-90	-88	
	6Mbps OFDM	-92	-91	-89	
	9Mbps OFDM	-92	-91	-89	
	18Mbps OFDM	-90	-89	-87	
	36Mbps OFDM	-83	-82	-80	
	54Mbps OFDM	-77	-76	-74	
	MCS0(GF)	-92	-91	-89	
	MCS7(GF)	-74	-73	-71	
Maximum input level (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

5.4.2 WLAN Transmitter Characteristics

TA = +25 °C, VBAT = 3.3 V. Parameters are measured at ANT pin on CH1 (2412 MHz).

Table 15: WLAN Transmitter Characteristics – QFN

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured from IEEE spectral mask and EVM	1 Mbps DSSS	17.5	20.0	21.0	dBm
	2 Mbps DSSS	17.5	20.0	21.0	
	5.5 Mbps CCK	17.5	20.0	21.0	
	11 Mbps CCK	17.5	20.0	21.0	
	6 Mbps OFDM	16.5	19.0	20.0	
	9 Mbps OFDM	16.5	19.0	20.0	
	12 Mbps OFDM	16.5	19.0	20.0	
	18 Mbps OFDM	16.5	19.0	20.0	
	24 Mbps OFDM	15.5	18.0	19.0	
	36 Mbps OFDM	15.5	18.0	19.0	
	48 Mbps OFDM	14.0	16.5	17.5	
	54 Mbps OFDM	13.0	15.5	16.5	
	MCS0 OFDM	16.5	19.0	20.0	
	MCS7 OFDM	13.0	15.5	16.5	
Transmit center frequency accuracy		-20		+20	ppm

Table 16: WLAN Transmitter Characteristics – fcCSP (Normal Power Mode)

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	16.0	18.5	19.5	dBm
	2 Mbps DSSS	16.0	18.5	19.5	
	5.5 Mbps CCK	16.0	18.5	19.5	
	11 Mbps CCK	16.0	18.5	19.5	
	6 Mbps OFDM	15.5	18.0	19.0	
	9 Mbps OFDM	15.5	18.0	19.0	
	12 Mbps OFDM	15.5	18.0	19.0	
	18 Mbps OFDM	15.5	18.0	19.0	
	24 Mbps OFDM	14.5	17.0	18.0	
	36 Mbps OFDM	14.5	17.0	18.0	
	48 Mbps OFDM	13.0	15.5	16.5	
	54 Mbps OFDM	12.0	14.5	15.5	
	MCS0 OFDM	15.5	18.0	19.0	
	MCS7 OFDM	12.0	14.5	15.5	
Transmit center frequency accuracy		-20		+20	ppm

Table 17: WLAN Transmitter Characteristics – fcCSP (Low Power Mode)

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	7.5	9.5	10.5	dBm
	2 Mbps DSSS	7.5	9.5	10.5	
	5.5 Mbps CCK	7.5	9.5	10.5	
	11 Mbps CCK	7.5	9.5	10.5	
	6 Mbps OFDM	6.0	8.0	9.0	
	9 Mbps OFDM	6.0	8.0	9.0	
	12 Mbps OFDM	6.0	8.0	9.0	
	18 Mbps OFDM	6.0	8.0	9.0	
	24 Mbps OFDM	3.5	5.5	6.5	
	36 Mbps OFDM	3.5	5.5	6.5	
	48 Mbps OFDM	0	2.0	3.0	
	54 Mbps OFDM	0	2.0	3.0	
	MCS0 OFDM	6.0	8.0	9.0	
	MCS7 OFDM	0	2.0	3.0	
Transmit center frequency accuracy		-20		+20	ppm

5.5 Current Consumption

TA = +25 °C, VBAT = 3.3 V, w/ CPU clock 80 MHz.

Table 18: Current Consumption in Active State – QFN

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 20.0 dBm	260	280	320	mA
		6 Mbps OFDM	@ 19.0 dBm	240	260	300	
		54 Mbps OFDM	@ 15.5 dBm	180	200	240	
		MCS7	@ 15.5 dBm	180	200	240	
	RX	No signal (Note 1)		25	29	51	
		1 Mbps DSSS (Note 1)		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.6	54	

Note 1 Low Current Mode and CPU clock 30 MHz.

Table 19: Current Consumption in Active State – fcCSP (Normal Power Mode)

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 18.5 dBm	250	270	310	mA
		6 Mbps OFDM	@ 18.0 dBm	230	250	290	
		54 Mbps OFDM	@ 14.0 dBm	190	210	250	
		MCS7	@ 14.0 dBm	190	210	250	
	RX	No signal (Note 1)		25	28.4	51	
		1 Mbps DSSS (Note 1)		26.5	29.7	53	
		1 Mbps DSSS		27	36.5	54	
		54 Mbps OFDM		29	38	54	
		MCS7		29	38	54	

Note 1 Low Current Mode and CPU clock 30 MHz.

Table 20: Current Consumption in Active State – fcCSP (Low Power Mode)

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 9.5 dBm	63	85	100	mA
		6 Mbps OFDM	@ 8.0 dBm	63	85	100	
		54 Mbps OFDM	@ 2.0 dBm	48	70	90	
		MCS7	@ 2.0 dBm	48	70	90	
	RX	No signal (Note 1)		25	28.4	51	
		1 Mbps DSSS (Note 1)		26.5	29.7	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	39.2	54	
		MCS7		29	39.2	54	

Note 1 Low Current Mode and CPU clock 30 MHz.

Table 21: Current Consumption in Low Power Operation

Parameter	Condition	Min	Typ	Max	Units
Low Power Operation	Sleep 1		0.2		µA
	Sleep 2		1.8		
	Sleep 3		3.5		

5.6 ESD Ratings

Table 22: QFN Package

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

Table 23: fcCSP Package

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

5.7 Brown-Out and Black-Out

The device enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Table 24). This condition must be considered during design of the power supply routing, especially if the SoC is operated from a battery. High-current operations, like TX operation, cause a dip in the supply voltage, potentially triggering a Brown-Out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (for example, four contacts for two AA batteries), wiring resistance, and PCB routing resistance.

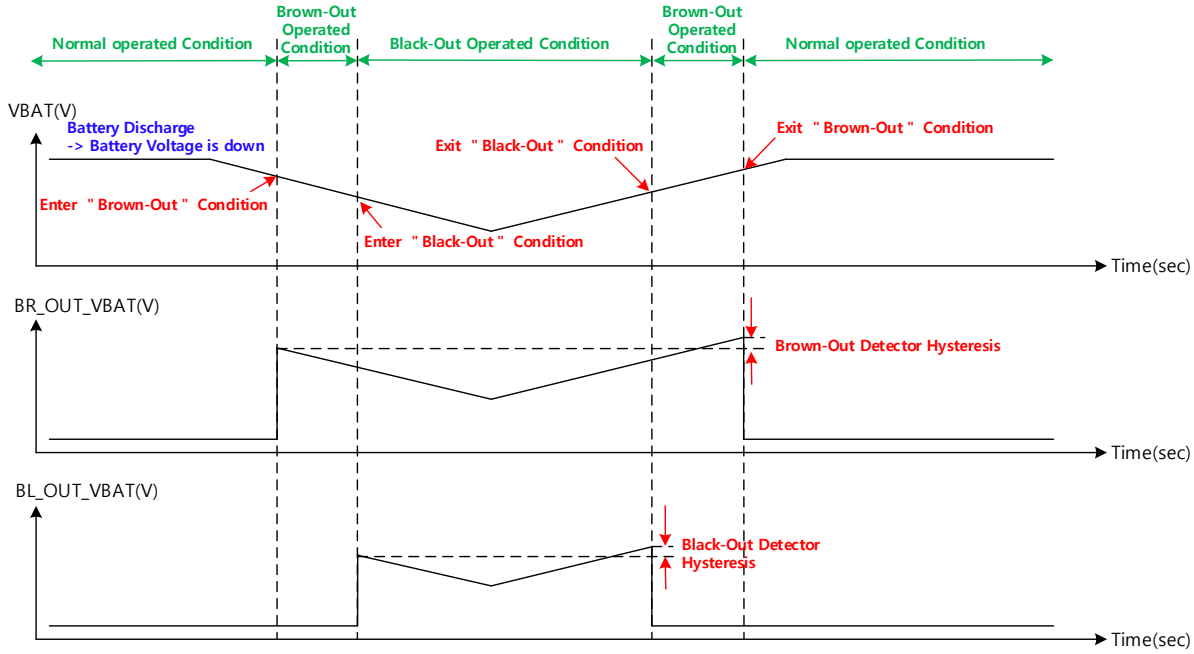

Figure 6: Brown-Out and Black-Out Levels

Brown-out and black-out conditions only operate in normal mode. The black-out condition is equivalent to a hardware reset event in which all states within the device are lost. Table 24 lists the brown-out and black-out voltage levels.

Table 24: Brown-Out and Black-Out Voltage Levels

Condition	Voltage	Hysteresis	Operation
Vbrown-out	2.10 V (Note 1)	90 mV	S/W Control
Vblack-out	1.75 V (Note 1)	90 mV	Full boot

Note 1 Recommended voltage level. Adjustable depending on the application condition.

5.8 Clock Electrical Characteristics

DA16200 needs two clock sources. One is the 32.768 kHz clock used by the RTC block, and the other is the 40 MHz clock for the internal processor and Wi-Fi system. More specifically, the 40 MHz clock is used as a source clock for the internal PLL, while the PLL output is used for the internal processor and Wi-Fi system block.

5.8.1 RTC Clock Source

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The RTC block of the SoC contains an internal 32.768 kHz RC oscillator as well, which is used as a clock for chip initialization before the external 32.768 kHz crystal reaches the stable time in the initial stage. It is necessary to convert it into an external clock for accurate clock counting after the initialization stage. This process is executed through the register setting. Table 25 shows the suitable loading

capacitor value and required tolerance. Figure 7 and Figure 8 show connections for the RTC crystal clock.

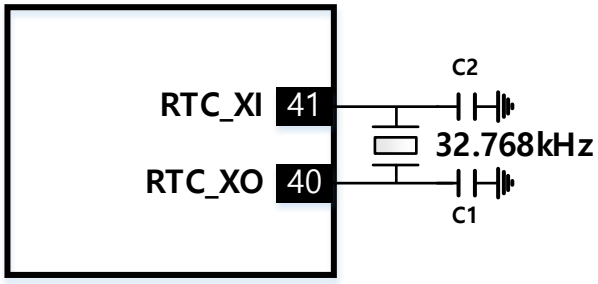

Figure 7: RTC Crystal Connections - QFN

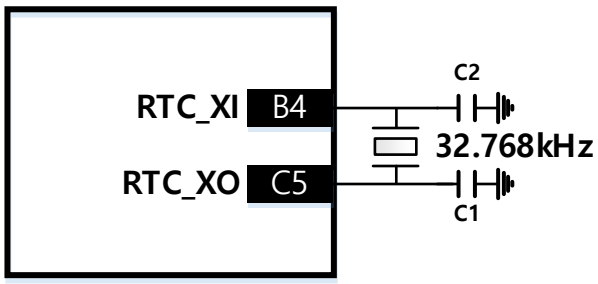

Figure 8: RTC Crystal Connections – fcCSP

Table 25 lists the RTC crystal requirements.

Table 25: RTC Crystal Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency			32.768		kHz
Frequency accuracy	Initial + temp + aging	-250		+250	ppm
Crystal ESR				100k	Ω
Load Capacitance			10		pF
Shunt Capacitance (Note 1)			15		pF

Note 1 There are no non-tunable capacitors inside.so, it must be adjusted using an external capacitor. External Shunt capacitors (C1, C2) have 15pF mounted on the DA16200 Module.

5.8.2 Main Clock Source

DA16200 contains a crystal oscillator for the main clock source which supports the external crystal clock. Basically, the external clock is 40 MHz. Table 26 shows the load capacitor value and required clock tolerance for 40 MHz. Figure 9 and Figure 10 show the crystal clock connections.

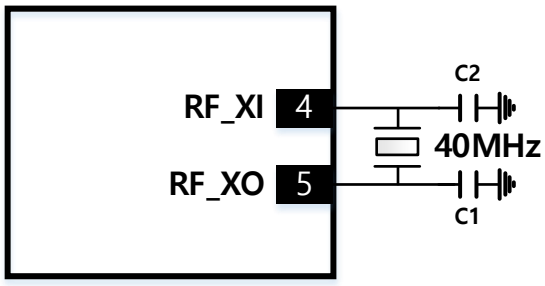

Figure 9: Crystal Clock Connections - QFN

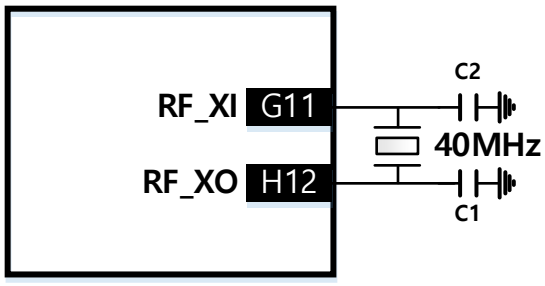

Figure 10: Crystal Clock Connections - fcCSP

Table 26 lists the WLAN crystal requirements.

Table 26: WLAN Crystal Clock Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency			40		MHz
Frequency accuracy	Initial + temp + aging	-20		+20	ppm
Crystal ESR				50	Ω
Load Capacitance (Note 1)		6	8	10	pF

Note 1 Not to exceed ±20ppm, there is an internal adjustable shunt capacitor inside the chipset, which must be written to the OTP block after X-TAL correction. There is a 0~12.7pF tunable capacitor inside the DA16200, to use without shunt capacitors outside, it must be selected an XTAL with a load capacitance of 6~10pF.

6 Power Management

DA16200 has an RTC block which provides power management and function control for low power operation. In normal operation, the RTC block is always powered on when RTC_PWR_KEY is enabled. The RTC block also has a control function for DA16200's internal power supplying components, like LDOs, DC-DCs, and power switches.

6.1 Power On Sequence

The sequence after the initial switching from power-off to power-on is shown in Figure 11.

The RTC_PWR_KEY of DA16200 is a pin that enables the RTC block. Once RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are turned on automatically in the sequence predefined by the RTC block.

Once RTC_PWR_KEY is turned on, LDOs for both XTAL and digital I/O are turned on shortly and then the DC-DC regulator is turned on according to the predefined interval. The enabling intervals can also be modified in the register settings after initial power-up.

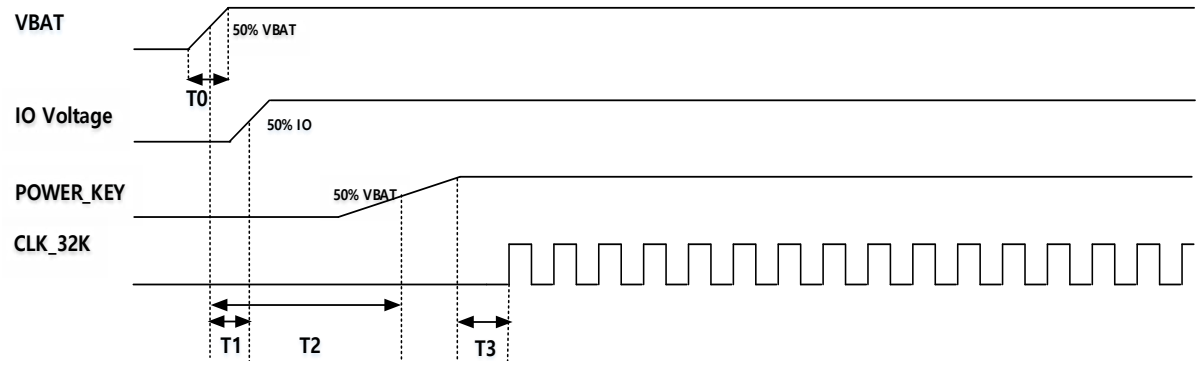

Figure 11: Power On Sequence

Table 27: Power On Sequence Timing Requirements

Name	Description	Min	Typ	Max	Unit
T0	VBAT power-on time from 10 % to 90 % of VBAT				ms
T1	IO voltage and VCC supply		0		ms
T2	RTC_PWR_KEY turn-on time from 50 % VBAT to 50 % POWER_KEY * Note 1		5*T0		ms
T3	Internal RC oscillator wake-up time		217		µs

Note 1 if the T0 = 10 ms to turn on VBAT, the recommended T2 is 50 ms for the safe booting operation. It would be externally controlled by MCU or it would be implemented using RC filter at the input of RTC_PWR_KEY. The recommended C is 470 nF or 1uF (not to exceed 1uF) and R value is chosen to have T2 delay. For example, R and C values will be 82 kΩ and 1 uF when T0 = 10 ms.

6.2 Power Management Unit

DA16200 has one internal DC-DC converter and several LDOs to supply power to all internal sub-blocks. Power management does the on-off control of these regulators and is implemented through the register setting inside the RTC block.

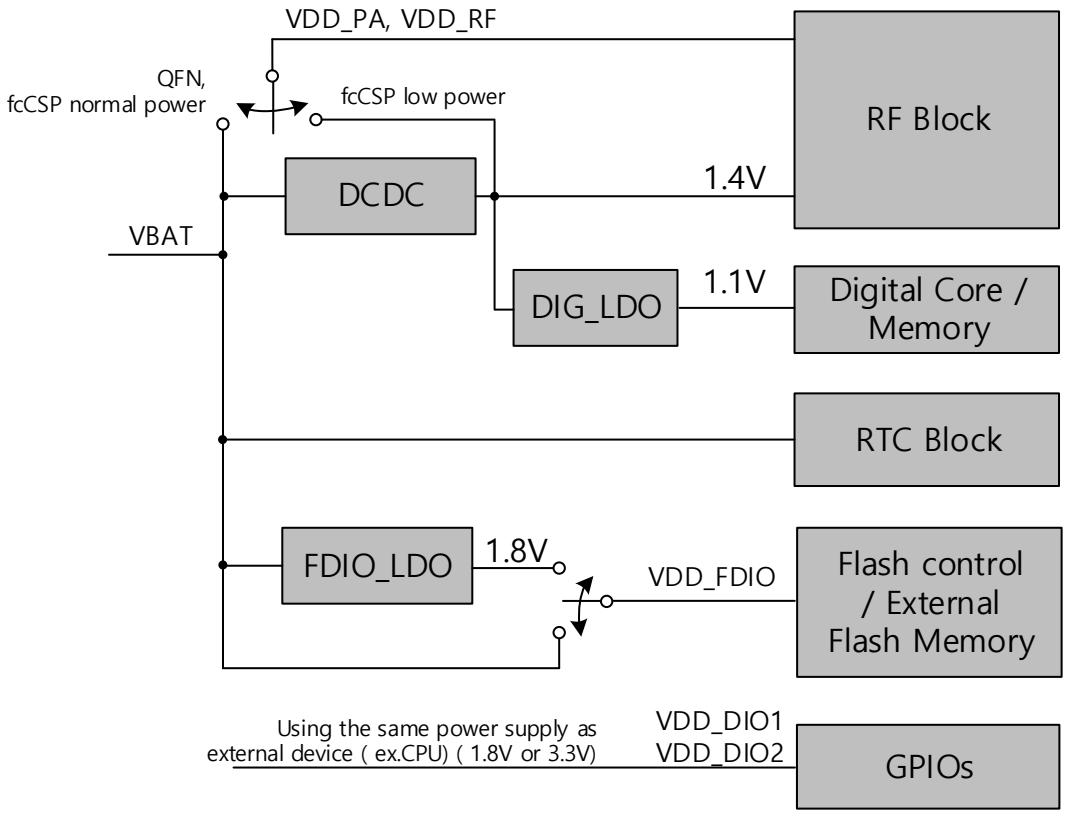

Figure 12: Power Management Block Diagram

Details of the internal DC-DC converters and LDOs are explained below:

- DC-DC converter: from the power supply of external VBAT input, it generates 1.4 V power for the digital LDO and RF block
- LDO for digital Blocks: from the DC-DC output, it generates 1.1 V power which is used for digital blocks
- LDO for I/O and external flash memory:
  - This LDO output is used only for 1.8 V digital I/O applications
  - From external VBAT power input, it generates 1.8 V output voltage which is used for digital I/O power domain in 1.8 V digital I/O applications
  - It is also used for external flash memory
  - For 3.3 V digital I/O applications, external power (3.3 V) is directly supplied for digital I/O power
- FDIO_LDO_OUT supports only 1.8 V

With the internal DC-DC converters and LDOs, all the power necessary for DA16200's internal sub-blocks are sufficiently generated.

6.3 Low Power Operation Mode

DA16200 provides three Sleep modes as low power operation modes.

6.3.1 Sleep Mode 1

Sleep mode 1 is an operational mode in which the RTC_PWR_KEY is not turned to high yet. The RTC_PWR_KEY is in the LOW state and the DA16200 is only supplied with VBAT power. With all the internal blocks off in Sleep mode 1, only the leakage current from a minimal number of internal blocks connected to VBAT remains.

6.3.2 Sleep Mode 2

Sleep mode 2 is an operational mode in which the RTC_PWR_KEY is set to high and the RTC block is running. Sleep mode 2 is activated by setting RTC registers to control the power management unit via a command from the CPU.

To turn Sleep mode 2 back to Sleep mode 1, set RTC_PWR_KEY to low.

Changing the state of the device from Sleep mode 2 to an ACTIVE state happens in one of two ways:

- The counter value is reached that is set by the CPU before entering Sleep mode 2
- An external wake-up event occurs via the RTC_WAKE_UP pin

6.3.3 Sleep Mode 3

Sleep mode 3 is a low power mode which is the same as sleep mode 2 with the addition of also maintaining the retention memory during sleep. This allows for the software to maintain information such as network connection state while in this sleep mode.

More information on how to use sleep mode 3 is contained in Ref. [2].

7 Core System

7.1 Arm Cortex-M4F Processor

The Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, low-cost debug, and includes floating point arithmetic functionality. The processor is intended for deeply embedded applications that require fast interrupt response features.

The features of the Cortex-M4F processor in DA16200 are summarized below:

- Operation clock frequency is up to 160 MHz
- 32-bit Arm Cortex-M4F architecture optimized for embedded applications
- Thumb-2 mixed 16/32-bit instruction set
- Hardware division and fast multiplication
- Includes Nested Vectored Interrupt Controller (NVIC)
- SysTick timer provided by Cortex-M4F processor
- Supports both standard JTAG (5-wire) and the low-pin-count Arm SWD (2-wire, TCLK/TMS) debug interfaces
- Cortex-M4F is binary compatible with Cortex-M3

For more information on the Arm Cortex-M4F, see Ref. [1].

7.2 Wi-Fi Processor

DA16200 includes an internal MCU (Arm Cortex-M4F) to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast and secure WLAN and Internet connections with 256-bit encryption. It supports the station, Soft AP, and Wi-Fi

Direct modes. It also supports WPA/WPA2 personal and enterprise security, WPA2 SI, WPA3 SAE, OWE, and WPS 2.0. It includes an embedded IPv4 and IPv6 TCP/IP stack.

7.3 Memory

7.3.1 Internal Memory

DA16200 contains four types of internal memories and also supports an external serial flash memory interface. The roles and functions of each memory are described in the following subsections.

7.3.1.1 ROM

This memory contains boot loader, system kernel, network stack, and various kinds of drivers for interfaces and peripherals.

7.3.1.2 SRAM

SRAM memory is used only as data space for the applications which run on the internal CPU. The applications execute directly from serial flash using an execute in place (XIP) process which loads the code into I-Cache as required. The SRAM is volatile memory and its contents will disappear when in the low-power Sleep mode.

The address range of the internal SRAM is from 0x0008_0000 to 0x000F_FFFF, and the controller of this memory supports the swap operation for the internal CPU. To do a swap operation of the controller, add the offset value to the SRAM address for read operation only.

If the offset value is 0x2080_0000, the controller will do a swap to reverse the byte order for a scalar 32-bit value. If the offset value is 0x2040_0000, the controller will do a swap to reverse the halfword (16-bit) order for a scalar 32-bit value. For example, if the value of address 0x0000_8000 is 0x12345678, reading address 0x2080_8000 will output value 0x78563412 and reading address 0x2040_8000 will output value 0x56781234.

7.3.1.3 Retention Memory

This memory is a kind of non-volatile memory and is used to save and manage essential information that should be preserved even in the low-power Sleep mode of the DA16200.

7.3.1.4 OTP

DA16200 includes a one-time field programmable non-volatile CMOS memory (OTP). The OTP memory array supports write accesses of 1 bit and read accesses of 32 bits by executing read/write commands through the OTP controllers register interface.

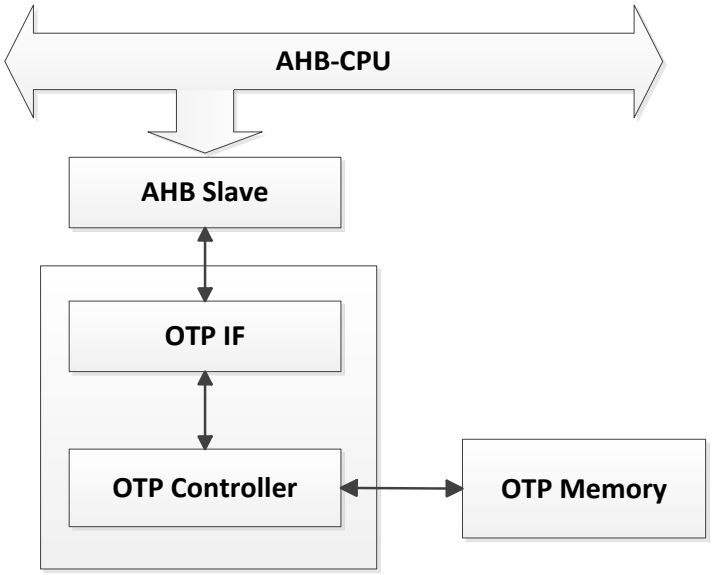

Figure 13: OTP Block Diagram

This memory is used to store and protect important information essential for mass production and the management of end products, such as boot information, MAC addresses, and serial numbers.

The OTP is also used for storing secret information which is used by the advanced security functions like secure boot, secure debug, and secure asset storage. This secret information is programmed during a secure manufacturing process and then locked so that it cannot be accessed directly by CPU read or write operations thus protecting it from external access.

Table 28: OTP Map

Offset	Field	Size (Bytes)
0x000	Dialog Reserved	1024
0x100	MAC Address #0 Low	4
0x101	MAC Address #0 High	4
0x102	MAC Address #1 Low	4
0x103	MAC Address #1 High	4
0x104	MAC Address #2 Low	4
0x105	MAC Address #2 High	4
0x106	MAC Address #3 Low	4
0x107	MAC Address #3 High	4
0x10A	XTAL Offset #0	4
0x10B	XTAL Offset #1	4
0x10C to 0x1FE	User Area	972

7.3.1.5 Serial Flash Interface

DA16200 supports an external serial memory interface, QSPI, explained in Section 9.1. This memory is used for storing DA16200's software code, including user application code, its predefined data, and various configuration data in the form of NVRAM.

7.3.1.6 Memory Map

Figure 15 shows the various peripherals that are part of the DA16200 and how they are mapped to the processor memory.

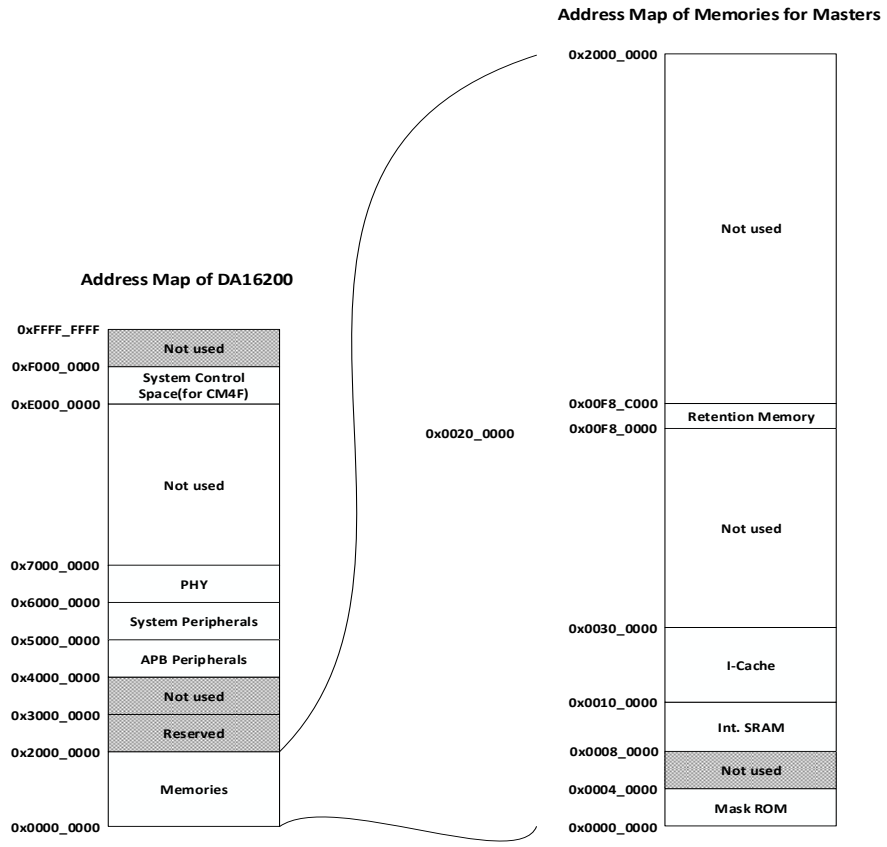

Figure 14: Memory Map

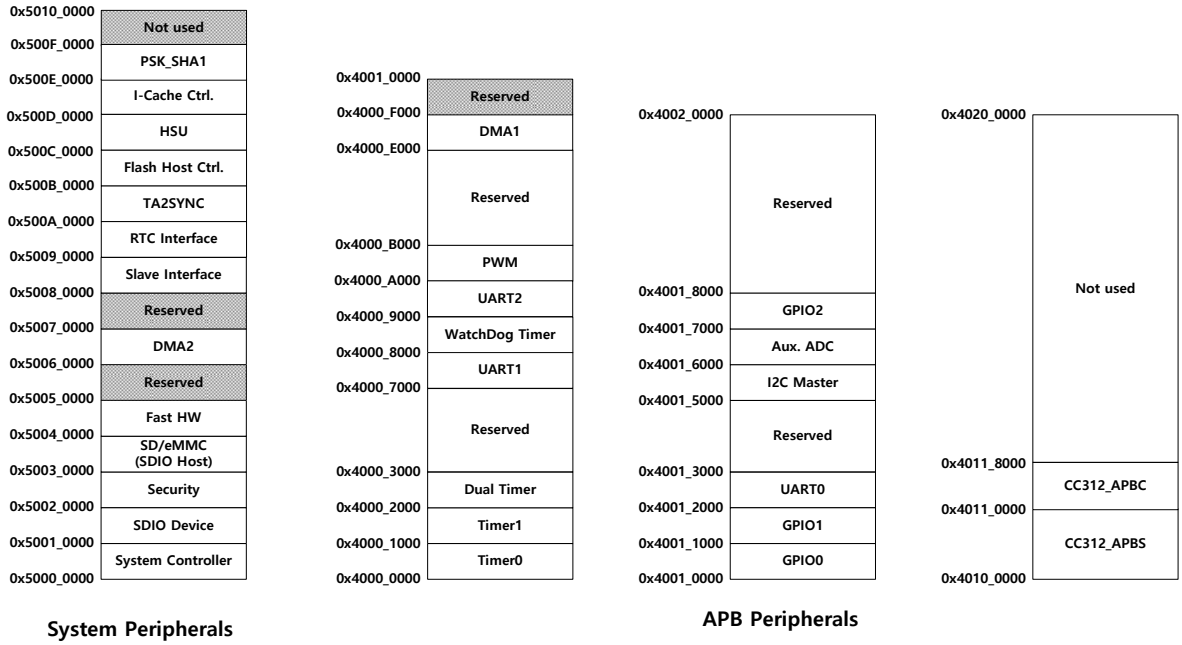

Figure 15: Memory Map: Peripherals

7.4 RTC

Among the pins in DA16200, four special pins are directly connected to the RTC block, which are RTC_PWR_KEY, RTC_GPO, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 29: RTC Pin Description

Pin Name	Pin Number		Description
	QFN	fcCSP	
RTC_PWR_KEY	42	A5	RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a predefined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in DA16200. When disabled, all blocks are powered off and this mode is defined as Sleep mode 1. DA16200 consumes minimum leakage current in Sleep mode 1.
RTC_GPO	44	E7	This pin is an output and high level is 'VBAT'. It has three different functions: • **GPO** function: its output value can be set as '1' or '0' via register setting. It can keep the value even in Sleep mode 2/3 • **Flash control** function: when in Sleep mode, it becomes '0'; when in Active mode, it is '1' • **Sensor wake-up** function: when the sensor wake-up function is used (Section 9.8.4), a programmable periodic signal is provided for an external device. Inside the RTC, there are registers to set count values
RTC_WAKE_UP	43	D6	This pin is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal via this pin and wakes up DA16200 from Sleep mode 2 or Sleep mode 3.
RTC_WAKE_UP2	23	H6	

DA16200 contains not only an on-chip oscillator that uses a 32.768 kHz external crystal but also an internal 32.768 kHz RC oscillator for faster initialization, which leads to prompt clock generation after power-up and is used until the external crystal becomes stable. Afterwards, the input source can be switched to the external crystal via a register setting.

The RTC block has a 36-bit real time counter. Its resolution is equal to one clock period of 32.768 kHz. The count value can be read via the register read command.

7.4.1 Wake-up Controller

The wake-up controller is designed to wake up DA16200 from a Sleep mode by an external signal. It detects an edge trigger of the wake-up signal and selects either the rising edge or the falling edge. Also, the wake-up signal must be maintained for at least 200 µs upon occurrence of transition on one side.

When it comes to the source of wake-up, 11 digital I/Os in addition to the two pins directly connected to the RTC block can be used. Although up to 11 digital I/Os are available for use, the maximum number of digital I/Os that are simultaneously available is eight. Table 30 describes the digital I/Os that are available for simultaneous use.

Table 30: Wake-up Sources

QFN and fcCSP Package	
Input Selection = 0	**Input Selection = 1**
GPIOA4	X
GPIOA5	X
GPIOA6	X

QFN and fcCSP Package	
Input Selection = 0	**Input Selection = 1**
GPIOA7	X
GPIOA8	X
GPIOA9	GPIOC6
GPIOA10	GPIOC7
GPIOA11	GPIOC8

For more information on the wake-up source selection, see the input selection register: 0x50091008[25:16].

The wake-up controller is in the RTC block. RTC registers can set several parameters and identify which pin is used to wake up the SoC by checking the status register after wake-up.

DA16200 has another wake-up function using analog sources, which is described in Section 9.8.4. Using the Aux-ADC, DA16200 detects whether it exceeds the predefined threshold value. If it detects the wanted condition, it will wake up from a Sleep mode. Four ports (GPIOA[3:0]) are used for this function.

7.4.2 Retention I/O Function

DA16200 I/O supports a retention mode where the I/O cells retain their previous values at the core side inputs when in Sleep mode 2 or Sleep mode 3.

Retention mode for the I/O cells is controlled by three bits in the retention enable register of the RTC block (0x5009_1018:BIT[27:24]).

To maintain a specific GPIO value when in Sleep mode 2 or Sleep mode 3, the specific bit controlling the I/O power for it must be enabled in the retention enable register.

For example, to maintain a HIGH value on GPIOA4 during Sleep mode 2 or Sleep mode 3, set the value of GPIOA4 to HIGH and also set the retention enable register BIT[25] to HIGH.

Descriptions of the retention enable register and the I/O power domains can be found in Table 31.

Table 31: I/O Power Domain

[25] DIO1	[26] DIO2	[27] FDIO
GPIOA[11:4]	GPIOC[8:6]	F_CLK
	TCLK/TMS	F_CSN
	UART0_RXD/UART0_TXD	F_IO0 to F_IO3

7.5 Pulse Counter

7.5.1 Introduction

The pulse counter is a module that counts the number of rising or falling edges of input signals. And this counter module can run even in Sleep mode 2/3. It includes one 32-bit up-counter. The input channel can be set with a register setting among the 11 digital I/Os. It also has a glitch filter that is designed to remove the unwanted trigger of an input signal.

7.5.2 Functional Description

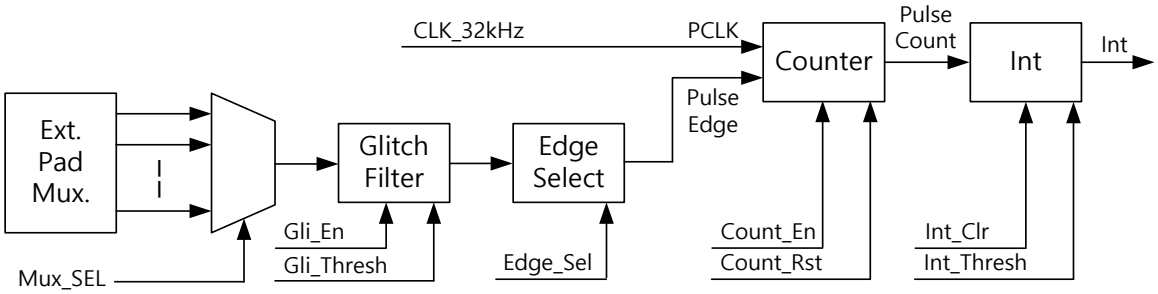

Figure 16: Pulse Counter Block Diagram

7.5.2.1 Input

Available input channels are described in Table 30. It uses the same input sources with the wake-up controller. By register setting, input channels can be selected among 11 digital I/Os.

7.5.2.2 Clock

The operation clock of the pulse counter is 32 kHz.

7.5.2.3 Counter

As described in Figure 16, the pulse counter is activated by several counter control signals. With a register setting, input signals can be selected on either the rising edges or falling edges. To enable the glitch filter module, the Gli_En and Gli_Thresh register values need to be set. The pulses whose cycles are shorter than the Gli_Thresh value are removed. The counter is a 32-bit up-counter and the counter value can be reset to zero by Count_Rst.

7.5.2.4 Interrupts

An interrupt occurs when the counter values reaches the Interrupt Threshold value (Int_Thresh). In Sleep mode 2/3, this interrupt can be used as a wake-up source.

7.6 HW Accelerators

7.6.1 Zeroing of SRAM

DA16200 provides a function to quickly set a constant value for the set SRAM area. This function is mainly used to initialize the set SRAM area to zero and can be used even when SRAM is used.

For example, assuming that the entire 512 KB SRAM is being initialized, the processing time is 8192 cycles based on the CPU clock, that is, the maximum processing time is 8192 cycles irrespective of the SRAM size to be initialized.

For more information to use this function, see Ref. [2].

7.6.2 CRC Calculation

The CRC algorithm detects the corruption of data during transmission and detects a higher percentage of errors than a simple checksum. The CRC calculation consists of an iterative algorithm involving XOR and shifts operations that is executed much faster in hardware than in software. The CRC calculator is mainly used to check the flash image and the features of CRC calculator in DA16200 are summarized below:

- Operation clock frequency is up to 160 MHz, the same as CPU clock
- Supports 8-bit, 16-bit, and 32-bit data paths
- Performs CRC operation simultaneously in real time during data transfer on the selected AHB bus
- Operation type of CRC calculation
  - CRC-32: generator polynomial is G(x) = x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 +x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1
  - CRC-16 CCITT: generator polynomial is G(x) = x^16 + x^12 + x^5 +1
  - CRC-16 IBM: generator polynomial is G(x) = x^16 + x^15 + x^2 +1

For more information to use this function, see Ref. [2].

7.6.3 Pseudo Random Number Generator

DA16200 provides a function, Pseudo Random Number Generator (PRNG), to generate a pseudo random number. The features of PRNG in DA16200 are summarized as follows:

- Operation clock frequency is up to 160 MHz, the same as CPU clock
- Supports partial parallel processing of 8-bit, 16-bit, and 32-bit unit

Generator polynomial is G(x) = x^31 + x^28 + 1 (Ref. [3])

7.7 DMA Operation

7.7.1 DMA1

DA16200 includes a DMA controller of its own with a single AHB master. The DMA1 has sixteen channels for fast data transfers from/to I2S, I2C, UARTs, and ADC to/from any on-chip RAM. The DMA requests of each module are directly connected to the dedicated DMA channels. Each DMA channel has a priority level, a smaller channel number standing for a higher priority.

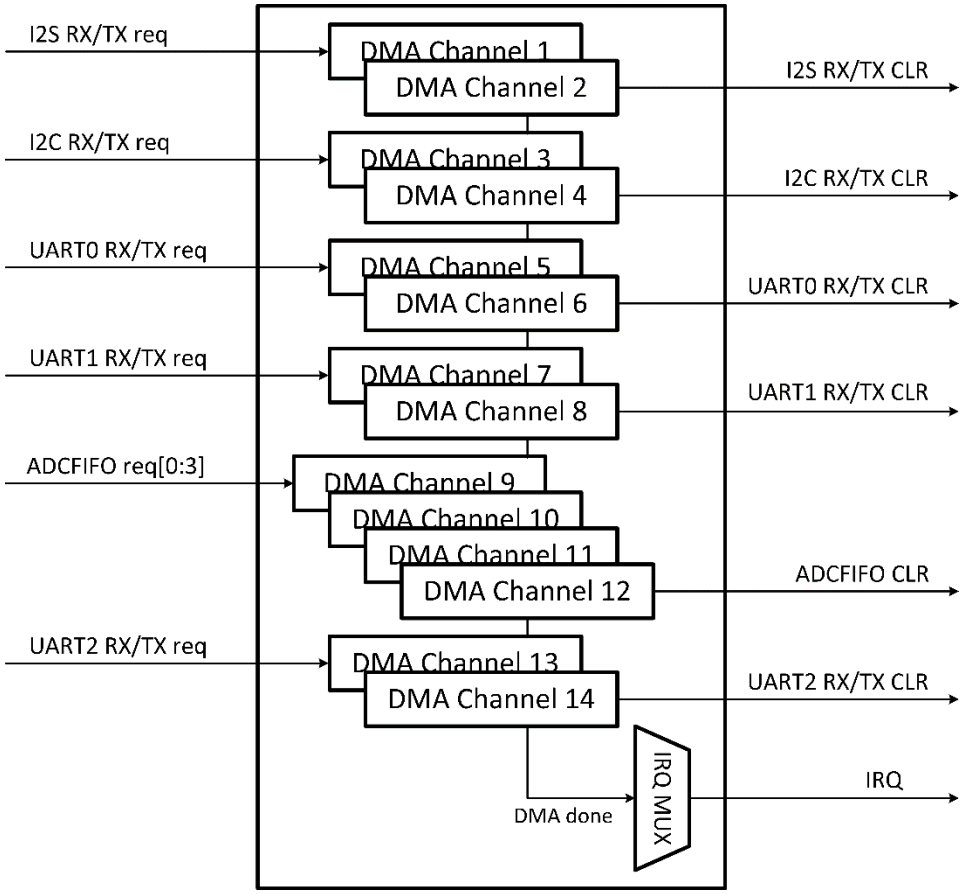

Figure 17: DMA1 Controller Block Diagram

Table 32: DMA1 Served Peripherals

DMA Channel	Module Name	Direction	Transfer Size
Channel 0	Mem-to-mem	T/RX	Word
Channel 1	I2S	RX	Word
Channel 2	I2S	TX	Word
Channel 3	I2C	RX	Byte
Channel 4	I2C	TX	Byte
Channel 5	UART0	RX	Byte
Channel 6	UART0	TX	Byte
Channel 7	UART1	RX	Byte
Channel 8	UART1	TX	Byte
Channel 9	ADCFIFO[0]	READ	Halfword
Channel 10	ADCFIFO[1]	READ	Halfword
Channel 11	ADCFIFO[2]	READ	Halfword
Channel 12	ADCFIFO[3]	READ	Halfword
Channel 13	UART2	RX	Byte
Channel 14	UART2	TX	Byte
Channel 15	Mem-to-mem	T/RX	Word

DA16200's DMA1 controller supports the Linked-List Item (LLI) function that can sequentially operate multiple DMA tasks. It is possible to reduce the SW burden and process delay with this function.

Figure 18 shows the DMA1 state machine.

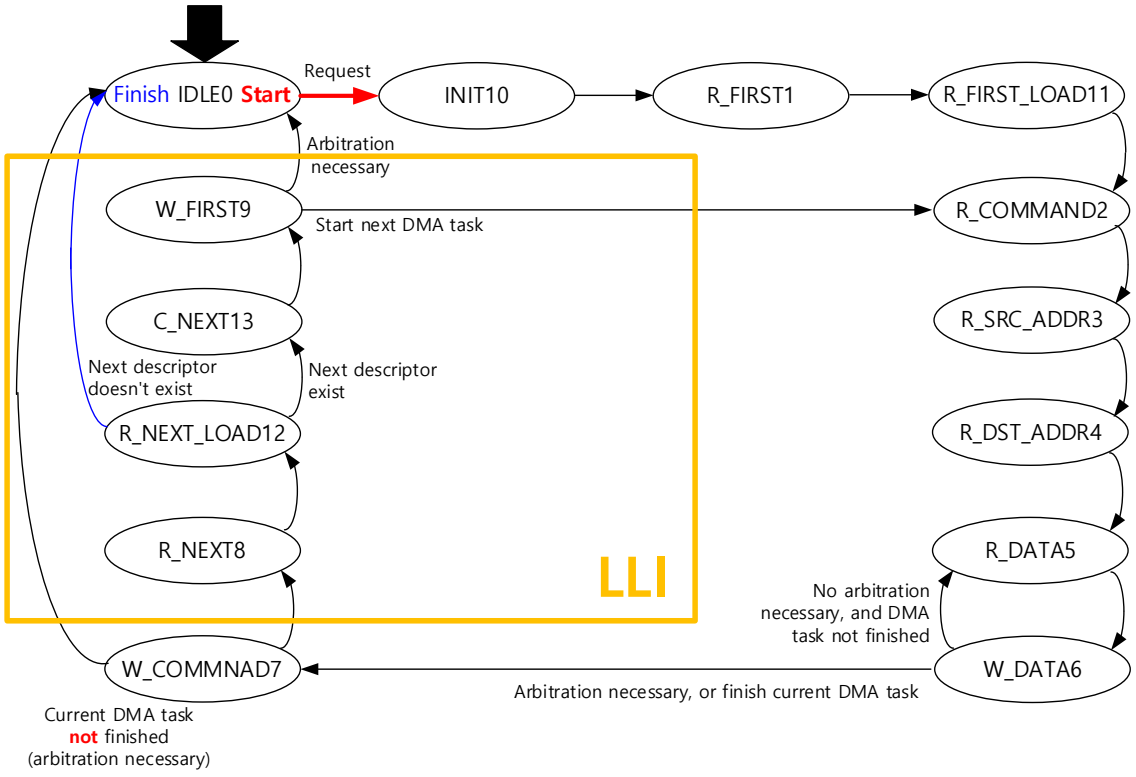

Figure 18: DMA1 State Machine

- **IDLE**: waits for the DMA request. When the DMA request appears, the state moves to R_FIRST
- **R_FIRST**: reads the address of the first DMA descriptor (head node of the linked list)
- **R_COMMAND**: reads the Command Field of the DMA descriptor
- **R_SRC_ADDR**: reads the Src_start_addr Field of the DMA descriptor
- **R_DST_ADDR**: reads the Dst_start_addr Field of the DMA descriptor
- **R_DATA**: reads the data from the source address
- **W_DATA**: writes the data read in the R_DATA state to the destination address. By the information written in the DMA descriptor, if data read/write is required, the state moves to R_DATA. If the DMA task is required to be suspended or stopped, the state moves to W_COMMAND
- **R_NEXT**: reads the next_descriptor field to check whether the next DMA task exists or not, before stopping the current DMA task
- **W_FIRST**: writes the address of the next DMA descriptor read in R_NEXT to the memory region where the first address of the DMA descriptor is stored. If arbitration is required, the state moves to IDLE state. If the current DMA channel is required to be operated, the state moves to R_FIRST state
- **INIT**, **R_FIRST_LOAD**, **R_NEXT_LOAD**, and **C_NEXT**: reduce the critical path delay in the DMA block. These states generate one clock delay

7.7.2 DMA2 (Fast DMA)

DMA2 (Fast DMA) controller consists of a master read port, a master write port, and a slave port for configuration register setting. Fast DMA performs bulk data transfers, data reading from the source address range, and data writing to the destination address range. Fast DMA is mainly used for fast data transfer from memory to memory.

The features of Fast DMA in DA16200 are summarized as follows:

- Transfer size is programmable from 1 byte to 1 Megabytes
- Up to four channels can be set at the same time
- LLI function of ring type is supported by using configuration registers of four channels
- Interrupt enable can be set for each channel
- Provides a hold function to pause data transfer for each channel

The basic unit of bus transmission is 32-bit and has a function to automatically correct address align, even if the source and destination addresses are not in word units.

For example, assuming that the transfer size is 23 bytes, the source base address is 0x001 for read access, and the destination base address is 0x102 for write access, the number of bytes per transaction is performed as follows:

- Source base address [1:0] = 0x1: the master read port of fast DMA performs read access with the following sequences:
  - 1 -> 2 -> 4 -> 4 -> 4 -> 4 -> 4 bytes
- Destination base address [1:0] = 0x2: the master write port of fast DMA performs write access with the following sequences:
  - 2 -> 4 -> 4 -> 4 -> 4 -> 4 -> 1 bytes

Figure 19 shows the DMA2 block diagram.

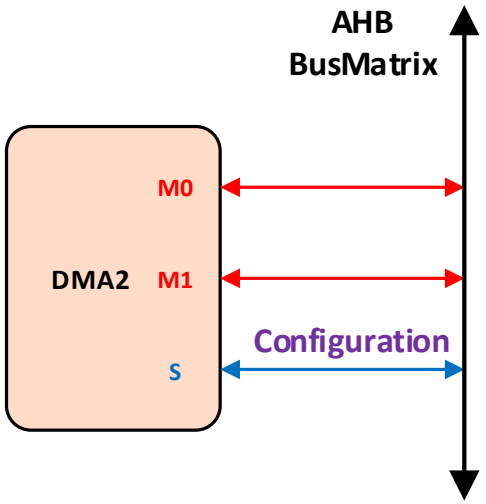

Figure 19: DMA2 Block Diagram

7.8 Simple Memory Protection

DA16200 provides simple protection for internal SRAM, ROM, and Retention Memory.

The memory controllers are AMBA AHB slaves and simple protection operates between the main AHB bus and the AHB slave port of the memory controllers.

The features of memory protection in DA16200 are summarized as follows:

- Memory protection provides the function to set the security area of each memory that should be protected
- The setting unit to set the security area for each memory is different:
  - SRAM: 1 kB/unit
  - MROM: 16 bytes/unit
  - Retention Memory: 4 bytes/unit
- Provides the access protection for the security zone for each AHB master
- Provides the write protection function for each AHB master
- Provides the read protection function for each AHB master
- Latency is 0 cycle

The index numbers to distinguish AHB masters are:

- 0x0: Cortex M4 – DCode bus
- 0x1: Cortex M4 – ICode bus
- 0x2: Cortex M4 – System bus
- 0x3: MAC DMA
- 0x4: DMA1
- 0x5: SD/eMMC (SD Host)
- 0x6: Serial Slave Interface (SPI, I2C, SDIO)
- 0x7: DMA2_M0 (read port)

- 0x8: DMA2_M1 (write port)
- 0x9: DMA of Crypto Engine
- 0xA: QSPI master – flash controller with XIP
- 0xB: Hardware Security Unit for Temporal Key Integrity Protocol (HSU for TKIP)
- 0xC: SPI master for another external SPI slaves

For more information to use this function, see Ref. [2].

7.9 Bus Protection of Serial Slave Interfaces

DA16200 supports a variety of serial slave interfaces, including SPI, I2C, and SDIO slaves.

When DA16200 interfaces with an external host, it is necessary to provide the access to the authorized area. Therefore, DA16200 provides bus protection for serial slave interfaces.

The features of bus protection in DA16200 are summarized as follows:

- Up to two accessible areas can be set and the setting unit is 4-byte
- The bus protection provides the write/read protection function outside the set area

For more information to use this function, see Ref. [2].

7.10 Watchdog Timer

The watchdog timer in DA16200 is based on a 32-bit down-counter that is initialized from the reload register, WDOGLOAD. The watchdog timer generates a regular interrupt, WDOGINT, depending on the programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH.

The watchdog monitors the interrupt and asserts a reset request signal, WDOGRES, when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues. If the interrupt is not cleared by the time the counter reaches 0 for a second time, the watchdog timer reasserts the reset signal.

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog unit can be enabled or disabled as required.

Figure 20 shows the watchdog timer block diagram.

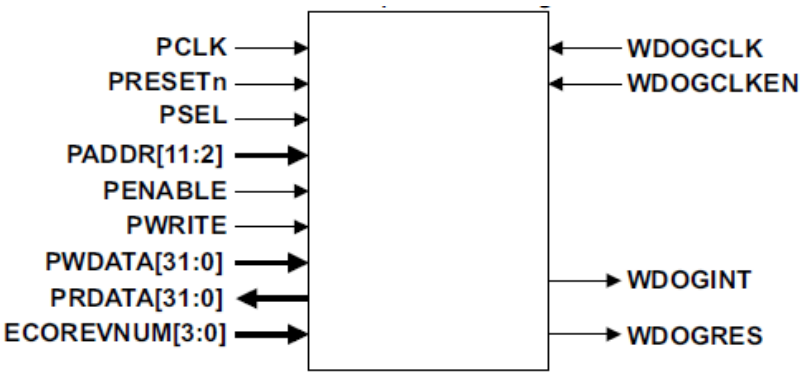

Figure 20: Watchdog Timer Block Diagram

Figure 21 shows the flow diagram for the watchdog operation.

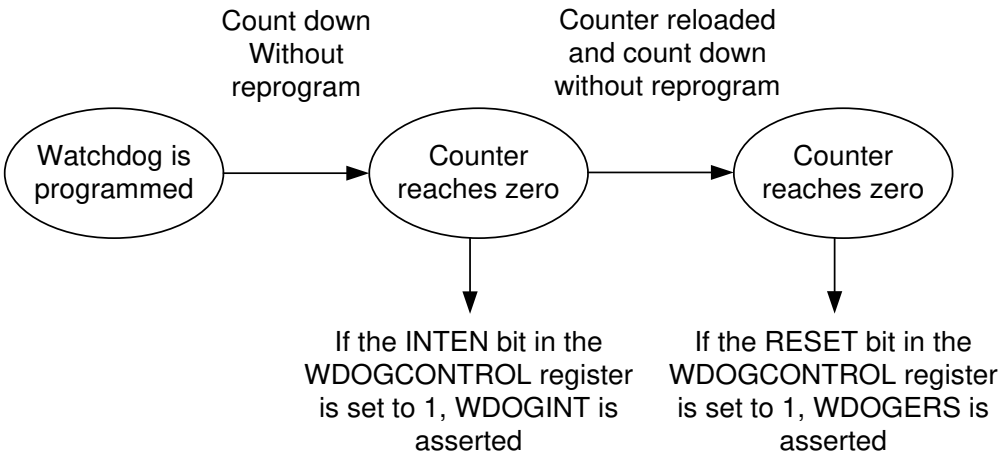

Figure 21: Watchdog Operation Flow Diagram

7.11 Clock Generator

The generation of the system's clocks is described in detail in Figure 22.

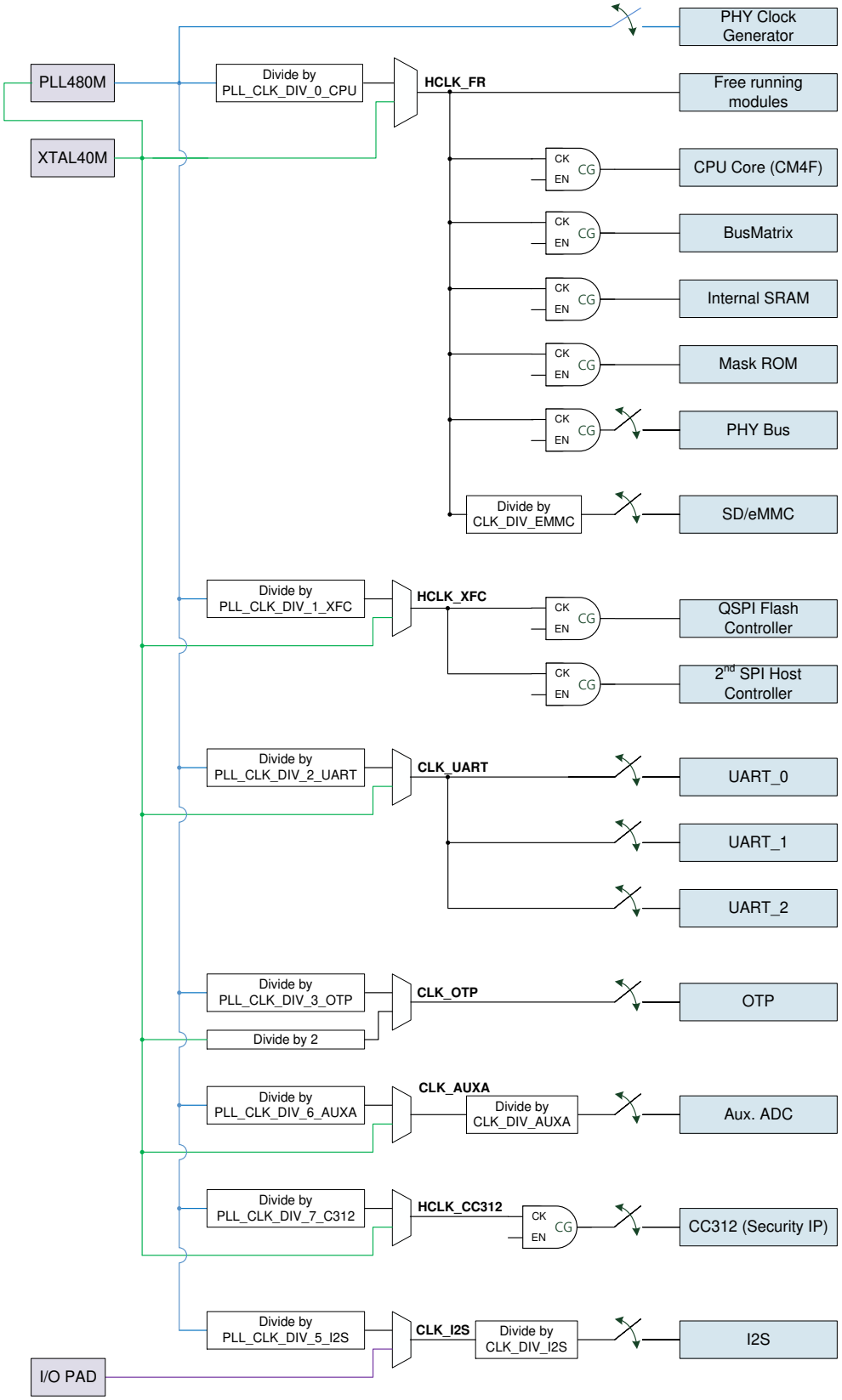

Figure 22: Clock Tree Diagram

8 Crypto Engine

The HW crypto engine provides acceleration of many crypto algorithms such as hashing, secret key generation, encryption/decryption and sign/verify operations.

Table 33 shows the HW accelerated crypto algorithms supported by the DA16200. This table is cited from Ref. [4]. Examples of how to use these crypto algorithms are explained in Ref. [2].

Table 33: HW Accelerated Crypto Algorithms in DA16200

Algorithm	Mode	Key Sizes
AES	ECB, CBC, CTR, OFB, CMAC, CBC-MAC, AESCCM, AES-CCM*, AES-GCM	128 bits, 192 bits, and 256 bits.
AES key wrapping	N/A	All
Chacha20 and Poly1305	N/A	256 bits.
Diffie-hellman • *ANSI X9.42-2003: Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography* • *Public-Key Cryptography Standards (PKCS) #3: Diffie Hellman Key Agreement Standard*	N/A	1024 bits, 2048 bits, and 3072 bits.
ECC key generation	N/A	NIST curves and 25519 curves.
ECIES	N/A	NIST curves and 25519 curves.
ECDSA	N/A	NIST curves and ED25519.
ECDH	N/A	NIST curves and 25519 curves.
Hash	SHA1, SHA224 and SHA256.	N/A
HKDF	N/A	N/A
HMAC	SHA1, SHA224 and SHA256.	N/A
KDF *NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions*	CMAC or HMAC.	N/A
RSA PKCS#1 operations • *Public-Key Cryptography Standards (PKCS) #1 v2.1: RSA Cryptography Specifications* • *Public-Key Cryptography Standards (PKCS) #1 v1.5: RSA Encryption*	Encryption and signature schemes.	2048 bits, 3072 bits, and 4096 bits.
RSA key generation	N/A	2048 bits and 3072 bits.

9 Peripherals

This section describes the peripherals that are supported by the DA16200 device.

9.1 QSPI Master with XIP Feature

QSPI master supports 4-line SPI communication with commercial flash memory devices and uses a Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when the 1-line communication mode is used, it can be used as the SPI master.

QSPI master is an IP for communication between the flash memory and AMBA AHB bus and is designed to support XIP. The features of the QSPI master are summarized as follows:

Serial flash interface:

- SPI compatible serial bus interface
  - Configurable SPI I/O modes:
    - Single I/O mode
    - Dual I/O mode
    - Quad I/O mode
  - JEDEC Standard: JESD216B
  - 24-bit and 32-bit addressing
  - Supports to access flash with XIP mode
    - Read access without command
    - Read access without address and command
  - Programmable SPI clock phase and polarity
  - Maximum number of SPI CS is four that can be operated
- Compatible with serial NOR flash devices, such as Macronix, Micron, Spansion, ESMT, and ISSI

AMBA slave interface

- Compliance to the *AMBA AHB Bus Specification*, *Rev 3.0 Ref.* [6]
- Direct code execution: directly addressable access without additional driver software
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction
- AMBA slave interface is optional to access configuration and status registers
- Simple timer is used to check the completion time of flash operation
- XIP path of QSPI master supports HW remapping function to execute selected boot image for over-the-air programming (OTA)

AMBA master interface

- Compliance to the *AMBA AHB Bus Specification*, *Rev 3.0 Ref.* [6]
- Supports DMA operation to access serial flash devices
  - Automatic copy of code image from serial flash to system RAM
  - Automatic programming of code image from system RAM to serial flash
- Performs a mem-to-mem copy in units of 32 bits, regardless of the address and length
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction

Figure 23 shows the QSPI Master Block Diagram.

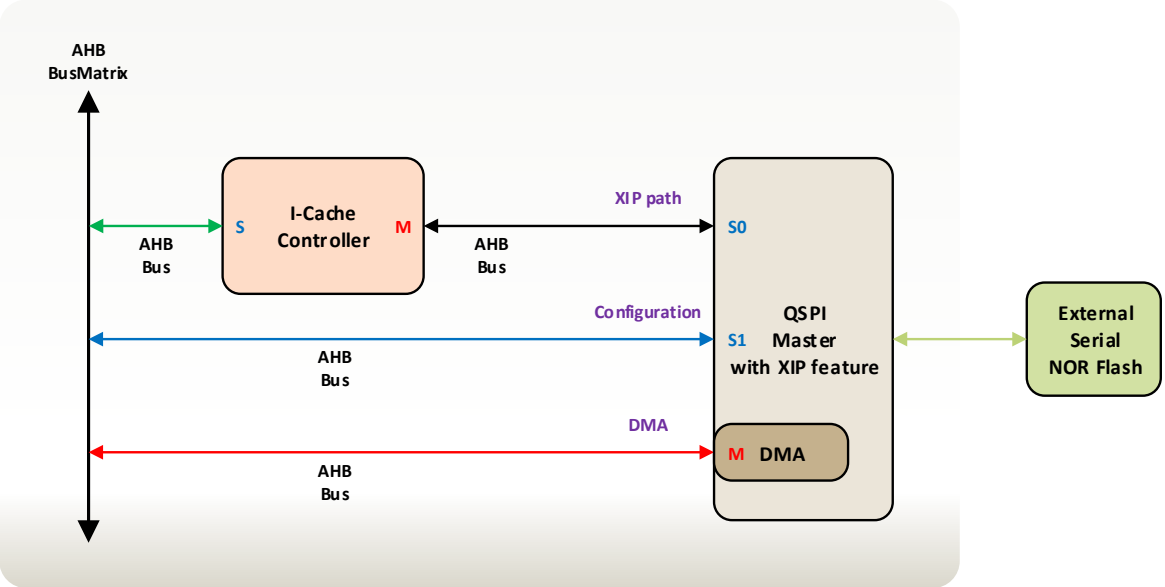

Figure 23: QSPI Master Block Diagram

Figure 24 shows the timing diagram for the QSPI master.

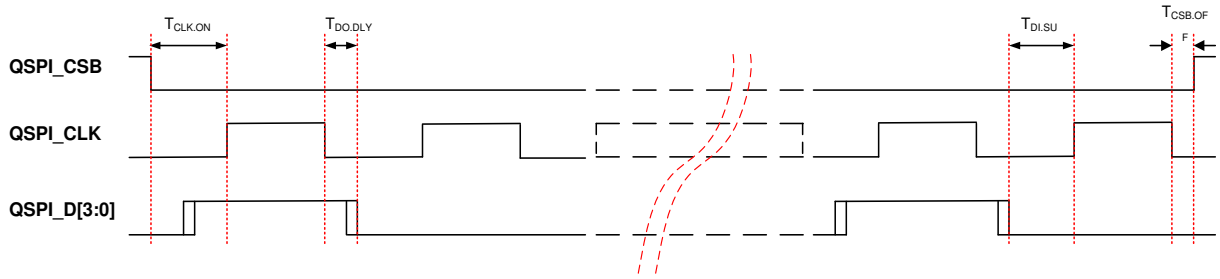

Figure 24: QSPI Master Timing Diagram (Mode 0)

Table 34 lists the timing parameters for the QSPI master.

Table 34: QSPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	10		120	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 ×T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		TCLK	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^{6})^{-1}$ seconds.

9.2 SPI Master

QSPI can use the SPI master with the use of a single line interface. Table 35 shows the pin definition of the SPI master interface. SPI signal timing is the same as QSPI.

To use DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from the GPIO special function by setting the registers in the GPIO.

Table 35: SPI Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOx			O	E_SPI_CSB[3:1]
GPIOA6	32	E3	O	E_SPI_CSB[0]
GPIOA7	31	E1	O	E_SPI_CLK
GPIOA8	30	G3	I/O	E_SPI_MOSI or E_SPI_D[0]
GPIOA9	29	H2	I/O	E_SPI_MISO or E_SPI_D[1]
GPIOA10	28	F2	I/O	E_SPI_D[2]
GPIOA11	27	G1	I/O	E_SPI_D[3]

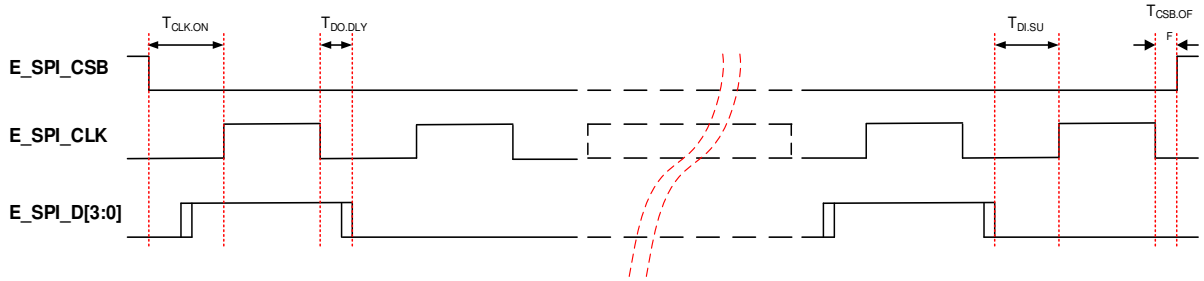

Figure 25: SPI Master Timing Diagram (Mode 0)

Table 36: SPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	5		60	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 × T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds.

9.3 SPI Slave

The SPI slave interface is a half-duplex connection for an external host to control the DA16200. The range of the SPI clock speed is based on the internal bus clock speed and can be calculated using:

spi clock = system clock/N

where N is an integer divider such as 1,2,3,4,5,6,...

The SPI slave supports both the Burst mode and Non-burst mode. In the Burst mode, SPI_CSB remains active from the start to the end of communication. In the Non-burst mode, SPI_CSB remains active at every eight bits.

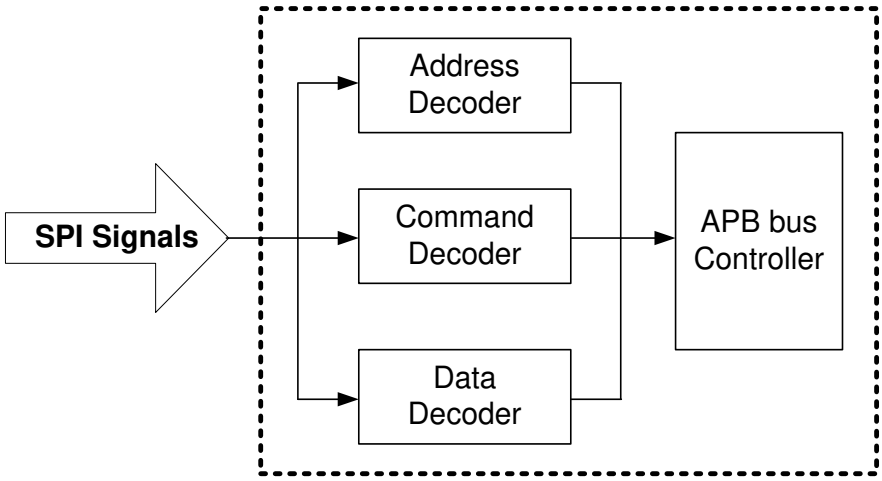

Figure 26: SPI Slave Block Diagram

Communication protocols of the SPI slave interface use either 4-byte or 8-byte control signals. Between the two available communication protocols, the CPU chooses one before initiating the control.

Figure 27 and Figure 28 shows the 8-byte and 4-byte control types.

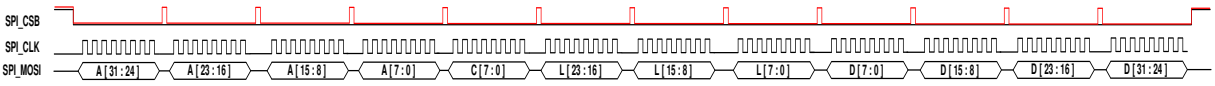

Figure 27: 8-byte Control Type

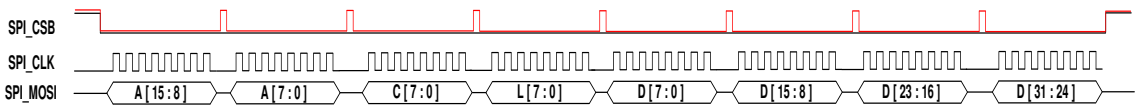

Figure 28: 4-byte Control Type

The 8-byte control type uses a 4-byte address, 1-byte control, and 3-byte length. The 4-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 3-byte length shows the length of data subject to continuous access in bytes. Hence, when the 8-byte control type is applied, the maximal length of data subject to continuous access is 16 MB.

The 4-byte control type uses a 2-byte address, 1-byte control, and 1-byte length. The 2-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 1-byte length shows the length of data subject to continuous access in bytes. Since the 32-bit address map is used internally, the 2-byte address is not enough to express everything. Thus, the upper 2-byte base address is designated, and then the lower 2-byte address is used.

Table 37 and Table 38 show the meaning of each bit in the 1-byte control in the 8-byte control type and the 4-byte control type, respectively.

Table 37: Control Field of the 8-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal Address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5:0		Not used. Set all bits to '0'	

Table 38: Control Field of the 4-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5	Common	1 = Refer base address as common area	0 = Refer base address
4	Length section	1 = Refer to register value	0 = Refer to length field
3:0	Length[12:8]	Length field upper	

Table 39 shows the pin definition of the SPI slave interface.

Table 39: SPI Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA2	37	B2	I	SPI_CSB
GPIOA6	32	E3	I	
GPIOA3	36	D4	I	SPI_CLK
GPIOA7	31	E1	I	
GPIOA1	38	C3	I	SPI_MOSI
GPIOA9	29	H2	I	
GPIOA11	27	G1	I	
GPIOA0	39	A3	O	SPI_MISO
GPIOA8	30	G3	O	
GPIOA10	28	F2	O	

Figure 29 shows the timing diagram for the SPI slave.

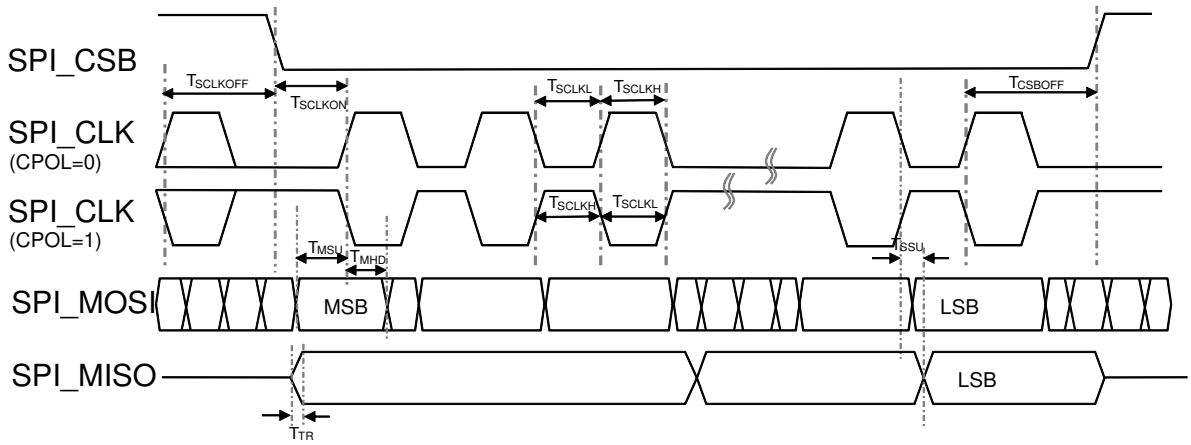

Figure 29: SPI Slave Timing Diagram

Table 40 lists the timing parameters for the SPI slave.

Table 40: SPI Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}	-	-	50	MHz
SCLK clock duty		40			%
Non active duration	$T_{SCLKOFF}$	400	-	-	ns
1st CLK active rising transition time	T_{SCLKON}	T_{SCLKL}(CPOL=0) T_{SCLKH} (CPOL=1)	-	-	ns
CSB non active rising transition time	T_{CSBOFF}	T_{SCLKH} (CPOL=0) T_{SCLKL} (CPOL=1)	-	-	ns
MOSI setup time	T_{MSU}	8	-	T_{SCLK} (Note 1)	ns
MOSI hold time	T_{MHD}	8	-	T_{SCLK}	ns
MISO delay time	T_{SSU}	-	-	8	ns
MISO transition time (10 % to 90 % transition)	T_{TR}	-	4	5	ns

Note 1 $T_{SCLK} = 0.5 \times (F_{SCLK} \times 10^{6})^{-1}$ second.

9.4 SDIO

SDIO is a full/high speed card suitable for memory card and I/O card applications with low power consumption. The full/high speed card supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 50 MHz. To be compatible with the serviceable SDIO clock, the internal BUS clock needs to be set to minimum 50 MHz. The CIS and CSA areas are located inside the internal memory and the SDIO registers (CCCR and FBR) are programmed by the SD host.

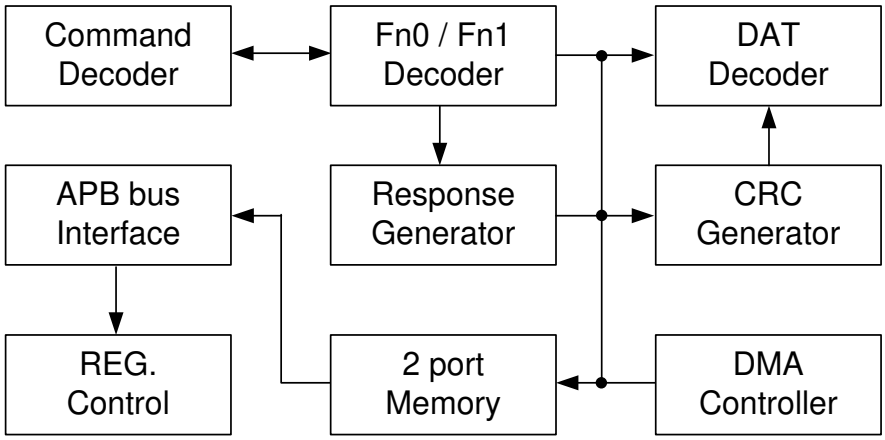

Figure 30: SDIO Slave Block Diagram

Table 41 shows the pin definition of the SDIO interface.

The GPIOA4 and GPIOA5 pins are set to SDIO CMD and CLK by default. If SDIO initialization is done and SDIO communication is enabled, then the SDIO data pin setting is done automatically. In other words, when the SDIO communication is detected, the pin used as the SDIO data among the GPIO pins is automatically activated in the SDIO use mode. However, the auto setting function is not supported for the F_xxx pin used as the flash function.

Table 41: SDIO Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SDIO_CMD
GPIOA5	33	D2	I	SDIO_CLK
GPIOA9	29	H2	I/O	SDIO_D0
GPIOA8	30	G3	I/O	SDIO_D1
GPIOA7	31	E1	I/O	SDIO_D2
GPIOA6	32	E3	I/O	SDIO_D3

Figure 31 shows the timing diagram for the SDIO slave.

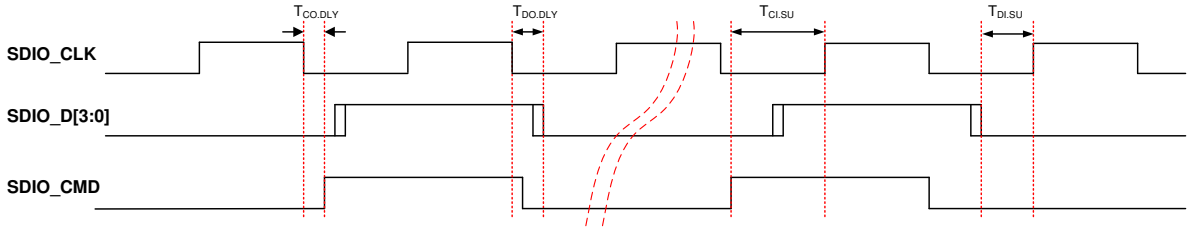

Figure 31: SDIO Slave Timing Diagram

Table 42 lists the timing parameters for the SDIO slave.

Table 42: SDIO Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CLK frequency	F_{SCLK}	-	-	50	MHz
SDIO_CLK clock duty			50		%
SDIO_CMD input setup time	$T_{CI.SU}$	3			ns
SDIO_CMD output delay time	$T_{CO.DLY}$			11 (Note 1)	ns
SDIO_D[3:0] input setup time	$T_{DI.SU}$	3			ns
SDIO_D[3:0] output delay time	$T_{DO.DLY}$			11 (Note 1)	ns

Note 1 SDIO signals can set previous output from half cycle.

The SDIO interface requires pullup resistors to be connected between the signal lines and the supply to enable communication.

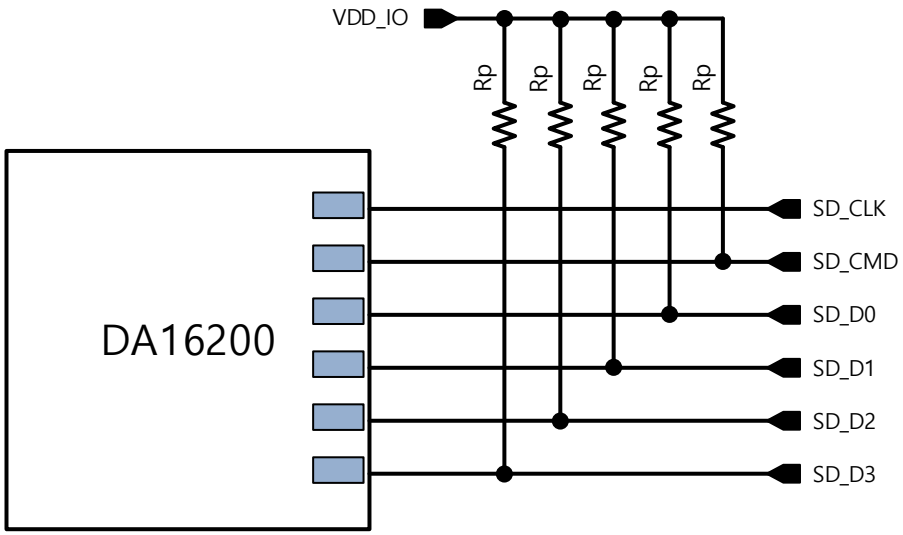

Figure 32: SDIO Pull-up Resistor

Pull-up resistor values may vary based on the board layout.

9.5 I2C Interface

9.5.1 I2C Master

DA16200 includes an I2C master module. Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz) and High Speed (3.4 MHz) mode. Table 43 shows the pin definition of the I2C master interface.

Table 43: I2C Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	O	I2C_CLK
GPIOA5	33	D2	O	
GPIOA9	29	H2	O	
GPIOA0	39	A3	I/O	I2C_SDA
GPIOA4	34	F4	I/O	
GPIOA8	32	G3	I/O	

Figure 33 shows the I2C timing diagram. The timing diagram is the same as that of the I2C slave timing diagram.

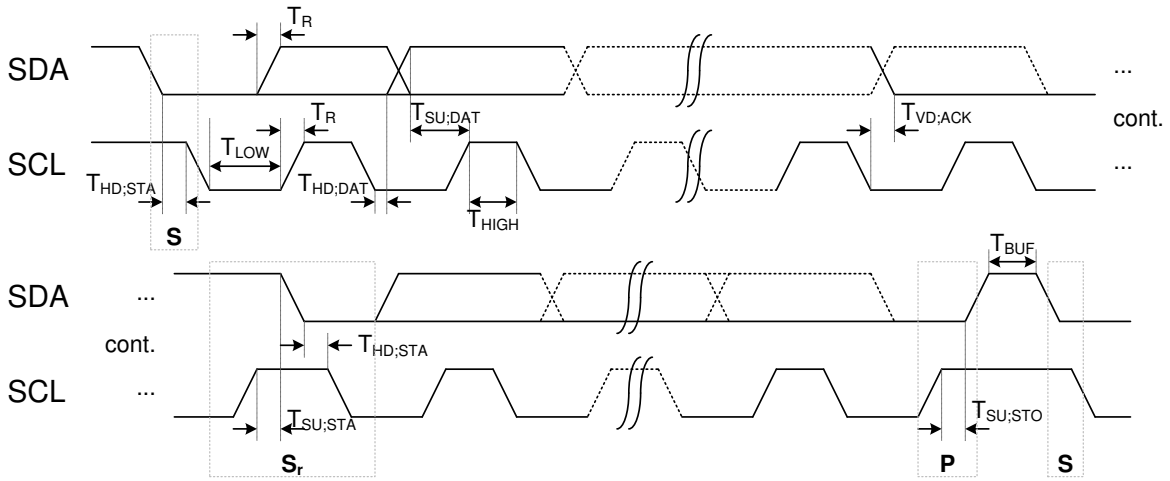

Figure 33: I2C Master Timing Diagram

Table 44 lists the I2C master timing parameters.

Table 44: I2C Master Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
Operating Bus clock frequency	F_{op_clk}	30	120	30	120	MHz
SCL clock frequency	F_{SCLK}	100	400	100	3400 (Note 2)	kHz
Clock Duty (Note 1)		40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.2	-	0.2	-	µs
Low period of the SCL clock	T_{LOW}	1.27	-	0.55	-	µs

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
High period of the SCL clock	T_{HIGH}	1.23	-	0.45	-	µs
Setup time for START condition	$T_{SU;STA}$	1.1	-	0.37	-	µs
Data hold time	$T_{HD;DAT}$	3x T_{op_clk} (Note 3)	-	3x T_{op_clk} (Note 3)	-	µs
Data setup time	$T_{SU;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	µs
Rise time of both SDA and SCL	T_R (Note 4)	0.02	0.3	0.05	0.05	µs
Setup time for STOP condition	$T_{SU;STO}$	0.36	-	0.45	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	3x T_{op_clk} (Note 3)	-	3x T_{op_clk} (Note 3)	-	µs
Buffer free time between START and STOP condition	T_{BUF}	0.5	-	0.5	-	µs

Note 1 Clock duty ratio = (T_{HIGH} /T_{SCLK}) × 100[%], T_{SCLK} = 1/F_{SCLK}.

Note 2 Max. clock = 3.4 MHz (T_{SCLK} = 294 ns) over 40 MHz of the F_{op_clk}.
Max. clock = 1.0 MHz (TSCLK = 1000 ns) under 40 MHz of the Fop_clk.

Note 3 T_{op_clk} = (1 / F_{op_clk}) x 10^6 µsec.

Note 4 T_R depends on a pull-up resistor value.

9.5.2 I2C Slave

The I2C slave interface provides support for an external host to control the DA16200. The pin mux configuration is defined in Table 45.

Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz) and High Speed (3.4 MHz).

Table 45: I2C Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	I	I2C_CLK
GPIOA3	36	D4	I	
GPIOA5	33	D2	I	
GPIOA7	31	E1	I	
GPIOA0	39	A3	I/O	I2C_SDA
GPIOA2	37	B2	I/O	
GPIOA4	34	F4	I/O	
GPIOA6	32	E3	I/O	

Figure 34 shows the I2C slave timing diagram.

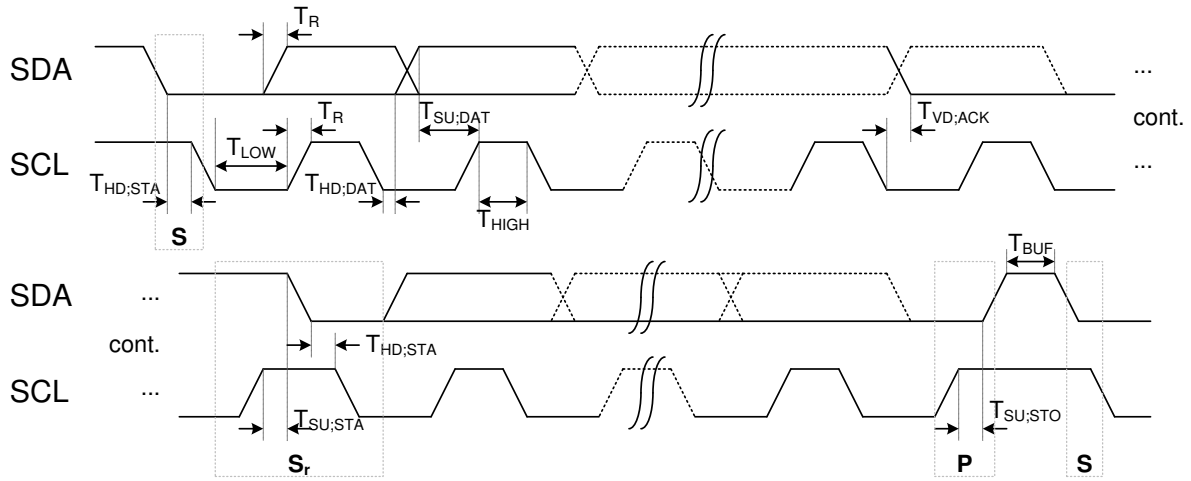

Figure 34: I2C Slave Timing Diagram

Table 46 lists the I2C slave timing parameters.

Table 46: I2C Slave Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	100	400	100	3400 (Note 2)	kHz
Clock Duty (Note 1)		40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.6	-	0.26	-	µs
Low period of the SCL clock	T_{LOW}	1.3	-	0.15	-	µs
High period of the SCL clock	T_{HIGH}	1.2	-	0.14	-	µs
Setup time for START condition	$T_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$T_{HD;DAT}$	0	-	0	-	µs
Data setup time	$T_{SU;DAT}$	0.1	-	0.05	-	µs
Rise time of both SDA and SCL	T_R	0.02	0.3	-	0.12	µs
Setup time for STOP condition	$T_{SU;STO}$	0.6	-	0.26	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	-	-	-	-	µs
Buffer free time between START and STOP condition	T_{BUF}	1.3	-	0.5	-	µs

Note 1 Clock duty ratio = (T_{HIGH}/T_{SCLK}) × 100[%], $T_{SCLK} = 1/F_{SCLK}$.

Note 2 Max. clock = 3.4 MHz (T_{SCLK} = 294 ns) over 40 MHz of the F_{op_clk}.
Max. clock = 1.0 MHz (TSCLK = 1000 ns) under 40 MHz of the Fop_clk.

9.5.3 Interface Pull-up

The I2C interface requires pull-up resistors to be connected between the signal lines and the supply to enable communication.

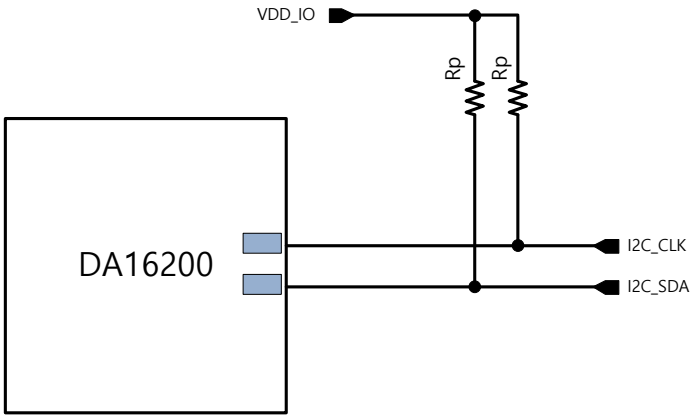

Figure 35: I2C Pull-up Resistor

Pull-up resistor values may vary based on the board layout.

9.6 SD/eMMC

The SD/eMMC host interface of the DA16200 provides access to SD or eMMC memory cards. The SD/eMMC host interface supports a 4-bit data bus with a maximum clock rate of 48 MHz giving a maximum data rate of 24 MB/s (192 Mbps).

The SD/eMMC pin mux condition is defined in Table 47.

Table 47: SD/eMMC Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SD/eMMC_CMD
GPIOA5	33	D2	O	SD/eMMC_CLK
GPIOA9	29	H2	I/O	SD/eMMC_D0
GPIOA8	30	G3	I/O	SD/eMMC_D1
GPIOA7	31	E1	I/O	SD/eMMC_D2
GPIOA6	32	E3	I/O	SD/eMMC_D3
GPIOA10	28	F2	I	SD/eMMC_WRP
GPIOA1	38	C3	I	

9.6.1 Block Diagram

Figure 36 shows the block diagram of the SD/eMMC host interface including the control register, clock control, command/response pipe, data pipe, and AHB master interface blocks.

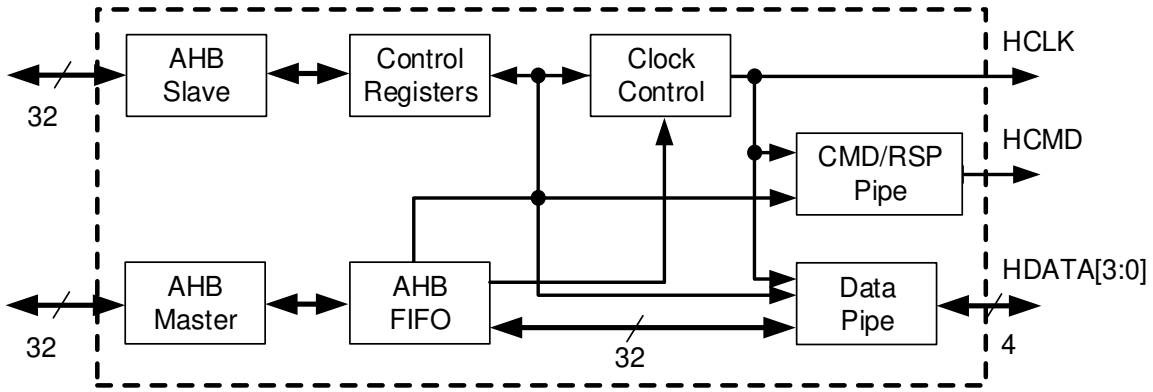

Figure 36: SD/eMMC Block Diagram

Figure 37 shows the timing diagram for the SD/eMMC master.

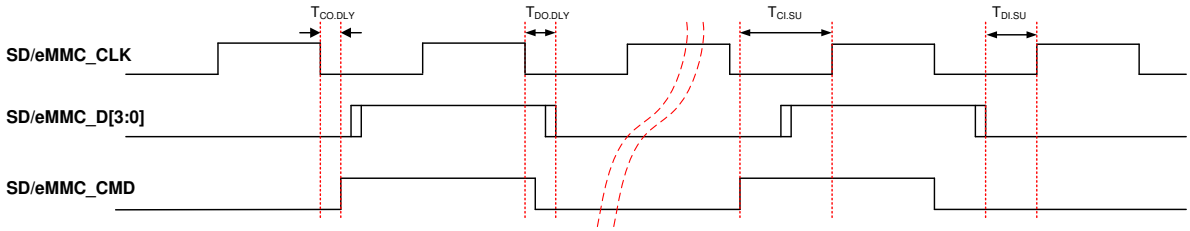

Figure 37: SD/eMMC Master Timing Diagram

Table 48 lists the timing parameters for the SD/eMMC master.

Table 48: SD/eMMC Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SD/eMMC_CLK frequency	F_{SCLK}	-	-	50	MHz
SD/eMMC_CLK clock duty			50		%
SD/eMMC_CMD input setup time	$T_{CI.SU}$	8			ns
SD/eMMC_CMD output delay time	$T_{CO.DLY}$			3	ns
SD/eMMC_D[3:0] input setup time	$T_{DI.SU}$	8			ns
SD/eMMC_D[3:0] output delay time	$T_{DO.DLY}$			8	ns

9.7 I2S

DA16200 provides an I2S interface. Once an I2S block receives audio data through the DMA, that audio data is sent to the external port according to the I2S standard. To use the external DAC, output through the GPIO port is possible when a register setting is made according to the pin configuration (see Table 49).

The I2S also provides a receive function. However, I2S transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by register setting. If the I2S signal is input from outside after the reception function is set, the audio signal can be decoded, stored in the FIFO, and read out through the DMA. The decodable reception function provides 8/16/24/32-bit modes and can receive either mono or stereo.

Using the I2S clock divider register, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from outside using the GPIO pin. For accurate I2S audio sampling, the I2S clock source can be input to external GPIO pins. It needs to select the GPIO pin setting as the I2S clock input and apply the appropriate clock source. The available I2S clock pins are shown in Table 49.

Table 49: I2S Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	O	I2S_MCLK
GPIOA5	33	D2	O	
GPIOA9	29	H2	O	
GPIOA0	39	A3	O	I2S_BCLK
GPIOA4	34	F4	O	
GPIOA8	30	G3	O	
GPIOA3	36	D4	O	I2S_LRCK
GPIOA7	31	E1	O	
GPIOA2	37	B2	I/O	I2S_SDO
GPIOA6	32	E3	I/O	
GPIOA3	36	D4	I	I2S_CLK_IN
GPIOA10	28	F2	I	

9.7.1 Block Diagram

I2S has the following features:

- Master Clock Mode only
- I2S Data pin can work in either Input mode or Output mode
- Clock source can be "internal 480 MHz/N" (currently using 24 MHz) or "external clock source"
- Max Sampling Rate: 48 kHz
- Mono/Stereo Mode

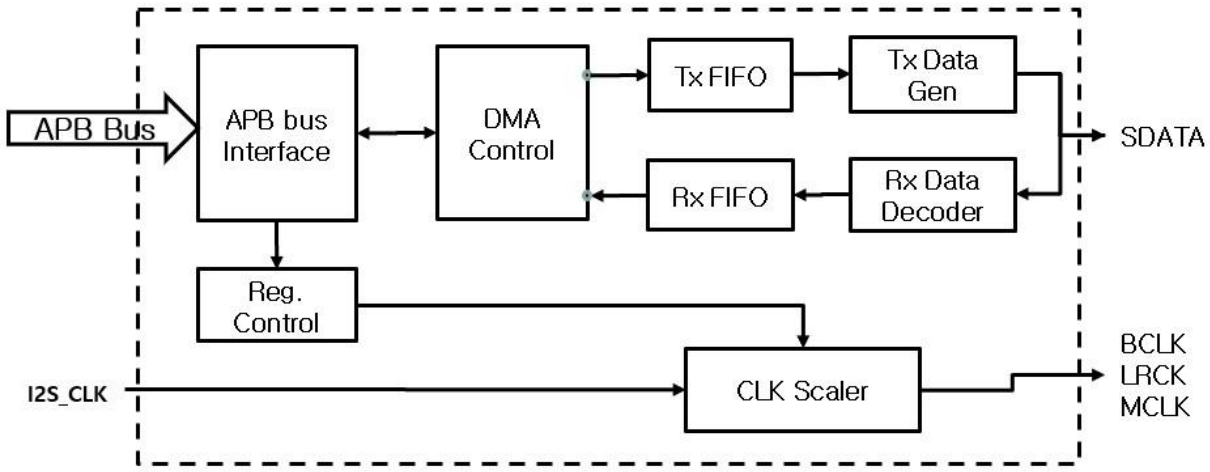

Figure 38: I2S Block Diagram

9.7.2 I2S Clock Scheme

The I2S uses a 24 MHz clock as default from the RF reference clock (40 MHz), so it can support 46.875 kHz of sampling rate. External clock sources are needed to support the standard sampling rate. See Table 50.

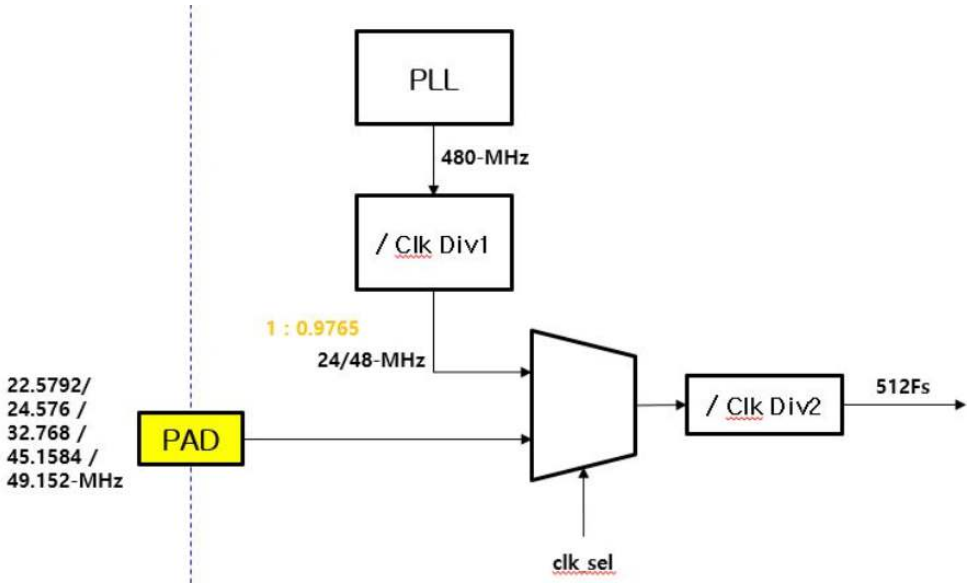

Figure 39: I2S Clock Scheme

Table 50: I2S Clock Selection Guide

Parameter										Units
LRCK	Fs	8	12	16	24	32	44.1	46.875	48	kHz
BCLK	64Fs	0.512	0.768	1.024	1.536	2.048	2.8224	3	3.072	MHz
MCLK	512Fs	4.096	6.144	8.192	12.288	16.384	22.5792	24	24.576	MHz
Clk Div2	N (=1,2,3…)	6	4	3	2	2	1	1	1	
I2S_CLK		24.576	24.576	24.576	24.576	32.768	22.5792	24 (Internal PLL)	24.576	MHz

NOTE
To confirm the exact LRCK operation, drive the Clock source at I2S_CLK.

9.7.3 I2S Transmit and Receive Timing Diagram

I2S output is possible in the following three modes. The main clock (MCLK) always outputs in 512×fs.

- I2S Mode

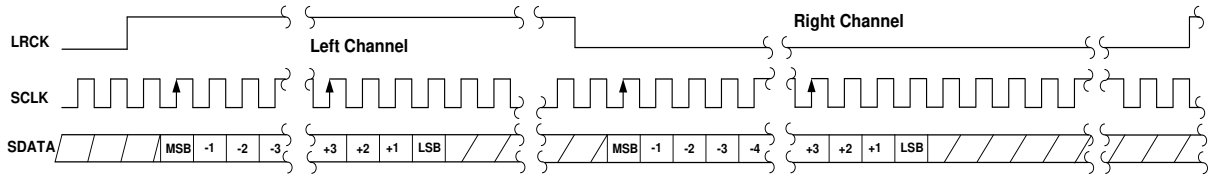

Figure 40: I2S Timing Diagram

- Left Justified Mode

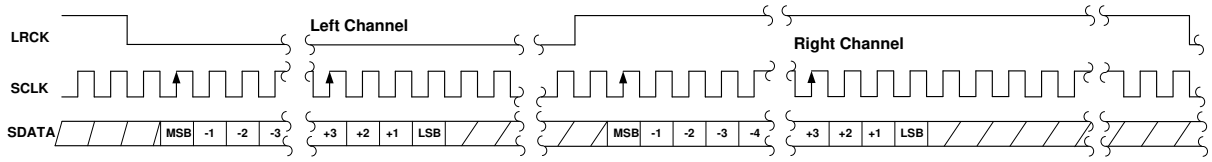

Figure 41: Left Justified Mode Timing Diagram

- Right Justified Mode

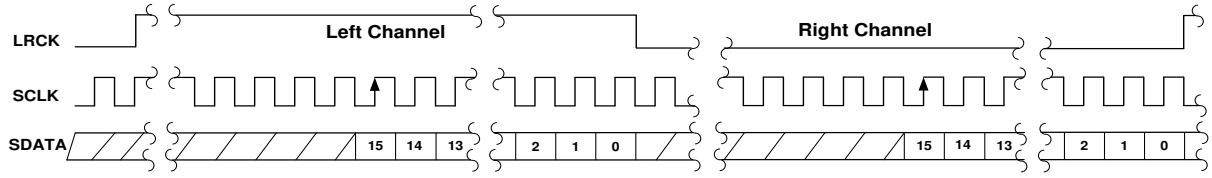

Figure 42: Right Justified Mode Timing Diagram

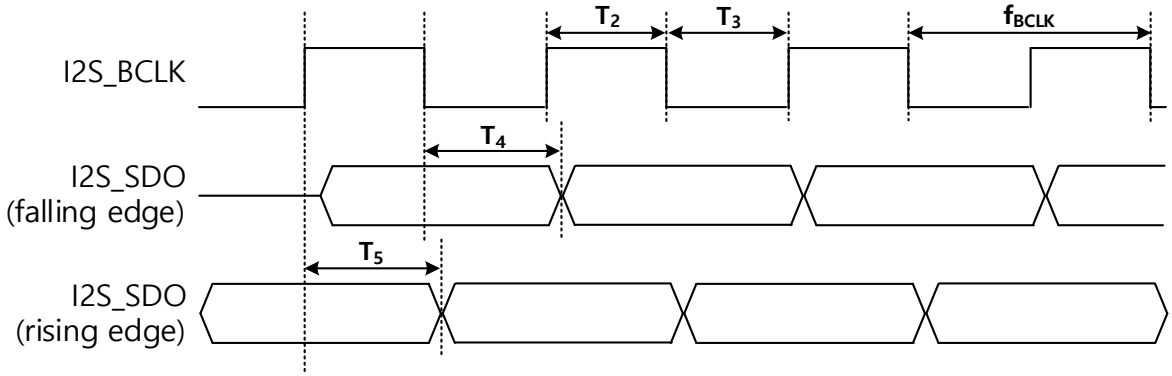

Figure 43: I2S Transmit Timing Diagram

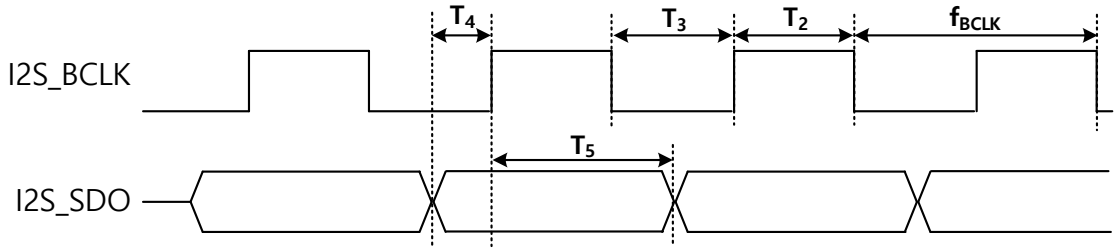

Figure 44: I2S Receive Timing Diagram

Table 51: I2S Transmit Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO output hold (falling edge)	T_4	160		-	ns
I2S_SDO output hold (rising edge)	T_5	160		-	ns

Table 52: I2S Receive Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO input setup time	T_4	15		-	ns
I2S_SDO input hold time	T_5	60		-	ns

9.8 ADC (Aux 12-bit)

9.8.1 Overview

DA16200 includes a high precision, ultra-low power, and wide dynamic range SAR ADC with a 12-bit resolution. It has a 4-channel single-end ADC.

Analog input is measured by four pins from GPIOA0 to GPIOA3, and pin selection is changed through the register setting.

Figure 45 shows the control block diagram.

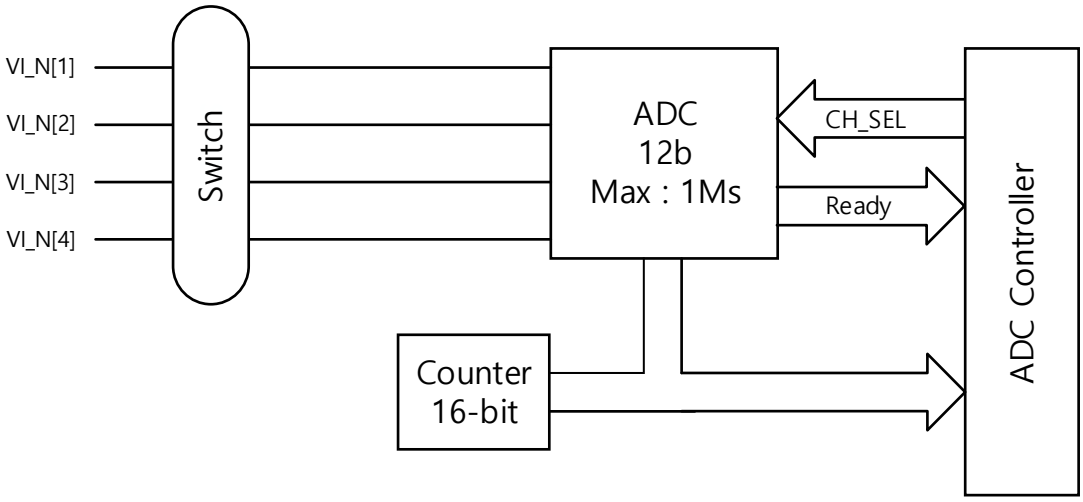

Figure 45: ADC Control Block Diagram

9.8.2 Timing Diagram

The input is digitized at a maximum of 1.0 Msps throughput rate. And the maximum input clock rate is 15 MHz.

Figure 46 shows the conversion timing, and Table 53 describes the DC specifications.

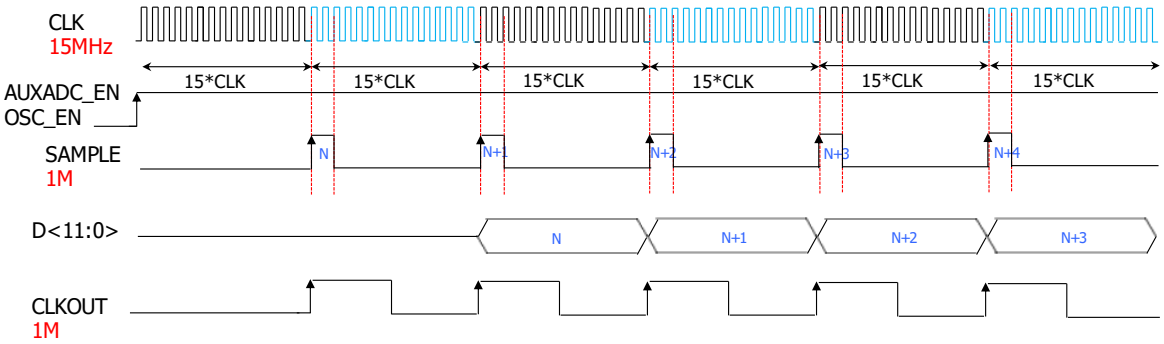

Figure 46: 12-bit ADC Timing Diagram

Table 53: DC Specification

Description	Min	Typ	Max	Unit
Resolution	4	12	12	Bits
Max clock input			15	MHz
Conversion frequency			1	MHz
Accuracy:				
• SNR • SNDR		• 67.2 • 61.7		• dB • dB
Analog input voltage	0		1.4	V
Reference voltage		0.7		V

9.8.3 DMA Transfer

There are four ADC channel settings available. Once the input data of each channel reaches the FIFO level, it is possible to read the data through the DMA path.

9.8.4 Sensor Wake-up

The DA16200 has an external sensor wake-up function that uses the analog input signal through an Aux ADC. Even in Sleep mode 2/3, it detects the change of an external analog signal, wakes up from Sleep mode 2/3, and converts the DA16200 into a normal operation. This function can be used in up to four channels. Also, when multiple external sensors are used, analog signals are detected while the channel are automatically changed. For example, if all four channels are set as input sources which have their threshold register respectively, the channels are measured sequentially from 0 to 3.

If one of the four values exceed the allowed range of values set by the threshold register, the DA16200 awakes from the Sleep mode 2/3. The value setting of the input change can be either over threshold or under threshold.

9.8.5 ADC Ports

Table 54 shows the pin definition of the ADC.

Table 54: ADC Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA3	36	D4	A	Analog signal
GPIOA2	37	B2	A	Analog signal
GPIOA1	38	C3	A	Analog signal
GPIOA0	39	A3	A	Analog signal

9.9 GPIO

All digital pads can be used as GPIO, and each GPIO port is mixed with a multi-functional interface. The GPIO features of DA16200 are listed below:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- Maskable interrupt generation based on input value change
- Possible to be output signal of PWM[3:0], external interrupt, QSPI_CSB[3:1], RF_SW[1:0], and UART_TXDOE[2:0] on the GPIO pins:
  - It provides special functions for GPIO pin use. PWM [3:0], external interrupt, QSPI_CSB [3:1], RF_SW [1:0], and UART_TXDOE [2:0] signals can be output by selecting unused pins among the GPIO pins. It is possible to select the function to be output from the GPIO register setting and select the remaining GPIO pin without using it to output the specific function to the desired GPIO pins

9.9.1 Antenna Switching Diversity

DA16200 provides the antenna switching diversity function for performance improvement in a multi-path environment. A PHY block measures the RSSI of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. To use this function, an external switching element is required, and switching control is done through GPIOs. Two GPIOs can be used for switching control, and for this purpose any unused pins among the GPIO pins can be selected. The control signal can be changed by register setting to suit the external switching device.

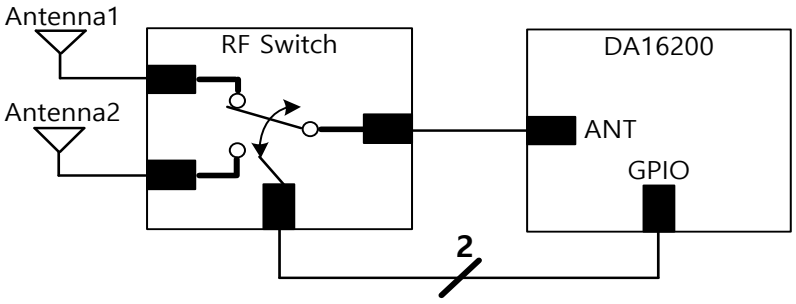

Figure 47: Antenna Switching Internal Block Diagram

If the Antenna Switching Diversity function is enabled, the function is automatically done by PHY hardware block. The basic operation scheme is as follows:

- The antenna's RSSI decision is made for 11b PPDU, except for 11g/n PPDU
- When PHY hardware detects the existence of 11b PPDU, it stores the RSSI
- After the switch to another antenna, the RSSI is stored and a decision is made about which antenna has better RSSI
- This operation is done during 11b PPDU's preamble duration to protect corruption of 11b PPDU data reception
- The decided antenna is not changed until there is a new 11b PPDU

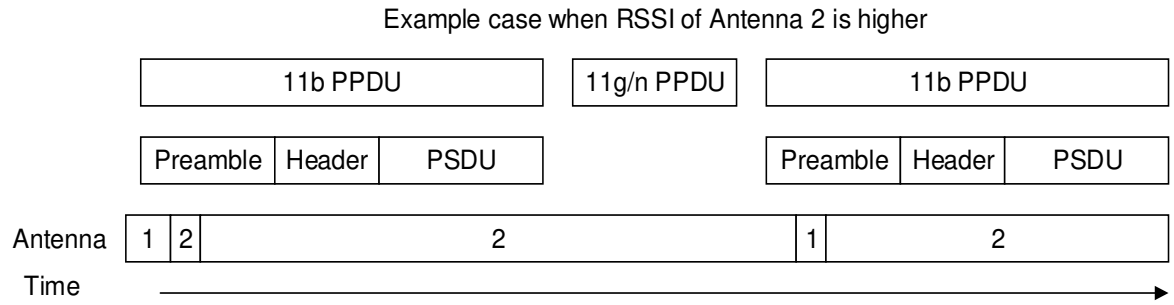

Figure 48: Antenna Switching Timing Diagram

For reference, this antenna switching diversity is different from MRC (Maximum Ratio Combining).

9.10 UART

DA16200 provides three UARTs, features of which are described below:

- Programmable use of UART (UART1 and UART2)
- Supports both byte and word access for reduction of bus burden
- Supports both RS-232 and RS-485
- Separate 32×8 bit transmit and 32×12 bit receive FIFO memory buffers to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop, and parity), which are added prior to transmission and removed on reception
- Independent masking of transmit FIFO, receive FIFO, and receive timeout
- Supports for DMA
- False start bit detection
- Programmable flow control (CTS/RTS, UART1)
- Fully programmable serial interface characteristics:
  - Data can be of 5, 6, 7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1- or 2- stop bit generation
  - Baud rate generation

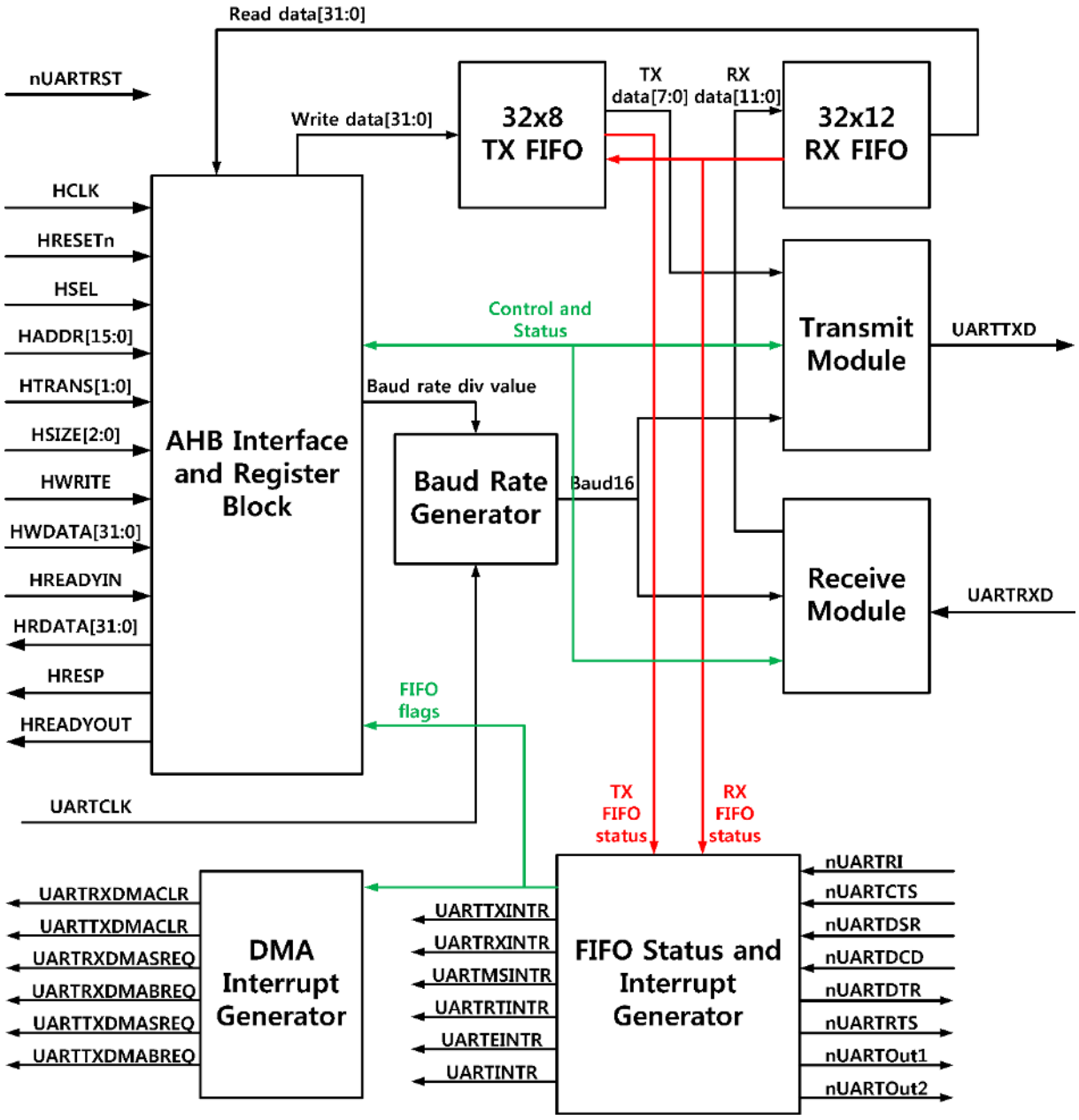

Figure 49: DA16200 UART Block Diagram

9.10.1 RS-232

As the serial communication between the UART and the selected device is asynchronous, additional bits (start and stop) are inserted into the data line to indicate the beginning and end. With these bits, two devices can be synchronized. This structure of serial data accompanied by start and stop bits is referred to as a character, as shown in Figure 50.

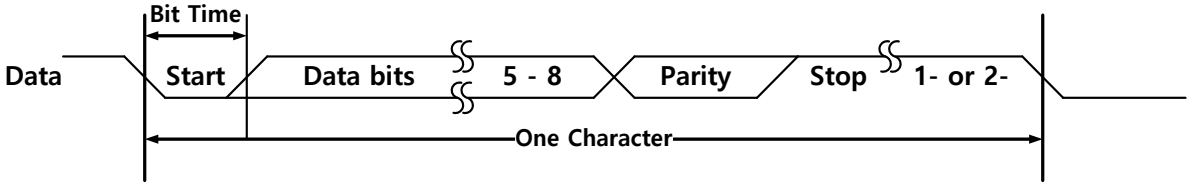

Figure 50: Serial Data Format

An additional parity bit may be added to the serial character. This bit appears between the last data bit and the stop bit(s) in the character structure. It provides the UART with the ability to do simple error checking on the received data.

The UART Line Control Register is used to control the serial character characteristics. The individual bits of the data word are sent after the start bit, starting with the least significant bit (LSB). These are followed by the optional parity bit, followed by the stop bit(s), which can be 1 or 2.

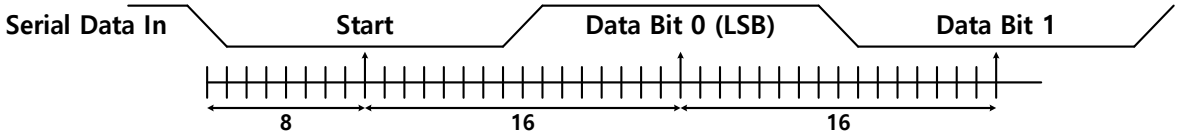

Figure 51: Receiver Serial Data Sampling Points

All the bits in the transmission are transmitted for exactly the same time duration. This is referred to as a Bit Period or Bit Time. One Bit Time equals 16 baud clocks. To ensure stability on the line, the receiver samples the serial input data at approximately the mid-point of the Bit Time, once the start bit has been detected. As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit. Figure 49 shows the sampling points of the first couple of bits in a serial character.

9.10.2 RS-485

DA16200 UART supports RS-485. A UART485EN register (0x054) is required to be assigned to enable the RS-485. In order to use RS-485, an additional signal (UARTTXDOE) is required to notice TXD intervals. This signal can be an output by selecting any of the unused GPIO pins.

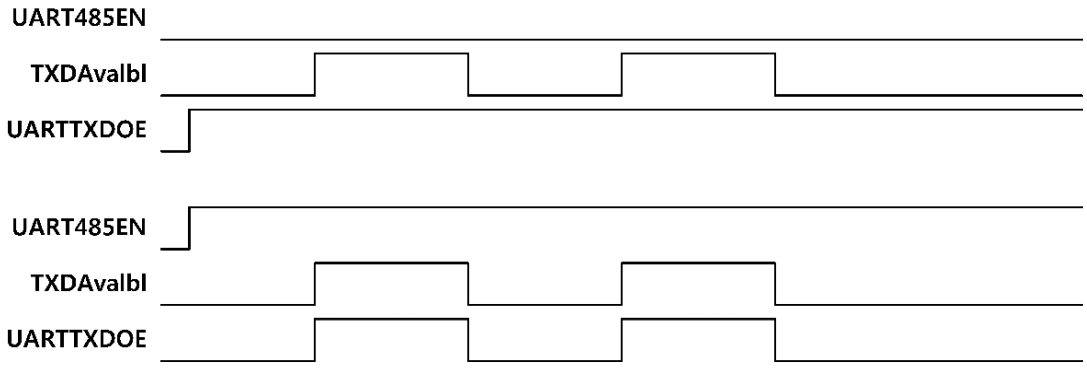

Figure 52: UARTTXDOE Output Signal for UART RS-485

9.10.3 Baud Rate

The UART clock frequency (FUARTCLK) is fixed at 80 MHz. The Baud Rate Divisor can be calculated as (FUARTCLK / (16 x Baud Rate)). The Baud Rate Divisor is comprised of the integer part (UART_INTBRDIV) and fractional part (UART_FRABRDIV). The maximum baud rate of DA16200 UART is 2.5 MBaud.

The example below shows how to calculate the divisor value.

If the required baud rate is 921600 with 80 MHz FUARTCLK, the Baud Rate Divisor becomes:

(8 x 107) / (16 x 921600) = 5.425.

This means that the integer value is 5 and the fractional value is 0.425.

Then, the fraction part becomes integer ((0.425 x 64) + 0.5) = 27.

Then, the generated baud rate divider is 5 + 27/64 = 5.422.

Finally, the generated baud rate becomes (8 x 107) / (16 x 5.422) = 922169.

And the error between the required baud rate and the generated baud rate is:

(922169 – 921600) / 921600 x100 = 0.062 %

9.10.4 Hardware Flow Control

The hardware flow control feature is fully selectable, and serial data flow is controlled by using nUARTRTS output and nUARTCTS input signals. Figure 53 shows how two different UARTs can communicate using hardware flow control.

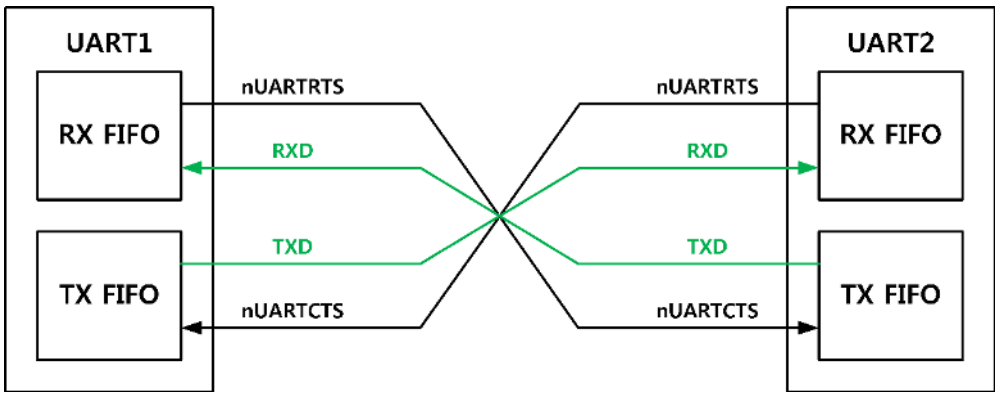

Figure 53: UART Hardware Flow Control

When RTS flow control is enabled, nUARTRTS signal is asserted until the receive FIFO is filled up to programmed level. When CTS flow control is enabled, the transmitter can transmit the data when the nUARTCTS signal is asserted. CTSEn (CTS enable) and RTSEn (RTS enable) bits are determined by 14th (RTS) and 15th bit (CTS) of UARTCR register.

Table 55: Control Bits to Enable and Disable Hardware Flow Control

CTSEn	RTSEn	Description
1	1	Both RTS and CTS flow control are enabled
1	0	Only CTS flow control is enabled
0	1	Only RTS flow control is enabled
0	0	Both RTS and CTS flow control are disabled

9.10.5 Interrupts

The DA16200 UART block provides five interrupt signals by separate interrupt lines. Each interrupt conditions are Modem Status, Receive FIFO Request, Transmit FIFO Request, Receive Timeout and Reception Error. These conditions are logically ORed to provide a single combined interrupt, UARTINTR. Table 56 shows the interrupt signals.

Table 56: UART Interrupt Signals

Signal Name	Description
UARTMSINTR	UART Modem Status Interrupt
UARTRXINTR	UART Receive FIFO Interrupt
UARTTXINTR	UART Transmit FIFO Interrupt
UARTRTINTR	UART Receive Timeout Interrupt
UARTEINTR	UART Error Interrupt
UARTINTR	UART Interrupt. Five Interrupt signals are combined by OR function

9.10.6 DMA Interface

The DA16200 UART block can generate DMA request signals with register settings by using a DMA interrupt generator module to connect to DA16200 DMA Controller (DMA1). The DMA operation of the UART is controlled with the DMA Control Register.

The DA16200 UART provides four DMA signals and receives two DMA signals, two signals to transmit (TXDMASREQ, TXDMABREQ), which are cleared by a TX clear signal (TXDMACLR) and two signals to receive (RXDMASREQ, RXDMABREQ), which are cleared by a RX clear signal (RXDMACLR).

When the DMA interface is not used, the TXDMACLR and RXDMACLR lines should be connected to a logic 0.

Table 57 shows the pin definition of the UART interface.

Table 57: UART Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
UART0_RXD	12	M10	I	UART0_RXD
UART0_TXD	11	L9	O	UART0_TXD
GPIOA7	31	E1	I	UART1_RXD
GPIOA5	33	D2	I	
GPIOA3	36	D4	I	
GPIOA1	38	C3	I	
GPIOA6	32	E3	O	UART1_TXD
GPIOA4	34	F4	O	
GPIOA2	37	B2	O	
GPIOA0	39	A3	O	
GPIOA5	33	D2	I	UART1_CTS
GPIOA4	34	F4	O	UART1_RTS
GPIOA11	27	G1	I	UART2_RXD
GPIOC7	9	K12	I	

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA10	28	F2	O	UART2_TXD
GPIOC6	10	L11	O	

9.11 PWM

Pulse Width Modulation (PWM) is a modulation technique used to encode a message into a pulse signal. The blocks are designed to adjust output pulse duration by the CPU bus clock (HCLK).

Figure 54 shows the structure of the PWM block.

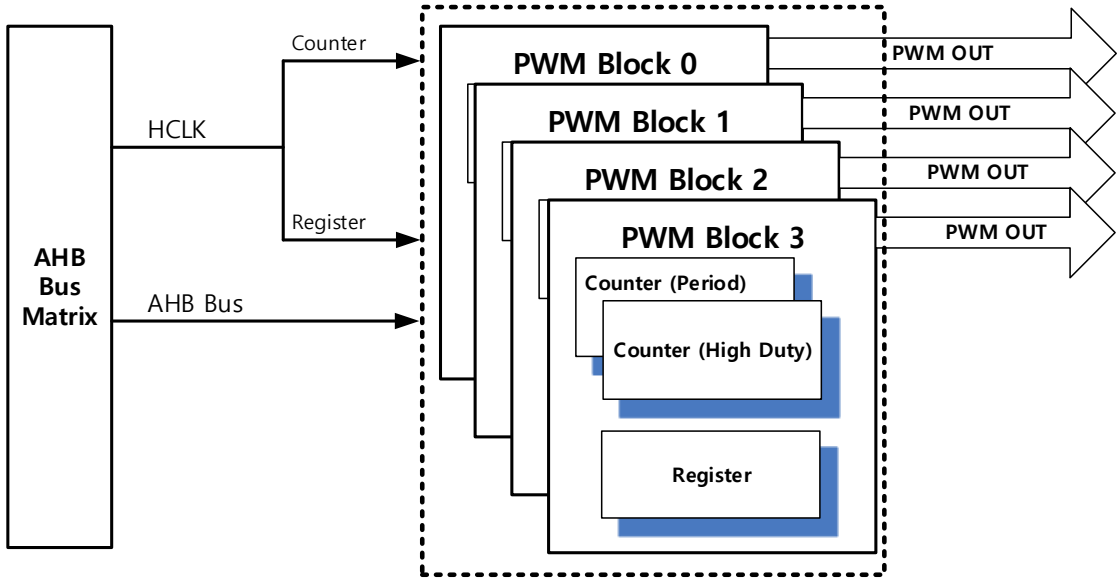

Figure 54: PWM Block Diagram

Table 58 shows the pin definition of the PWM interface. GPIOx means that PWM signals can go out through any GPIO pins via a register setting.

Table 58: PWM Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOx				PWM[3:0] output

9.11.1 Timing Diagram

Table 59 shows the relation between the internal bus clock and PWM output wave patterns. Figure 55 shows the conversion timing diagram. **a** and **b** can be adjusted through the register setting, and PWM wave patterns vary depending on the ratio. **a** controls the high width of pulses (nCycle High), while **b** controls the general cycle (nCycle Period).

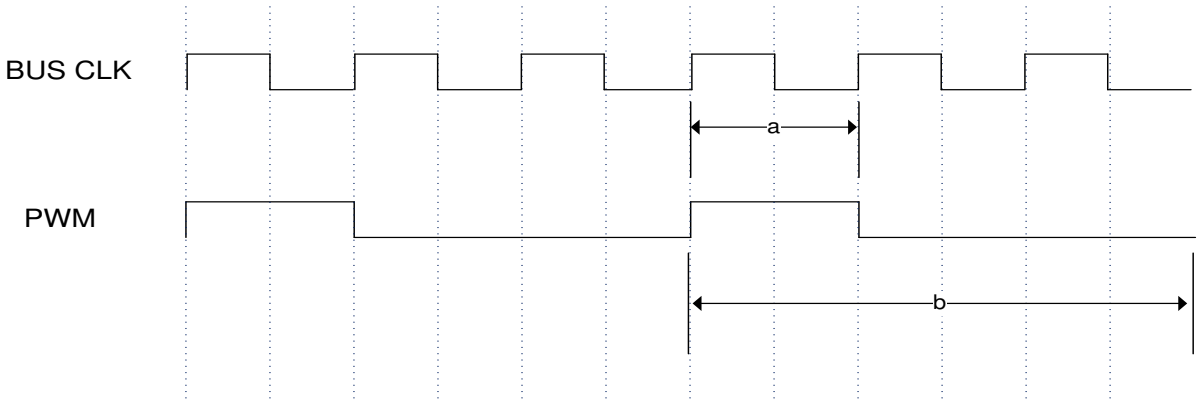

Figure 55: PWM Timing Diagram

Table 59: PWM Timing Diagram Description

Time	Description
a	Bus Clock Period × (nCycle High + 1)
b	Bus Clock Period × (nCycle Period + 1)

9.12 Debug Interface

DA16200 supports both IEEE Standard 1149.1 JTAG (5-wire) and the low-pin-count Arm SWD (2-wire, TCLK/TMS) debug interfaces. The SWD protocol provides the same debug features as JTAG.

The JTAG port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see Ref. [5].

Figure 56 shows the JTAG timing diagram.

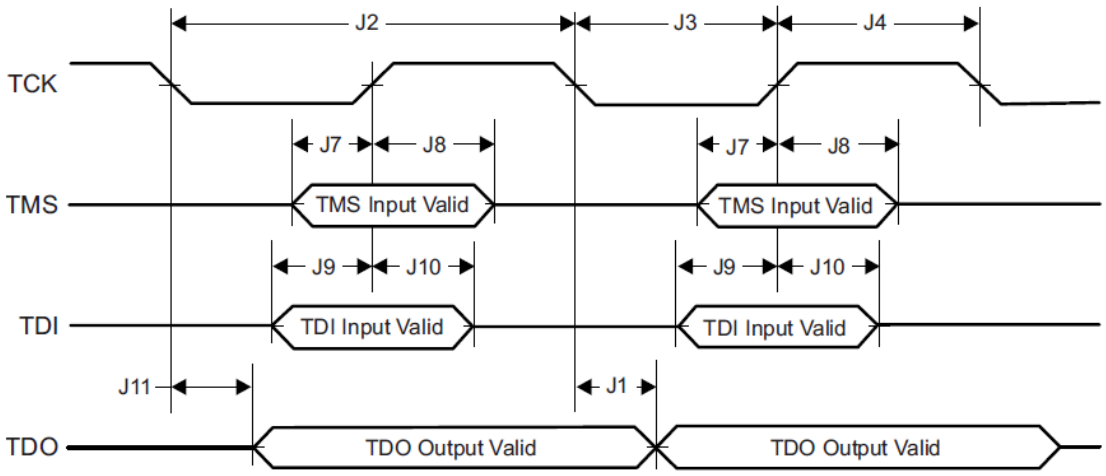

Figure 56: JTAG Timing Diagram

Table 60 shows the JTAG timing parameters.

Table 60: JTAG Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	f_{TCK}	Clock Frequency		15	MHz
J2	t_{TCK}	Clock Period		$1/f_{TCK}$	ns
J3	t_{CL}	Clock Low Period		$t_{TCK}/2$	ns
J4	t_{CH}	Clock High Period		$t_{TCK}/2$	ns
J7	t_{TMS_SU}	TMS Setup Time	1		
J8	t_{TMS_HO}	TMS Hold Time	16		
J9	t_{TDI_SU}	TDI Setup Time	1		
J10	t_{TDI_HO}	TDI Hold Time	16		
J11	t_{TDO_HO}	TDO Hold Time		15	

Table 61 shows the pin definition of the JTAG interface.

Table 61: JTAG Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
TMS (Note 1)	6	J11	I/O	Data
TCLK (Note 2)	7	J9	I	Clock
GPIOC8	8	K10	I	TDI: Data Input
GPIOC7	9	K12	O	TDO: Data Output
GPIOC6	10	L11	I	nTRST: Reset

The SWD protocol provides the same debug features as JTAG.

Note 1 For SWD Debug, TMS = SWDIO, a bidirectional signal.

Note 2 For SWD Debug, TCLK = SWCLK.

9.13 Bluetooth Coexistence

The DA16200 provides a Bluetooth coexistence function to properly coordinate the use of the 2.4 GHz Wi-Fi radio with external devices that also use a 2.4 GHz radio such as Bluetooth.

9.13.1 Interface Configuration

The following three pins can be set in pin multiplexing:

- BT_sig0 (oWlanAct)
  - Output - indicates WLAN is currently active
- BT_sig1 (iBtAct)
  - Input - indicates BT/BLE is currently active
- BT_sig2 (iBTPri)
  - Input (optional) - indicates BT/BLE has higher priority than WLAN

A variety of configuration settings are available, including active high/low, manual force mode, use status of the optional iBTPri function, and whether to switch oWlanAct to active in the event of TX/RX/TRX.

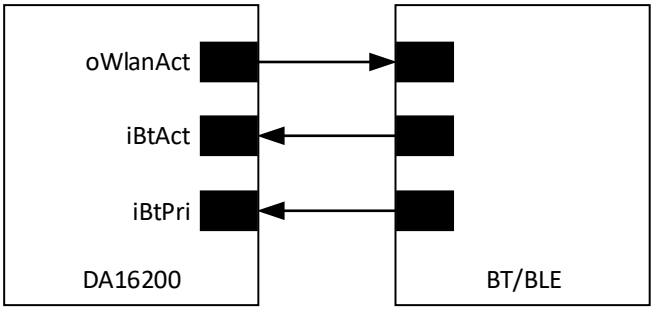

Figure 57: Bluetooth Coexistence Interface

9.13.2 Operation Scenario

Bluetooth coexistence can be enabled/disabled through configuration registers. The activation scenarios based on the status of each pin are described below:

- BT_sig0 (oWlanAct)
  - When asserted, the external BT/BLE device is expected to stop occupying RF
- BT_sig1 (iBtAct)
  - When asserted, DA16200 stops occupying RF
- BT_sig2 (iBTPri)
  - Optional and thus may not be used
  - When iBtPri is active, the DA16200 will stop occupying the RF when iBtAct is active even if a Wi-Fi transmission is in progress

10 Register Map

10.1 GPIO Register

There are 15 GPIOs in DA16200. GPIOA[11:0] and GPIOC[8:6].

The GPIO features for this device are as follows:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- To make a GPIO pin an interrupt pin
- Possible to be output signal of PWM [3:0], external Interrupt, SPI_CSB [3:1], RF_SW [1:0] and UART_TXDOE [1:0] on any GPIO pin

Table 62: GPIO Registers Overview

Address	Register	Description
Common control for GPIO Pin Status		
0x5000_1208	FSEL_GPIO1	Function Selection of the GPIOA [14:0]
0x5000_120C	FSEL_GPIO2	Function Selection of the GPIOB [11:0] and GPIOC [8:0]
0x5000_1220	GPIO_DS	Driving Strength for GPIOA [14:0]
0x5000_1224	GPIO_SR	Slew Rate Control for GPIOA [14:0]
0x5000_1228	GPIO_PE_PS	Pull-up/Pull-down Control for GPIOA [14:0]
0x5000_122C	GPIO_IE_IS	Input enable/CMOS Control for GPIOA [14:0]
0x5000_1234	GPIO1_DS	Driving Strength for GPIOB [11:0]
0x5000_1238	GPIO1_SR	Slew Rate Control for GPIOB [11:0]
0x5000_123C	GPIO1_PE_PS	Pull-up/Pull-down Control for GPIOB [11:0]
0x5000_1240	GPIO1_IE_IS	Input enable/CMOS Control for GPIOB [11:0]
0x5000_1244	GPIO2_DS	Driving Strength for GPIOC [8:0]
0x5000_1248	GPIO2_SR	Slew Rate Control for GPIOC [8:0]
0x5000_124C	GPIO2_PE_PS	Pull-up/Pull-down Control for GPIOC [8:0]
0x5000_1250	GPIO2_IE_IS	Input enable/CMOS Control for GPIOC [8:0]
GPIO In/Out control		
0x4001_0000	DataIn0	GPIOA Input value
0x4001_0004	DataOut0	GPIOA Output value
0x4001_0008	Reserved	
0x4001_000C	Reserved	
0x4001_0010	DataOut_Set0	GPIOA Data output enable set
0x4001_0014	DataOut_Clr0	GPIOA Data output clear
0x4001_0018	AltFunc_Set0	GPIOA Alternate Function output enable set
0x4001_001C	AltFunc_Clr0	GPIOA Alternate Function output clear
0x4001_0020	IntrEn_Set0	GPIOA Interrupt Enable set
0x4001_0024	IntrEn_Clr0	GPIOA Interrupt Enable clear

Address	Register	Description
0x4001_0028	IntrType_Set0	GPIOA Interrupt Type set
0x4001_002C	IntrType_Clr0	GPIOA Interrupt Type clear
0x4001_0030	IntrPol_Set0	GPIOA Interrupt Polarity set
0x4001_0034	IntrPol_Clr0	GPIOA Interrupt Polarity clear
0x4001_0038	IntrStatus0	GPIOA Interrupt Status
0x4001_003C	Func_Out_En0	Alternate Function output enable for GPIOA
0x4001_0FC0	PWM_OutSel0	PWM_OUT[3:0] port selection for GPIOA
0x4001_0FC4	mSPI_CS_OutSel0	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOA
0x4001_0FC8	RF_SW_OutSel0	RF_SW[2:1] port selection for GPIOA
0x4001_0FCC	UART_OutSel0	UART_TXDOE[3:0] port selection for GPIOA
0x4001_1000	DataIn1	GPIOB Input value
0x4001_1004	DataOut1	GPIOB Output value
0x4001_1008	Reserved	
0x4001_100C	Reserved	
0x4001_1010	DataOut_Set1	GPIOB Data output enable set
0x4001_1014	DataOut_Clr1	GPIOB Data output clear
0x4001_1018	AltFunc_Set1	GPIOB Alternate Function output enable set
0x4001_101C	AltFunc_Clr1	GPIOB Alternate Function output clear
0x4001_1020	IntrEn_Set1	GPIOB Interrupt Enable set
0x4001_1024	IntrEn_Clr1	GPIOB Interrupt Enable clear
0x4001_1028	IntrType_Set1	GPIOB Interrupt Type set
0x4001_102C	IntrType_Clr1	GPIOB Interrupt Type clear
0x4001_1030	IntrPol_Set1	GPIOB Interrupt Polarity set
0x4001_1034	IntrPol_Clr1	GPIOB Interrupt Polarity clear
0x4001_1038	IntrStatus1	GPIOB Interrupt Status
0x4001_103C	Func_Out_En1	Alternate Function output enable for GPIOB
0x4001_1FC0	PWM_OutSel1	PWM_OUT[3:0] port selection for GPIOB
0x4001_1FC4	mSPI_CS_OutSel1	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOB
0x4001_1FC8	RF_SW_OutSel1	RF_SW[2:1] port selection for GPIOB
0x4001_1FCC	UART_OutSel1	UART_TXDOE[3:0] port selection for GPIOB
0x4001_7000	DataIn2	GPIOC Input value
0x4001_7004	DataOut2	GPIOC Output value
0x4001_7008	Reserved	
0x4001_700C	Reserved	
0x4001_7010	DataOut_Set2	GPIOC Data output enable set
0x4001_7014	DataOut_Clr2	GPIOC Data output clear
0x4001_7018	AltFunc_Set2	GPIOC Alternate Function output enable set
0x4001_701C	AltFunc_Clr2	GPIOC Alternate Function output clear
0x4001_7020	IntrEn_Set2	GPIOC Interrupt Enable set

Address	Register	Description
0x4001_7024	IntrEn_Clr2	GPIOC Interrupt Enable clear
0x4001_7028	IntrType_Set2	GPIOC Interrupt Type set
0x4001_702C	IntrType_Clr2	GPIOC Interrupt Type clear
0x4001_7030	IntrPol_Set2	GPIOC Interrupt Polarity set
0x4001_7034	IntrPol_Clr2	GPIOC Interrupt Polarity clear
0x4001_7038	IntrStatus2	GPIOC Interrupt Status
0x4001_703C	Func_Out_En2	Alternate Function output enable for GPIOC
0x4001_7FC0	PWM_OutSel2	PWM_OUT[3:0] port selection for GPIOC
0x4001_7FC4	mSPI_CS_OutSel2	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOC
0x4001_7FC8	RF_SW_OutSel2	RF_SW[2:1] port selection for GPIOC
0x4001_7FCC	UART_OutSel2	UART_TXDOE[3:0] port selection for GPIOC

Table 63: FSEL_GPIO1 (0x5000_1208)

Bit	Mode	Symbol	Description	Reset
31:30	R/W		Pin function selection for GPIOA[15]	0x3F61_1389
29:28	R/W		Pin function selection for GPIOA[14]	
27:26	R/W		Pin function selection for GPIOA[13]	
25:24	R/W		Pin function selection for GPIOA[12]	
22:20	R/W		Pin function selection for GPIOA[11:10]	
19:16	R/W		Pin function selection for GPIOA[9:8]	
15:12	R/W		Pin function selection for GPIOA[7:6]	
11:8	R/W		Pin function selection for GPIOA[5:4]	
7:4	R/W		Pin function selection for GPIOA[3:2]	
3:0	R/W		Pin function selection for GPIOA[1:0]	

* See Table 131.

Table 64: FSEL_GPIO2 (0x5000_120C)

Bit	Mode	Symbol	Description	Reset
21:20	R/W	-	Pin function selection for GPIOC[8:6]	0x002E_AA00
19:7	R/W	-	Reserved	
6:4	R/W		Pin function selection for GPIOC[14:13]	
3:0	R/W		Pin function selection for GPIOC[12:9]	

* See Table 132.

Table 65: GPIO_DS (0x5000_1220)

Bit	Mode	Symbol	Description	Reset
29:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [29:28] GPIOA14	0x5555_5555

Bit	Mode	Symbol	Description	Reset
			[27:26] GPIOA13 [25:24] GPIOA12 [23:22] GPIOA11 [21:20] GPIOA10 [19:18] GPIOA9 [17:16] GPIOA8 [15:14] GPIOA7 [13:12] GPIOA6 [11:10] GPIOA5 [9:8] GPIOA4 [7:6] GPIOA3 [5:4] GPIOA2 [3:2] GPIOA1 [1:0] GPIOA0	

Table 66: GPIO_SR (0x5000_1224)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x0000

Table 67: GPIO_PE_PS (0x5000_1228)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Pull-Up/Pull-Down Enable (active high) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0xFFFF
15:0	R/W	-	Pull Selection, Pull-Up = 1 Pull-Down =0 [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x0000

Table 68: GPIO_IE_IS (0x5000_122C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Input Enable (active high, default = 1)	0x7FFF

Bit	Mode	Symbol	Description	Reset
			[30] GPIOA14 [29] GPIOA13 … [17] GPIOA1 [16] GPIOA0	
15:0	R/W	-	Input Selection: 0 CMOS, 1: Schmitt (default = 1) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x7FFF

Table 69: GPIO1_DS (0x5000_1234)

Bit	Mode	Symbol	Description	Reset
23:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [23:22] GPIOB11 [21:20] GPIOB10 [19:18] GPIOB9 [17:16] GPIOB8 [15:14] GPIOB7 [13:12] GPIOB6 [11:10] GPIOB5 [9:8] GPIOB4 [7:6] GPIOB3 [5:4] GPIOB2 [3:2] GPIOB1 [1:0] GPIOB0	0x0055_5555

Table 70: GPIO1_SR (0x5000_1238)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0000

Table 71: GPIO1_PE_PS (0x5000_123C)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Pull-Up/Pull-Down Enable (active high) [27] GPIOB11	0x0FFF

Bit	Mode	Symbol	Description	Reset
			[26] GPIOB10 … [17] GPIOB1 [16] GPIOB0	
11:0	R/W	-	Pull Selection, Pull-Up = 1, Pull-Down =0 [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0000

Table 72: GPIO1_IE_IS (0x5000_1240)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Input Enable (active high, default = 1) [27] GPIOB11 [26] GPIOB10 … [17] GPIOB1 [16] GPIOB0	0x0FFF
11:0	R/W	-	Input Selection: 0 CMOS 1: Schmitt (default = 1) [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0FFF

Table 73: GPIO2_DS (0x5000_1244)

Bit	Mode	Symbol	Description	Reset
17:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [17:16] GPIOC8 [15:14] GPIOC7 [13:12] GPIOC6 [11:10] GPIOC5 [9:8] GPIOC4 [7:6] GPIOC3 [5:4] GPIOC2 [3:2] GPIOC1 [1:0] GPIOC0	0x0001_5555

Table 74: GPIO2_SR (0x5000_1248)

Bit	Mode	Symbol	Description	Reset
8:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1 [0] GPIOC0	0x0000

Table 75: GPIO2_PE_PS (0x5000_124C)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Pull-Up/Down Enable (active high) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Pull Selection, Pull-Up = 1, Pull-Down =0 [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1 [0] GPIOC0	0x0000

Table 76: GPIO2_IE_IS (0x5000_1250)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Input Enable (active high, default = 1) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Input Selection: 0 CMOS 1: Schmitt (default = 1) [8] GPIOC8 [7] GPIOC7 … [1] GPIOB1 [0] GPIOB0	0x01FF

Table 77: DataIn0 (0x4001_0000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOA Input Data	0x0000

Table 78: DataOut0 (0x4001_0004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Output Data	0x0000

Table 79: DataOut_Set0 (0x4001_0010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 80: DataOut_Clr0 (0x4001_0014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Data Output clear 1 = Output clear	0x0000

Table 81: AltFunc_Set0 (0x4001_0018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Alternate Function Output enable set 1 = Output enable 0 = Disable	0x0000

Table 82: AltFunc_Clr0 (0x4001_001C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Alternate Function Output clear 1 = Output clear	0x0000

Table 83: IntrEn_Set0 (0x4001_0020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt set 1 = Interrupt enable 0 = disable	0x0000

Table 84: IntrEn_Clr0 (0x4001_0024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt clear 1 = Interrupt clear	0x0000

Table 85: IntrType_Set0 (0x4001_0028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt Type set 1: Edge 0: Level	0x0000

Table 86: IntrType_Clr0 (0x4001_002C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt Type clear	0x0000

Table 87: IntrPol_Set0 (0x4001_0030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt Polarity set 1: Active high 0: Active low	0x0000

Table 88: IntrPol_Clr0 (0x4001_0034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt Polarity clear	0x0000

Table 89: IntrStatus0 (0x4001_0038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt Status	0x0000

Table 90: Func_Out_En0 (0x4001_003C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOA 1 = Enable 0 = Disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 91: PWM_OutSel0 (0x4001_0FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOA [15:12]: port selection of the PWM_OUT[3] [11: 8]: port selection of the PWM_OUT[2] [7: 4]: port selection of the PWM_OUT[1] [3: 0]: port selection of the PWM_OUT[0]	0x0000

Table 92: mSPI_CS_OutSel0 (0x4001_0FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOA [15:12]: port selection of the mSPI_CSB[3] [11: 8]: port selection of the mSPI_CSB[2] [7: 4]: port selection of the mSPI_CSB[1] [3: 0]: port selection of the Ext_Intr	0x0000

Table 93: RF_SW_OutSel0 (0x4001_0FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOA [7: 4]: port selection of the RF_SW2 [3: 0]: port selection of the RF_SW1	0x0000

Table 94: UART_OutSel0 (0x4001_0FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOA [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE [3: 0]: Port selection of the UART0_TXDOE	0x0000

Table 95: DataIn1 (0x4001_1000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOB Input Data	0x0000

Table 96: DataOut1 (0x4001_1004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Output Data	0x0000

Table 97: DataOut_Set1 (0x4001_1010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 98: DataOut_Clr1 (0x4001_1014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Data Output clear 1 = Output clear	0x0000

Table 99: AltFunc_Set1 (0x4001_1018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Alternate Function Output enable set 1 = Output enable	0x0000

Bit	Mode	Symbol	Description	Reset
			0 = Disable	

Table 100: AltFunc_Clr1 (0x4001_101C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Alternate Function Output clear 1 = Output clear	0x0000

Table 101: IntrEn_Set1 (0x4001_1020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt set 1 = Interrupt enable 0 = Disable	0x0000

Table 102: IntrEn_Clr1 (0x4001_1024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt clear 1 = Interrupt clear	0x0000

Table 103: IntrType_Set1 (0x4001_1028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt Type set 1: Edge 0: Level	0x0000

Table 104: IntrType_Clr1 (0x4001_102C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt Type clear	0x0000

Table 105: IntrPol_Set1 (0x4001_1030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt Polarity set 1: Active high 0: Active low	0x0000

Table 106: IntrPol_Clr1 (0x4001_1034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt Polarity clear	0x0000

Table 107: IntrStatus1 (0x4001_1038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt Status	0x0000

Table 108: Func_Out_En1 (0x4001_103C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOB 1 = Enable 0 = Disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 109: PWM_OutSel1 (0x4001_1FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOB [15:12]: Port selection of the PWM_OUT[3] [11: 8]: Port selection of the PWM_OUT[2] [7: 4]: Port selection of the PWM_OUT[1] [3: 0]: Port selection of the PWM_OUT[0]	0x0000

Table 110: mSPI_CS_OutSel1 (0x4001_1FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOB [15:12]: Port selection of the mSPI_CSB[3] [11: 8]: Port selection of the mSPI_CSB[2] [7: 4]: Port selection of the mSPI_CSB[1] [3: 0]: Port selection of the Ext_Intr	0x0000

Table 111: RF_SW_OutSel1 (0x4001_1FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOB [7: 4]: Port selection of the RF_SW2 [3: 0]: Port selection of the RF_SW1	0x0000

Table 112: UART_OutSel1 (0x4001_1FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOB [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE	0x0000

Bit	Mode	Symbol	Description	Reset
			[3: 0]: Port selection of the UART0_TXDOE	

Table 113: DataIn2 (0x4001_7000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOC Input Data	0x0000

Table 114: DataOut2 (0x4001_7004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Output Data	0x0000

Table 115: DataOut_Set2 (0x4001_7010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 116: DataOut_Clr2 (0x4001_7014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Data Output clear 1 = Output clear	0x0000

Table 117: AltFunc_Set2 (0x4001_7018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Alternate Function Output enable set 1 = Output enable 0 = Disable	0x0000

Table 118: AltFunc_Clr2 (0x4001_701C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Alternate Function Output clear 1 = Output clear	0x0000

Table 119: IntrEn_Set2 (0x4001_7020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt set 1 = Interrupt enable 0 = Disable	0x0000

Table 120: IntrEn_Clr2 (0x4001_7024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt clear 1 = Interrupt clear	0x0000

Table 121: IntrType_Set2 (0x4001_7028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt Type set 1: Edge 0: Level	0x0000

Table 122: IntrType_Clr2 (0x4001_702C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt Type clear	0x0000

Table 123: IntrPol_Set2 (0x4001_7030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt Polarity set 1: Active high 0: Active low	0x0000

Table 124: IntrPol_Clr2 (0x4001_7034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt Polarity clear	0x0000

Table 125: IntrStatus2 (0x4001_7038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt Status	0x0000

Table 126: Func_Out_En2 (0x4001_703C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOC 1 = Enable 0 = Disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 127: PWM_OutSel2 (0x4001_7FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOC [15:12]: Port selection of the PWM_OUT[3] [11: 8]: Port selection of the PWM_OUT[2] [7: 4]: Port selection of the PWM_OUT[1] [3: 0]: Port selection of the PWM_OUT[0]	0x0000

Table 128: mSPI_CS_OutSel2 (0x4001_7FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOC [15:12]: Port selection of the mSPI_CSB[3] [11: 8]: Port selection of the mSPI_CSB[2] [7: 4]: Port selection of the mSPI_CSB[1] [3: 0]: Port selection of the Ext_Intr	0x0000

Table 129: RF_SW_OutSel2 (0x4001_7FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOC [7: 4]: Port selection of the RF_SW2 [3: 0]: Port selection of the RF_SW1	0x0000

Table 130: UART_OutSel2 (0x4001_7FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOC [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE [3: 0]: Port selection of the UART0_TXDOE	0x0000

Table 131: GPIO PIN MUX

Bit Sel	Value										
	0	1	2	3	4	5	6	7	8	9	10
FSEL_GPIO[31:30]	Semi-fixed pin: JTAG_01 TMS TCLK	D_SYS D_SYS_OUT[0] D_SYS_OUT[1]	GPIO(2) x GPIOA[15]	GPIO(2) x GPIOA[15]							
FSEL_GPIO[29:28] FSEL_GPIO[27:26] FSEL_GPIO[25:24]	UART2_01 I2S_CLK_In UART2_RXD UART2_TXD	BT(0:2) BT_sig2 (iBTPri) BT_sig1 (iBtAct) BT_sig0 (oWlanAct)	D_SYS D_SYS_CLK D_SYS_OUT[3] D_SYS_OUT[2]	GPIO(2) GPIOA[14] GPIOA[13] GPIOA[12]							
FSEL_GPIO[22:20]	G(1) + BT GPIOA[11] BT_sig2 (iBTPri)	G(1) + I2S GPIOA[11] I2S_CLK_In	G(1) + eMMC(6) GPIOA[11] mSDeMMC_WRP	sSPI (2:3) sSPI_MOSI sSPI_MISO	UART2 (0:1) UART2_RXD UART2_TXD	mSPI (4:5) E_SPI_IO3 E_SPI_IO2	GPIO(2) GPIOA[11] GPIOA[10]	GPIO(2) GPIOA[11] GPIOA[10]			
FSEL_GPIO[19:16]	5G control(45) 5GC_Sig[5] 5GC_Sig[4]	sSPI (2:3) sSPI_MOSI sSPI_MISO	eMMC (0:1) mSDeMMC_D0 mSDeMMC_D1	sSDIO (0:1) sSDIO_D0 sSDIO_D1	I2C_master mI2C_CLK mI2C_SDA	BT (0:1) BT_sig1(iBtAct) BT_sig0(oWlanAct)	mSPI (2:3) E_SPI_IO1 E_SPI_IO0	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[9] GPIOA[8]	GPIO(2) GPIOA[9] GPIOA[8]	
FSEL_GPIO[15:12]		sSPI (0:1) sSPI_CLK sSPI_CSB	eMMC (2:3) mSDeMMCIO_D2 mSDeMMCIO_D3	sSDIO (2:3) sSDIO_D2 sSDIO_D3	UART1 (0:1) UART1_RXD UART1_TXD	I2C slave sI2C_CLK sI2C_SDA	mSPI (0:1) E_SPI_CLK E_SPI_CSB	I2S(2:3) I2S_LRCK I2S_SDO	GPIO(2) GPIOA[7] GPIOA[6]	GPIO(2) GPIOA[7] GPIOA[6]	
FSEL_GPIO[11:8]	5G control(01) 5GC_Sig[3] 5GC_Sig[2]	I2C slave sI2C_CLK sI2C_SDA	eMMC (4:5) mSDeMMC_CLK mSDeMMC_CMD	sSDIO (4:5) sSDIO_CLK sSDIO_CMD	UART1 (2:3) UART1_CTS UART1_RTS	I2C master mI2C_CLK mI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[5] GPIOA[4]	GPIO(2) GPIOA[5] GPIOA[4]	
FSEL_GPIO[7:4]	AD12 (2) X (Analog In) X (Analog In)	sSPI (0:1) sSPI_CLK sSPI_CSB	I2S (2:3) I2S_LRCK I2S_SDO	I2C slave sI2C_CLK sI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD		AD12(1) + GPIO(1) GPIO[3] X (Analog In)	AD12(1) + I2S_CLK I2S_CLK_In X (Analog In)	GPIO(2) GPIOA[3] GPIOA[2]	GPIO(2) GPIOA[3] GPIOA[2]	
FSEL_GPIO[3:0]	AD12 (2)	sSPI (2:3)	I2S (0:1)	I2C slave	UART1 (0:1)	I2C master	5G control(01)	AD12(1) + GPIO(1)	AD12(1) + WRP	GPIO(2)	GPIO(2)

	X (Analog In) X (Analog In)	sSPI_MOSI sSPI_MISO	I2S_MCLK I2S_BCLK	sI2C_CLK sI2C_SDA	UART1_RXD UART1_TXD	mI2C_CLK mI2C_SDA	5GC_Sig[1] 5GC_Sig[0]	GPIO[1] X (Analog In)	mSDeMMC_WRP X (Analog In)	GPIOA[1] GPIOA[0]	GPIO[1] GPIO[0]

Table 132: GPIO2 PIN MUX

Bit Sel	Value					
	0	1	2	3	4	5
FSEL_GPIO2[21:20]	JTAG(2:3) TDI TDO nTRST	G(1) + UART2 (0:1) GPIO[8] UART2_RXD UART2_TXD	GPIO(2) GPIOC[8] GPIOC[7] GPIOC[6]			
FSEL_GPIO2[6:4]	QSPI (4:5) F_IO3 (F_HOLD) F_IO2 (F_WP)	UART2 (0:1) UART2_TXD UART2_RXD		sSDIO(4:5) sSDIO_D3 sSDIO_D2	GPIO(2) GPIOC[14] GPIOC[13]	GPIO(2) GPIOC[14] GPIOC[13]
FSEL_GPIO2[3:0]	QSPI (3:0) F_IO1 (F_SI) F_IO0 (F_SO) F_CLK F_CSB[1]	sSPI (3:0) sSPI_MISO sSPI_MOSI sSPI_CLK sSPI_CSB	I2S(0:3) I2S_SDO I2S_LRCK I2S_MCLK I2S_BCLK	sSDIO(0:3) sSDIO_D1 sSDIO_D0 sSDIO_CLK sSDIO_CMD	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]

10.2 UART Register

There are three UARTs in DA162000. UART0 is a dedicated port for the debug console. The two other UARTs, namely UART1 and UART2, are available to the user. HW flow control is possible at UART1 but not at UART2.

RS485 and RS232 are supported in DA16200. The specifications supported for RS232 and RS485 are summarized as follows:

Table 133: UART Feature Specification

Specification	RS-232	RS-485
Differential	No	Yes
Operation Mode	Full duplex	Half duplex
Maximum Baud Rate	921600 Baud	5M Baud
Flow Control	Support	Support

Note 1 See the UART section in SDK Programmer's Guide [2] for the pin configurations of the UARTs.

The base address of each UART is:

- UART0: 4001_2XXX
- UART1: 4000_7XXX
- UART2: 4000_9XXX

Note 1 All UARTs have the same bit map.

Table 134: UART Registers Overview

Offset	Register	Description
0x000	UART_DATA	UART Data Register
0x004	UART_RXSTS / UART_ERRCLR	UART Receive Status Register Error Clear Register
0x018	UART_FLAG	UART Flag Register
0x024	UART_INTBRDIV	UART Integer Baud Rate Divisor Register
0x028	UART_FRABRDIV	UART Fractional Baud Rate Divisor Register
0x02C	UART_LCNTRL	UART Line Control Register
0x030	UART_CNTRL	UART Control Register
0x034	UART_INTFLS	UART Interrupt FIFO Level Select Register
0x038	UART_INTMSKSC	UART Interrupt Mask Set/Clear Register
0x040	UART_INTMSKSTS	UART Masked Interrupt Status Register
0x044	UART_INTCLR	UART Interrupt Clear Register
0x048	UART_DMACNTRL	UART DMA Control Register
0x04C	UART_WAEN	UART Word Access Enable Register
0x054	UART_485EN	UART RS-485 Mode Enable Register

Table 135: UART_DATA (0x000)

Bit	Mode	Symbol	Description	Reset
15:12	-	-	Reserved	0x0

Bit	Mode	Symbol	Description	Reset
11:8	RO	-	Error status for data read. These bits cannot be read when UART_WAEN is enabled. [11] Overrun Error [10] Break Error [9] Parity Error [8] Framing Error	0x0
7:0	R/W	DATA	Receive data bits for data read Transmit data bits for data write	0x00

Table 136: UART_RXSTS / UART_ERRCLR (0x004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:0	WO	-	UART_ERRCLR, A write to this register clears every error. The value is not important	0x00
7:4	RO	-	UART_RXSTS, Reserved	0x0
3:0	RO	-	UART_RXSTS, UART error status [3] Overrun error [2] Break error [1] Parity error [0] Framing error	0x0

Table 137: UART_FLAG (0x018)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:4	RO	-	The status of FIFOs [7] TXFE, Transmit FIFO empty [6] RXFF, Receive FIFO full [5] TXFF, Transmit FIFO full [4] RXFE, Receive FIFO empty	0x9
3	RO	BUSY	UART busy. This bit is set to 1 as soon as the transmit FIFO becomes non-empty	0x0
2:0	-	-	Reserved	0x0

Table 138: UART_INTBRDIV (0x024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IBRD	Integer baud rate divisor	0x0000

Table 139: UART_FRABRDIV (0x028)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:0	R/W	FBRD	Fractional baud rate divisor	0x00

Table 140: UART_LCNTRL (0x02C)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7	R/W	SPS	Stick parity select 0 = Stick parity disabled 1 = Either * If PARSEL bit is 0, the parity bit is transmitted and checked as a 1 * If PARSEL bit is 1, the parity bit is transmitted and checked as a 0	0x0
6:5	R/W	DTLEN	The number of data bits transmitted or received in a frame. b'11 = 8 bits b'10 = 7 bits b'01 = 6 bits b'00 = 5 bits	0x0
4	R/W	FIFOEn	FIFO Enable 0 = UART FIFO disabled 1 = UART Transmit and Receive FIFO enabled	0x0
3	R/W	TSTP	Two stop bits select 0 = Two bits are transmitted as stop bit 1 = One bit is transmitted as stop bit	0x0
2	R/W	PARSEL	Parity select: 0 = Odd parity 1 = Even parity	0x0
1	R/W	PAREn	Parity enable: 0 = Parity is disabled 1 = Parity is enabled	0x0
0	-		Reserved	0x0

Table 141: UART_CNTRL (0x030)

Bit	Mode	Symbol	Description	Reset
15	R/W	CTSEn	UART CTS hardware flow control enable 0 = CTS hardware flow control disabled 1 = CTS hardware flow control enabled	0x0
14	R/W	RTSEn	UART RTS hardware flow control enable 0 = RTS hardware flow control disabled 1 = RTS hardware flow control enabled	0x0
13:10	-	-	Reserved	0x0
9	R/W	RXEn	Receive enable 0 = Receive section of the UART disabled 1 = Receive section of the UART enabled	0x1
8	R/W	TXEn	Transmit enable 0 = Transmit section of the UART disabled 1 = Transmit section of the UART enabled	0x1

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	0x00
0	R/W	UARTEn	UART enable 0 = UART is disabled 1 = UART is enabled	0x0

Table 142: UART_INTFLS (0x034)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:3	R/W	RXIFLS	UART receive interrupt FIFO level select. The receive interrupt occurs as follows: b'000 = Receive FIFO ≥ 1/8 full b'001 = Receive FIFO ≥ 1/4 full b'010 = Receive FIFO ≥ 1/2 full b'011 = Receive FIFO ≥ 3/4 full b'100 = Receive FIFO ≥ 7/8 full b'101 b'111 = Reserved	0b010
2:0	R/W	TXIFLS	UART transmit interrupt FIFO level select. The transmit interrupt occurs as follows: b'000 = Transmit FIFO ≤ 1/8 full b'001 = Transmit FIFO ≤ 1/4 full b'010 = Transmit FIFO ≤ 1/2 full b'011 = Transmit FIFO ≤ 3/4 full b'100 = Transmit FIFO ≤ 7/8 full b'101 b'111 = Reserved	0b010

Table 143: UART_INTMSKSC (0x038)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	R/W	RXTIM	Receive timeout interrupt mask	0x0
5	R/W	TXIM	Transmit interrupt mask	0x0
4	R/W	RXIM	Receive interrupt mask	0x0
3:0	-	-	Reserved	0x0

Table 144: UART_INTMSKSTS (0x040)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	RO	-	Error interrupt mask [10] = Overrun error interrupt mask	0x0

Bit	Mode	Symbol	Description	Reset
			[9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	
6	RO	RXTIMS	Receive timeout masked interrupt status	0x0
5	RO	TXIMS	Transmit masked interrupt status	0x0
4	RO	RXIMS	Receive masked interrupt status	0x0
3:0	-	-	Reserved	0x0

Table 145: UART_INTCLR (0x044)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	WO	-	Error interrupt mask [10] = Overrun error interrupt clear [9] = Break error interrupt clear [8] = Parity error interrupt clear [7] = Framing error interrupt clear	0x0
6	WO	RXTICLR	Receive timeout interrupt clear	0x0
5	WO	TXICLR	Transmit interrupt clear	0x0
4	WO	RXICLR	Receive interrupt clear	0x0
3:0	-	-	Reserved	0x0

Table 146: UART_DMACNTRL (0x048)

Bit	Mode	Symbol	Description	Reset
15:2	-	-	Reserved	0x0000
1	R/W	TXDMAEn	Transmit DMA enable 0 = Transmit DMA is disabled 1 = Transmit DMA is enabled	0x0
0	R/W	RXDMAEn	Receive DMA enable 0 = Receive DMA is disabled 1 = Receive DMA is enabled	0x0

Table 147: UART_WAEN (0x04C)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	WA	UART word access enable register 0 = UART Word Access is disabled 1 = UART Word Access is enabled	0x1

Table 148: UART_485EN (0x054)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	RS485En	UART RS-485 mode enable register	0x0

Bit	Mode	Symbol	Description	Reset
			0 = UART RS-485 mode is disabled 1 = UART RS-485 mode is enabled	

10.3 I2S Register

DA16200 provides an I2S interface that has both I2S transmission and reception functions. However, the transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by setting the register.

When the I2S clock divider register is used, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from the outside with the use of the GPIO pin.

Table 149: I2S Registers Overview

Address	Register	Description
Common control for I2S Pin Status		
0x4001_4000	I2S_CTRL0	I2S Control Register 0
0x4001_4004	I2S_CTRL1	I2S Control Register 1
0x4001_4008	I2S_DATA	I2S Data Register
0x4001_400C	I2S_STATUS	I2S Status Register
0x4001_4010	Reserved	
0x4001_4014	I2S_IMASK	I2S Interrupt Mask Register
0x4001_4018	Reserved	
0x4001_401C	Reserved	
0x4001_4020	I2S_ICR	I2S Rx Overrun Interrupt Clear Register
0x4001_4024	I2S_DMACR	I2S DMA Enable Register
0x5000_1314	I2S_CLK_SEL	I2S Clock divider Register

Table 150: I2S_CTRL0 (0x4001_4000)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	CLK_DIV	I2S_SCLK control factor 4'h0: I2SCLK/2 4'h1: I2SCLK/4 4'h3: I2SCLK/8 4'h7: I2SCLK/16	4'b0011
11	R/W	STEREO	1 = Stereo 0 = Mono	1'b0
10:9	R/W	PCM_BW	PCM bus width for Tx / Rx Tx Rx 2'b11: PCM_24 PCM_32 2'b10: PCM_20 PCM_24/PCM_20 2'b01: PCM_16 PCM_16 2'b00: PCM_8 PCM_8	2'b00
8	R/W	MUTE	If set, SDATA output assert “0”	1'b0

Bit	Mode	Symbol	Description	Reset
7	R/W	HALF_DELAY	Relationship between FS and SCLK 1: Falling edge	1'b0
6	R/W	PCMM	If set, PCM Mode is enabled	1'b1
5	R/W	Right_Align	If set, PCM data output right is enabled	1'b0
4	R/W	ENDIAN	SDATA Output mode 1 = Big endian 0 = Little endian	1'b0
3	R/W	MCLK_INV	If set, MCLK inversion	1'b1
2	R/W	LRCK_INV	If set, LRCK inversion	1'b0
1	R/W	I2S_Enalbe	If set, I2S block is enabled	1'b0
0	R/W	CLK_DOWN	If set, output clock signals, LRCK/BCLK/SCLK, assert “0”	1'b0

Table 151: I2S_CTRL1 (0x4001_4004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	
7	R/W	RxFIFO_Rst	Master Rx FIFO reset 0: Reset 1: Normal	1'b0
6	-	-	Reserved	
5	R/W	Left_Justify	Rx decoding left justified	1'b0
4	R/W	Rx_Mode	Rx decoding edge 0: Rising edge @SCLK 1: Falling edge	1'b0
3	R/W	Mst_RxEn	Master Rx load enable signal 0: Tx enable 1: Rx enable	1'b0
2	-	-	Reserved	
1	R/W	Rx_ChSel	Rx data channel selection 0=Rx decoding only Right channel 1=Rx decoding only Left channel	1'b0
0	R/W	LR_ChSel	Left/Right Channel selection 1: First data comes out LRCK high 0: First data comes out LRCK low duration	1'b0

Table 152: I2S_DATA (0x4001_4008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	I2S_DATA	I2S_DATA Write data @ Tx Read data @ Rx	32'b0000

Table 153: I2S_STATUS (0x4001_400C)

Bit	Mode	Symbol	Description	Reset
5:0	R	Status	[5]: Rx FIFO Not Empty [4]: Rx FIFO Full [2]: BUSY [1]: Tx FIFO Not FULL [0]: Tx FIFO EMPTY	

Table 154: I2S_IMASK (0x4001_4014)

Bit	Mode	Symbol	Description	Reset
3	R/W	TXIM	Tx FIFO Interrupt DMA TX request Mask When TX FIFO arrives at half size. 1 = Enable 0 = Disable	1'b0
2	R/W	RXIM	Rx FIFO Interrupt DMA RX request Mask When RX FIFO arrives at half size. 1 = Enable 0 = Disable	1'b0
1	R/W	RTIM	Rx Receive Timeout Interrupt Mask 1 = Enable 0 = Disable Reserved. Not used.	1'b0
0	R/W	RORIM	Rx Over Run Interrupt DMA RX request Mask When RX FIFO arrives at full size. 1 = Enable 0 = Disable	1'b0

Table 155: I2S_ICR (0x4001_4020)

Bit	Mode	Symbol	Description	Reset
0	R/W	RORIC	Rx Over Run Interrupt DMA RX request Clear	1'b0

Table 156: I2S_DMACR (0x4001_4024)

Bit	Mode	Symbol	Description	Reset
1	R/W	TXDMAE	Tx DMA Enable 1 = Enable 0 = Disable	1'b0
0	R/W	RXDMAE	Rx DMA Enable 1 = Enable 0 = Disable	1'b0

Table 157: I2S_CLK_SEL (0x5000_1314)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	-	FNPLL frequency divider factor register 3'h0: No clock 3'h1: FNPLL 1/2	3'b000

Bit	Mode	Symbol	Description	Reset
			3'h2: FNPLL 1/4 3'h3: FNPLL 1/8	

10.4 SDeMMC Register

The SD/eMMC host IP provides the function for DA16200 to access SD or eMMC cards. This SD/eMMC host IP only supports a 4-bit data bus and the maximum clock rate is 50 MHz.

Table 158: SDeMMC Register

Address	Register	Description
Common control for SDeMMC Pin Status		
0x5003_0000	HIF_CTRL0	Host Interface Control Register
0x5003_0004	HIF_EVNT_CTRL	Event Control & Status Register
0x5003_0008	HIF_INT_CTRL	Interrupt Control & Status Register
0x5003_000C	HIF_CLK_CNT_CTRL	Host Clock Control Count Register
0x5003_0010	HIF_CMD_ARG	Command Arguments
0x5003_0014	HIF_CMD_IDX	Command Index
0x5003_0018	HIF_CMD_ARGQ	Command Arguments Queue
0x5003_001C	HIF_CND_IDXQ	Command Index Queue
0x5003_0020	HIF_PAD_CTRL	Pad Control Register
0x5003_0024	HIF_BLK_LG	Block Length Register
0x5003_0028	HIF_BLK_CNT	Transfer Block Count Register
0x5003_002C		Reserved
0x5003_0030	HIF_RSP_TMO_CNT	Response Time-Out Count Register
0x5003_0034	HIF_RD_TMO_CNT	Read Data Time-Out Count Register
0x5003_0038	HIF_WB_TMO_CNT	Write Busy Time-Out Count Register
0x5003_003C	HIF_RSP_CIX_ST	Response Command Index Status
0x5003_0040	HIF_RSP_ARG_0	Response Argument Status--0
0x5003_0044	HIF_RSP_ARG_1	Response Argument Status -- 1
0x5003_0048	HIF_RSP_ARG_2	Response Argument Status -- 2
0x5003_004C	HIF_RSP_ARG_3	Response Argument Status -- 3
0x5003_0050	HIF_AHB_SA	AHB Starting Address
0x5003_0054	HIF_AHB_EA	AHB End Address
0x5003_0058		Reserved
0x5003_005C		Reserved
0x5003_0060	HIF_BUS_ST	Bus Status Register
0x5003_0064	HIF_SM_ST	CMD/RSP & Data State Machine Status
0x5003_0068	HIF_XTR_CNT	Transferred Data Block Count Status
0x5003_006C	HIF_ERR_CNT	Error Data Block Count Status

Table 159: HIF_CTRL0 (0x5003_0000)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	ALL_RST	Reset All H/W Circuit Control 0: Normal Operation 1: Reset	1'b0
14	R/W	HIF_RST	Control Register and H/W Circuit Control 0: Normal Operation 1: Reset	1'b0
13	R/W	CSM_RST	Command State Machine Reset Control 0: Normal Operation 1: Reset	1'b0
12	R/W	DSM_RST	Data State Machine Reset Control 0: Normal Operation 1: Reset	1'b0
11	R/W	STOP_XTR	Immediately Stop the Ongoing Data Transfer 0: Normal Operation 1: Immediately Stop the Ongoing Data Transfer	1'b0
9:8	R/W	WR_STR_CTL[1:0]	Data Transfer Start Control for Write Operation 2'b0x: The starting of write data is triggered by TRIG bit of HIF_CMD_IDX register 2'b10: Not trigger the starting for write data operation 2'b11: Trigger the starting for write data operation	2'b00
7	R/W	HIF_PWR_CTL	Host Interface Power Control 0: Turn-off host interface power 1: Turn-on host interface power	1'b0
6	-	-	Reserved	
5	R/W	CDI_POL_CTL	Card Detect Input Polarity Control 0: Active low 1: Active high	1'b0
4	R/W	RD_CRC_CHK	Read Data CRC Check Control 0: Disable 1: Enable	1'b1
3	R/W	RSP_CRC_CK	Response CRC Check Control 0: Disable 1: Enable	1'b1
2	R/W	BUS_4BIT	4 Bit Data Bus Mode 0: 1-bit Mode 1: 4-bit Mode	1'b0
1	R/W	HIGH_SPD	High Speed Timing Mode 0: Default Speed Timing Mode (SDC and SDATA[3:0] signals output at clock falling edge) 1: High Speed Timing Mode (SDC and SDATA[3:0] signals output at clock rising edge)	1'b0
0	R/W	CDO_MODE	Command/Data Output Mode 0: Open Drain Mode 1: Push-Pull Mode	1'b0

Table 160: HIF_EVNT_CTRL (0x5003_0004)

Bit	Mode	Symbol	Description	Reset
31	R	P_CD_IN_ST	Card Detect Pad Status	1'b0
30	R	P_WP_IN_ST	Write Protect Pad Status	1'b0
29	R/W	CD_IN_EST	Card Detect Event Status 0: No Event Generation 1: Event Generation	1'b0

Bit	Mode	Symbol	Description	Reset
28	R/W	WP_IN_EST	Write Protect Event Status 0: No Event Generation 1: Event Generation	1'b0
27	R/W	XTR_END_EST	Read/Write Data Transfer End Event Status 0: No Event Generation 1: Event Generation	1'b0
26	R/W	BLK_END_EST	Read/Write One Block Data Event Status 0: No Event Generation 1: Event Generation	1'b0
25	R/W	NG_CRCS_EST	Negative Write CRC Status Token Event Status 0: No Event Generation 1: Event Generation	1'b0
24	R/W	WDB_TMO_EST	Write Data Busy Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
23	R/W	RXT_END_EST	Read Data Transfer End Event Status 0: No Event Generation 1: Event Generation	1'b0
22	R/W	SRD_END_EST	Complete to Read Single Block Data Event Status 0: No Event Generation 1: Event Generation	1'b0
21	R/W	RD_CRCE_EST	Read Data CRC Error Event Status 0: No Event Generation 1: Event Generation	1'b0
20	R/W	RD_TMO_EST	Read Data Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_EST	Command/Response End Event Status 0: No Event Generation 1: Event Generation	1'b0
17	R/W	RP_CRCE_EST	Response CRC Error Event Status 0: No Event Generation 1: Event Generation	1'b0
16	R/W	RSP_TMO_EST	Response Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
15:14	-	-	Reserved	
13	R/W	CD_IN_ETE	Card Detect Event Control 0: Disable 1: Enable	1'b0
12	R/W	WP_IN_ETE	Write Protect Event Control 0: Disable	1'b1

Bit	Mode	Symbol	Description	Reset
			1: Enable	
11	R/W	XTR_END_ETE	Read/Write Data Transfer End Event Control 0: Disable 1: Enable	1'b1
10	R/W	BLK_END_ETE	Read/Write One Block Data Event Control 0: Disable 1: Enable	1'b0
9	R/W	NG_CRCS_ETE	Negative Write CRC Status Token Event Control 0: Disable 1: Enable	1'b1
8	R/W	WDB_TMO_ETE	Write Data Busy Time-out Event Control 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_ETE	Read Data CRC Error Event Control 0: Disable 1: Enable	1'b1
4	R/W	RD_TMO_ETE	Read Data Time-out Event Control 0: Disable 1: Enable	1'b1
3	-	-	Reserved	1'b1
2	R/W	RSP_END_ETE	Response End Event Control 0: Disable 1: Enable	1'b1
1	R/W	RP_CRCE_ETE	Response CRC Error Event Control 0: Disable 1: Enable	1'b1
0	R/W	RSP_TMO_ETE	Response Time-out Event Control 0: Disable 1: Enable	1'b1

Table 161: HIF_INT_CTRL (0x5003_0008)

Bit	Mode	Symbol	Description	Reset
31	R	HST_INT_ST	SD/eMMC Host Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
30	-	-	Reserved	1'b0
29	R/W	CD_INT_ST	Card Detect Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
28	R/W	WP_INT_ST	Write Protect Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0

Bit	Mode	Symbol	Description	Reset
27	R/W	XTR_END_IST	Read/Write Data Transfer End Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
26	R/W	BLK_END_IST	Read/Write One Block Data Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
25	R/W	NG_CRCS_IST	Negative Write CRC Status Token Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
24	R/W	WDB_TMO_IST	Write Data Busy Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
23:22	-	-	Reserved	1'b0
21	R/W	RD_CRCE_IST	Read Data CRC Error Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
20	R/W	RD_TMO_IST	Read Data Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_IST	Command/Response End Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
17	R/W	RD_CRCE_IST	Read Data CRC Error Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
16	R/W	RSP_TMO_IST	Response Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
15	R/W	HST_ENT_EN	SD/eMMC Host Interrupt Function Enable Control 0: Disable 1: Enable	1'b0
14	-	-	Reserved	
13	R/W	CD_INT_EN	Card Detect Interrupt Control 0: Disable 1: Enable	1'b0
12	R/W	WP_INT_EN	Write Protect Interrupt Control 0: Disable 1: Enable	1'b0
11	R/W	XTR_INT_EN	Read/Write Data Transfer End Interrupt Control 0: Disable 1: Enable	1'b0
10	R/W	BLK_INT_EN	Read/Write One Block Data Interrupt Control	1'b0

Bit	Mode	Symbol	Description	Reset
			0: Disable 1: Enable	
9	R/W	NG_CRCS_INT	Negative Write CRC Status Token Interrupt Control 0: Disable 1: Enable	1'b0
8	R/W	WDB_TMO_INT	Write Data Busy Time-out Interrupt Control 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_INT	Read Data CRC Error Interrupt Control 0: Disable 1: Enable	1'b0
4	R/W	RD_TMO_INT	Read Data Time-out Interrupt Control 0: Disable 1: Enable	1'b0
3	-	-	Reserved	1'b0
2	R/W	RP_DIRE_INT	Response Direction Bit Error Interrupt Control 0: Disable 1: Enable	1'b0
1	R/W	RP_CRCE_INT	Response CRC Error Interrupt Control 0: Disable 1: Enable	1'b0
0	R/W	RSP_TMO_INT	Response Time-out Interrupt Control 0: Disable 1: Enable	1'b0

Table 162: HIF_CLK_CNT_CTRL (0x5003_000C)

Bit	Mode	Symbol	Description	Reset
31:23	-	-	Reserved	
22	R/W	STOP_HCLK	Enable to Stop SD/eMMC Interface Clock 0: Disable 1: Enable	1'b0
21	R/W	SYNC_STCTL	Synchronous Circuit Stage Control 0: 3-Stage Synchronizer (Low clock ratio) 1: 2-Stage Synchronizer (High clock ratio)	1'b0
20	R/W	HCLK_OE	HCLK Output Enable Control 0: Disable 1: Enable (Normal Operation)	1'b1
19	-	-	Reserved	
18:17	R/W	HCLK_CTL	Internal Host Clock Control 00: Turn off the internal host clock 01: Turn off the internal host clock immediately 10: Turn on the internal host clock immediately 11: Always turn on internal host clock	2'b11
16	R	HCLK_SW	SW Host Clock Control **Note:** S/W can program this bit to high/low, to toggle the internal host clock when HCLK_CTL[1:0] = 2'b00	1'b0
15:0	R/W	HCLK_CT_CNT	Host Clock Control Count Register This control register specifies the number of host clock to enable or stop the host clock signal	16'h0

Table 163: HIF_CMD_ARG (0x5003_0010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	HCLK_CMD_ARG	This register specifies the value of SD/eMMC command argument	32'h0

Table 164: HIF_CMD_IDX (0x5003_0014)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	CMDQ_TRIG	Trigger to transfer the value of Command Index and Argument registers into Command Index Queue and Command Argument Queue registers. The trigger (transfer) operation is only active when the value of this bit is high, and the status of command queue is not busy (QBUSY_ST)	1'b0
14	R/W	CMD_TCTL	Command Trigger Control 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result has been read	1'b0
13	R/W	STB_CTL	Command Start Bit and Transmission Bit Control 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by H/W circuit 1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register	1'b0
12:11	R/W	RSP_TYPE	Response Type Control 00: No Response 01: R3 Response 10: Short Response (Total: 48 bits) 11: Long Response (Total: 136 bits)	2'b00
10:9	R/W	DATA_TYPE	Data Type Control 0x: Command only (without data transfer) 10: Command with single/multiple read data 11: Command with single/multiple write data	2'b00
8	-	-	Reserved	
7	R/W	STR_NIT	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b0
6	R/W	TRM_BIT	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b1
5:0	R/W	HIF_CMD_IDX	This register specifies the value of the SD/eMMC command index	6'h0

Table 165: HIF_CMD_ARGQ (0x5003_0018)

Bit	Mode	Symbol	Description	Reset
31:0	R	HCLK_CMD_ARG	This register is a queue to receive the value of the SD/eMMC command argument register when the trigger (transfer) operation is active	32'h0

Table 166: HIF_CMD_IDXQ (0x5003_001C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R	QBUSY_ST	Busy status of the current command queue 0: Completed 1: Ongoing	1'b0
14	R	CMD_TCTLQ	Command Trigger Control Queue 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result has been read	1'b0
13:12	R	RSP_TYPEQ	Response Type Control Queue 0x: No Response 10: Short Response (Total: 48 bits) 11: Long Response (Total: 136 bits)	2'b00
11	R	STB_CTL	Command Start Bit and Transmission Bit Control Queue 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by H/W circuit 1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register	1'b0
10:8	R	DATA_TYPEQ	Data Type Control Queue 0xx: Command only (without data transfer) 100: Command with single read data 101: Command with multiple read data 110: Command with single write data 111: Command with multiple write data	3'b000
7	R	STR_NITQ	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b0
6	R	TRM_BITQ	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b1
5:0	R	HIF_CMD_IDXQ	This register specifies the value of the SD/eMMC command index	6'h0

Table 167: HIF_PAD_CTRL (0x5003_0020)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	
29:28	R/W	HCOE_DLY	Output Enable Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
27:26	R/W	HCO_DLY	Output Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
25:24	R/W	HCI_DLY	Input Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
23:22	R/W	HDATI_ST	Input Schmitt Trigger Level Control for Host Data signals	2'b00
21:20	R/W	HDAT_PUD	Host Data signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
19:16	R/W	HDATO_DS	Output Drive Strength Control for Host Data Signals	2'b00
15:14	R/W	HCMDI_ST	Input Schmitt Trigger Level Control for Host Data signals	2'b00
13:12	R/W	HDAT_PUD	Host Command signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
11:8	R/W	HCMDO_DS	Output Drive Strength Control for Host Command Signals	4'h0
7:6	-	-	Reserved	
5:4	R/W	HCLK_PUDC	Host Clock signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
3:0	R/W	HCLK_DS	Host Clock Control Count Register Output Drive Strength Control for Host Clock Signals	4'h0

Table 168: HIF_BLK_LG (0x5003_0024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	
27:16	R/W	HIF_BLK_LG	Block Length Register This register specifies the length (unit: byte) of each block for read/write data transfer	8'h0
15:6	-	-	Reserved	
5:4	R/W	HDOE_DLY	Output Enable Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
3:2	R/W	HDO_DLY	Output Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
1:0	R/W	HDI_DLY	Input Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00

Table 169: HIF_BLK_CNT (0x5003_0028)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	
23:0	R/W	HIF_BLK_CNT	Block Count Register	24'h0

Table 170: HIF_RSP_TMO_CNT (0x5003_0030)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7:0	R/W	RSP_TMO_CNT	This register specifies the number of host clock cycles for the response time-out interrupt. If the host cannot receive the response, it does not return to the host before the specified clock cycles	8'h40

Table 171: HIF_RD_TMO_CNT (0x5003_0034)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RD_TMO_CNT	Read Data Time-Out Count Register This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles	8'h0040_0000

Table 172: HIF_WB_TMO_CNT (0x5003_0038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WB_TMO_CNT	Read Data Time-Out Count Register This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles	32'h0A00_0000

Table 173: HIF_RSP_CIX_ST (0x5003_003C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7	R	RSP_STR_B	Status of the Start bit of the received response R2 Response: RSP[135] Other Responses: RSP[47]	1'b0
6	R	RSP_DIR_B	Status of the Direction (Transmission) bit of the received response R2 Response: RSP[134] Other Responses: RSP[46]	1'b0
5:0	R	RSP_CMD_IDX	Status of the Command Index of the received response R2 Response: RSP[133:128] Other Responses: RSP[45:40]	6'h0

Table 174: HIF_RSP_ARG_0 (0x5003_0040)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_0	Status of the received response argument-0 R2 Response: RSP[127:96] Other Responses: RSP[39:8]	32'h00

Table 175: HIF_RSP_ARG_1 (0x5003_0044)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_1	Status of the received response argument-1 R2 Response: RSP[95:64] Other Responses: Reserved	32'h00

Table 176: HIF_RSP_ARG_2 (0x5003_0048)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_2	Status of the received response argument-2 R2 Response: RSP[63:32] Other Responses: Reserved	32'h00

Table 177: HIF_RSP_ARG_3 (0x5003_004C)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_3	Status of the received response argument-3 R2 Response: RSP[31:0] Other Responses: Reserved	32'h00

Table 178: HIF_AHB_SA (0x5003_0050)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_SA	This register specifies the start address of AHB bus for data transfer	32'h00

Table 179: HIF_AHB_EA (0x5003_0054)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_EA	This register specifies the end address of AHB bus for data transfer	32'h00

Table 180: HIF_BUS_ST (0x5003_0060)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7	R/W	RSP_RET_ST	Receive the response from the device 0: Not receive 1: Receive	1'b0
6	R	CMD_BUSY	CMD/RSP Status Machine Busy Status 0: Not ongoing command/response (Idle) 1: Have ongoing command/response (Busy)	1'b0
5	R	DAT_BUSY	Data Status Machine Busy Status 0: Not ongoing data transfer (Idle) 1: Have ongoing data transfer (Busy)	1'b0
4	R	HCMD_ST	Status of Host Interface CMD signal	1'b0
3:0	R	RSP_CMD_IDX	Status of Host Interface Data signals	4'h0

Table 181: HIF_SM_ST (0x5003_0064)

Bit	Mode	Symbol	Description	Reset
31:16	R	HIF_DAT_CNT	Data Count Status	16'h0
15:13	-	-	Reserved	
12:8	R	HIF_DAT_SM	Data State Machine Status	5'h0
7:5	-	-	Reserved	
4:0	R	HIF_CMD_SM	CMD/RSP State Machine Status	5'h0

Table 182: HIF_XTR_CNT (0x5003_0068)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	
23:0	R	RSP_TMO_CNT	Transferred Data Block Count Status This register reports the number of the transferred data blocks. The value of this counter will be cleared after a new read/write command has been sent	24'h00

Table 183: HIF_ERR_CNT (0x5003_006C)

Bit	Mode	Symbol	Description	Reset
31:25	-	-	Reserved	
24	R/W	ERR_CNT_FG	Error Count Flag Read: 0: No data CRC error 1: Data CRC error (Read CRC error or Non-positive Write CRC status token) Write: Clear the error count flag for allowing to record the data error block count 0: No effect 1: Clear the error count flag for allowing to record the data error block count when the data CRC error was occurred	1'b0
23:0	R	HIF_ERR_CNT	ERR Data Block Count Status This register recorded the number of the error data blocks. When the first data error occurred (Read CRC error or received the non-Positive Write CRC Status Token) during the read/write data transfer, the value of the transferred data block count will be recorded into this register. S/W needs to write “1” into the CLE_ERR_CNT bit to clear the internal flag that it controls, to record the error block count or not when the data error was occurred	24'h00

10.5 SPI and I2C Register

DA16200 includes I2C master and slave functions. Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz) and High Speed (3.4 MHz) mode for both Master and Slave mode.

DA16200 also supports SPI master and Slave functions. To use DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from the GPIO special function by setting the registers in the GPIO.

The SPI slave interface is a half-duplexd connection for an external host to control the DA16200. The range of the SPI clock speed is based on the internal bus clock speed and can be calculated using:

spi clock = system clock/N

where N is an integer divider such as 1,2,3,4,5,6,...

There is a separate communication protocol for SPI slave. See section 9.3 SPI slave for more detailed information.

Table 184: SPI and I2C Registers Overview

Address	Register	Description
Common control for SPI and I2C Pin Status		
0x5008_023C	SPI_INTR_STATUS_REG	SPI Interrupt Status Register
0x5008_0240	SPI_CTRL_REG	SPI Control Register
0x5008_0244	I2C_CTRL_REG	I2C Control Register
0x5008_0248	SPI_LENGTH_REG	SPI Length Register
0x5008_024C	I2C_BUFFER_ADDR_REG	I2C Buffer Address Register
0x5008_0250	SPI_BASE_ADDR_REG	SPI Base Address Register
0x5008_0254	CMD_ADDR_REG	Command Address Register
0x5008_0258	RESP_ADDR1_REG	Response Address1 Register
0x5008_025C	RESP_ADDR2_REG	Response Address2 Register
0x5008_0260	AT_CMD_BASE_REG	AT Command Base Address Register
0x5008_0264	AT_CMD_REF_REG	AT Command Base Address Register
0x5008_0264	SPI_TIMER_REG	SPI Timer Register

Table 185: SPI_INTR_STATUS_REG (0x5008_023C)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	INTR	SPI slave interrupt status register bit[15]: Command interrupt status/clear bit[14]: AT Command interrupt status/clear bit[13]: Processing end interrupt status/clear	0x0
12:0	R/W	-	Reserved	0x000

Table 186: SPI_CTRL_REG (0x5008_0240)

Bit	Mode	Symbol	Description	Reset
15	R/W	CmdIntr	Command interrupt enable 1: Enable 0: Disable	1'b0
14	R/W	ATIntr	AT Command interrupt enable 1: Enable 0: Disable	1'b0
13	R/W	PEIntr	Processing end interrupt enable 1: Enable 0: Disable	1'b0
12	R/W	Prot	Protocol mode 1: 8-byte 0: 4-byte (default)	1'b0
11	R/W	SW_Rst	SPI block software reset 1: Normal 0: Reset state	1'b1
10	R/W		MISO Output mode selection 1: Normal 0: Half Pre output	1'b1
9	R/W	-	Reserved	1'b0
8	R/W	Endian	Endian mode for Data	1'b1
7:6	R/W	MODE	Define the SPI mode (CPOL, CPHA) 0: New data on falling, capture on rising, Clk low in idle state 1: New data on rising, capture on falling, Clk low in idle state 2: New data on rising, capture on falling, Clk high in idle state 3: New data on falling, capture on rising, Clk high in idle state	2'b00
5:4	R/W	ChipID	Valid when 8-byte protocol mode Effective when matching ChipID field is the same as command[1:0] on the SPI protocol function	2'b00
3:2	R/W	DBusW	Data bus width 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = Not used	2'b10
1:0	R/W	ABusW	Address bus width 00 = 8-bit 01 = 16-bit 10 = 24-bit 11 = 32-bit (default)	2'b11

Table 187: I2C_CTRL_REG (0x5008_0244)

Bit	Mode	Symbol	Description	Reset
7	R/W	SW_Rst	I2C block software reset 1: Normal 0: Reset state	1'b0
6	R/W	Endian	Endian mode for Data	1'b1
5:4	R/W	ChipID	Device ID for lower 2-bit	2'b00
3:2	R/W	DBusW	Data bus width 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = Not used	2'b10
1:0	R/W	ABusW	Address bus width 00 = 8-bit 01 = 16-bit 10 = 24-bit 11 = 32-bit (default)	2'b11

Table 188: SPI_LENGTH_REG (0x5008_0248)

Bit	Mode	Symbol	Description	Reset
23:0	R/W	Length	SPI reference length at read access	0x0100

Table 189: I2C_BUFFER_ADDR_REG (0x5008_024C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Length	I2C buffer address	0x0000

Table 190: SPI_BASE_ADDR_REG (0x5008_0250)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	BaseAddr	When SPI protocol 4-byte is set Upper 2-byte Address value is written in this field	0x0000

Table 191: CMD_ADDR_REG (0x5008_0254)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CmdAddr	Write/Read Request If accessed, internal interrupt should be generated	0x0000

Table 192: RESP_ADDR1_REG (0x5008_0258)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #1	0x0000

Table 193: RESP_ADDR2_REG (0x5008_025C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #2	0x0000

Table 194: AT_CMD_BASE_REG (0x5008_0260)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command base address Indicates the AT command reference register	0x0000

Table 195: AT_CMD_REF_REG (0x5008_0264)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command reference register Indicates the SRAM address that external AP will access	0x0000

Table 196: SPI_TIMER_REG (0x5008_0268)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Timer	Optional	0x1000

10.6 RTC Register

DA16200 provides RTC functions. Clock source for RTC can be selected with a register between 32 kHz OSC and 32 kHz XTAL. There is a 36-bits free-running counter in the RTC block making it a reference time. RTC block controls sleep and wake up operation of DA16200. And it also controls internal power on/off for each HW blocks.

Table 197: RTC Register Overview

Address	Registers	Description
0x5009_1000	wakeup_counter0	Wakeup counter [31:0]
0x5009_1004	wakeup_counter1	Wakeup counter [35:32]
0x5009_1008	gpio_wakeup_config	Wakeup by GPIO config register
0x5009_100C	gpio_wakeup_control	Wakeup by GPIO control register
0x5009_1010	rtc_control	RTC control register
0x5009_1014	xtal_control	32 kHz XTAL control register
0x5009_1018	retention_control	Retention memory power control register
0x5009_101C	dc_power_control	DCDC control register
0x5009_1020	ldo_control	Control LDOs
0x5009_1024		Reserved
0x5009_1028	wakeup_source	Wake up source
0x5009_102C		Reserved
0x5009_1030	AO indicator	Indicate retention memory contents
0x5009_1034		Reserved
0x5009_1038	counter0	Real time counter [31:0]
0x5009_103C	counter1	Real time counter [35:32]
0x5009_1040	ldo_status	LDO status register
0x5009_1044	ldo_pwr_control	uLDO control register
0x5009_1048		Reserved
0x5009_104C	bor_circuit	Brown and Black out control register
0x5009_1050		Reserved
0x5009_1054		Reserved
0x5009_1058		Reserved
0x5009_105C	watchdog_cnt	RTC watch dog counter

Table 198: wakeup_counter0 (0x5009_1000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W		Set to RTC timer value which is expected to wakeup	0x00000000

Table 199: wakeup_counter1 (0x5009_1004)

Bit	Mode	Symbol	Description	Reset
3:0	R/W		Set to RTC timer value which is expected to wakeup	0x0

Table 200: gpio_wakeup_config (0x500_91008)

Bit	Mode	Symbol	Description	Reset
25:16	R/W		Wake-up source selection. (Note 1) [16] 0: GPIOA4 1: GPIOC0 [17] 0: GPIOA5 1: GPIOC1 [18] 0: GPIOA6 1: GPIOC2 [19] 0: GPIOA7 1: GPIOC3 [20] 0: GPIOA8 1: GPIOC4 [21] 0: GPIOA9 1: GPIOC6 [22] 0: GPIOA10 1: GPIOC7 [23] 0: GPIOA11 1: GPIOC8 [24] 0: GPIOC5 1: GPIOA12 [25] 0: GPIOA13 1: GPIOA14	0x000
12:10	R/W	-	Edge selection of RTC_WAKE_UP2/3/4 (Note 2). [12] RTC_WKAE_UP4 [11] RTC_WAKE_UP3 [10] RTC_WAKE_UP2 0: Rising edge 1: Falling edge	0x0
9:0	R/W	-	Edge sel: selected signal by [25:16] 0: Rising edge 1: Falling edge	0x000

Note 1 GPIOA[11:0] and GPIOC[8:6] can be used in 6x6.

Note 2 RTC_WAKE_UP and RTC_WAKE_UP2 can be used in 6x6.

Table 201: gpio_wakeup_control (0x5009_100C)

Bit	Mode	Symbol	Description	Reset
28:26	R/W	-	Wakeup enable (Note 1). [28] RTC_WAKE_UP4 [27] RTC_WAKE_UP3 [26] RTC_WAKE_UP2 0: Wakeup disable 1: Wakeup enable	0x0
25:16	R/W	-	Wakeup enable of selected signal by gpio_wakeup_config[25:16] 0: Wakeup disable 1: Wakeup enable	0x000
13:10	R	-	Indicate wake up source [13] RTC_WAKE_UP4 [12] RTC_WAKE_UP3 [11] RTC_WAKE_UP2 [10] RTC_WAKE_UP 1: Indicates wake up from that port	0x0
9:0	R	-	Indicate GPIO wakeup source 9:0 1: Indicates wakeup from that port	0x000

Note 1 RTC_WAKE_UP and RTC_WAKE_UP2 can be used in 6x6.

Table 202: rtc_control (0x5009_1010)

Bit	Mode	Symbol	Description	Reset
6	R/W	-	Wakeup enable for RTC_WAKE_UP 0: Wakeup disable 1: Wakeup enable	1'b0
5	R/W	-	Brown out interrupt enable field 0: No interrupt will be enabled 1: When event, IRQ will be generated	1'b0
4	R/W	-	Black out interrupt enable field 0: No interrupt will be enabled 1: When event, IRQ will be generated	1'b0
3	R/W	-	RTC Watch-Dog Count 0: Count disable 1: Count enable	1'b0
2	R/W	-	RTC_WAKE_UP input polarity selection 0: Rising edge 1: Falling edge	1'b0
1	R/W	-	RTC_WAKE_UP interrupt enable (Normal mode) 0: No interrupt will be enabled 1: When an event occurs, IRQ will be generated	1'b0
0	R/W	-	Power down enable 0: No effect 1: Go to power down mode	1'b0

Table 203: xtal_control (0x5009_1014)

Bit	Mode	Symbol	Description	Reset
10	R/W	-	VBAT BIAS current control (0: max current, 1: min current)	1'b0
9:8	R/W	-	XTAL LDO current control (0: max current, 3: min current)	2'b00
7:5	R/W	-	40M XTAL LDO output voltage control	3'b100
4	R/W	-	EN_XR_BAT External resistor enable 0: Internal resistor used 1: External resistor used	1'b0
3:2	R/W	-	CLK_SEL1:0 Select clock source (default 32 kHz OSC) 0: 32 kHz OSC 1: 32 kHz Crystal 2: For test	2'b00
1	R/W	-	EN_XTAL_BAT 32 kHz Crystal Power on/off (default:1) (0: off, 1: on)	1'b1
0	R/W	-	PDB_OSC	1'b1

Bit	Mode	Symbol	Description	Reset
			32 kHz Oscillator Power on/off (default:1) (0: off, 1: on)	

Table 204: retention_control (0x5009_1018)

Bit	Mode	Symbol	Description	Reset
27:24	R/W	-	GPIO retention control bit [27] FDIO region [26] GPIOC [25] GPIOA [24] reserved 0: Disable 1: Enable	4'b0000
22:16	R/W	-	RET_RET[6:0] Retention memory Retention mode enable 0: Disable 1: Enable	7'b0000000
14:8	R/W	-	RET_SLR[6:0] Retention memory Sleep mode enable (when memory sleep, Memory's content will be lost) 0: Disable 1: Enable	7'b0000000
7:4	R/W	-	Power down information	4'b0000
2	R/W	-	PDB_ISO_shared_io (GPIOA0~3) 0: Isolation enable, cannot access to GPIOA0~3 1: Isolation disable, access to GPIOA0~3	1'b1
1	R/W	-	RTM_INFORM	1'b0
0	R/W	-	PDB_ISO default 0 1: Isolation disable, access to Retention Memory 0: Isolation enable, cannot access to Retention Memory	1'b0

Table 205: dc_power_control (0x5009_101C)

Bit	Mode	Symbol	Description	Reset
1	R/W	-	Auto Power On Enable 0: No effect 1: When set to “1”, go to sleep and wake up automatically, all register values will be reset value.	1'b0
0	R/W	-	DCDC1.2 power off 0: No effect 1: When set to “1”, DCDC1.2 Off	1'b0

Table 206: ldo_control (0x5009_1020)

Bit	Mode	Symbol	Description	Reset
9	R/W	-	PDB_IP1_LDO (IQADC/DAC power control) 0: IP1 LDO power off 1: IP1 LDO power on	1'b0
8	R/W	-	PDB_RF_LDO 0: RF LDO power off 1: RF LDO power on	1'b0
7	R/W	-	DIG_LDO_CNTL (to IP4 block) 0: DIG LDO power off 1: DIG LDO power on	1'b1
6	R/W	-	DCDC_CNTL_XTAL (to RF block) 0: DIG LDO power off 1: DIG LDO power on	1'b1
5	R/W	-	PDB_uLDO for retention memory power supply LDO control 0: LDO off 1: LDO on	1'b0
4	R/W	-	PDB_IP3_OTP: OTP power switch 0: OTP block power off 1: OTP block power on	1'b1
3	R/W	-	OTP_PWRPRDY: indicates OTP power stable 0: OTP block power is not ready 1: OTP block power is stable	1'b1
2	R/W	-	LDO_PLL1: for PLL power 0: PLL LDO off 1: PLL LDO on	1'b0
1		-	Reserved	
0	R/W	-	PDB_XTAL_NOISE_REDU: XTAL noise reduction circuit 0: No effect 1: Noise reduction circuit on	1'b0

Table 207: wakeup_source (0x5009_1028)

Bit	Mode	Symbol	Description	Reset
11:8	R	-	ADC Sensor Wakeup status: indicates ADC wakeup source pin [11]: Sensor Wakeup GPIOA3 [10]: Sensor Wakeup GPIOA2 [9]: Sensor Wakeup GPIOA1 [8]: Sensor Wakeup GPIOA0	4'h0
6	R/W	-	DWAKE source detect Read case: 1 indicates wakeup source from GPIOs Write case: 0: Wait for event	1'b0

Bit	Mode	Symbol	Description	Reset
			1: Source clear	
5	R/W	-	Pulse CNT detect Read case: 1 indicates wakeup source from pulse CNT function Write case: 0: Wait for event 1: Source clear	1'b0
4	R/W	-	Sensor (ADC) detect Read case: 1 indicates wakeup source from ADC sensor function Write case: 0: Wait for event 1: Source clear	1'b0
3	R/W	-	WatchDog detect Read case: 1 indicates wakeup source from RTC watch dog Write case: 0: Wait for event 1: Source clear	1'b0
2	R/W	-	POR indicator Read case: 1 indicates wakeup source from POR port Write case: 0: Wait for event 1: Source clear	1'b0
1	R/W	-	FRC compare detect Read case: 1 indicates wakeup from RTC count meet the wanted value Write case: 0: Wait for event 1: Source clear	1'b0
0	R/W	-	Ext Wakeup signal detect Read case: 1 indicates wakeup source from RTC_WAKE_UPx pins Write case: 0: Wait for event 1: Source clear	1'b0

Table 208: AO Indicator (0x5009_1030)

Bit	Mode	Symbol	Description	Reset
3	R/W	-	AO register restore enable (REM to AO) 0: No effect 1: Indicates some contents are in retention memory which should be restored when wake up	1'b0
[2:0]			Reserved	3'b000

Table 209: counter0 (0x5009_1038)

Bit	Mode	Symbol	Description	Reset
31:0	R	-	RTC free running counter read value [31:0]	0x00

Table 210: counter1 (0x5009_103C)

Bit	Mode	Symbol	Description	Reset
3:0	R	-	RTC free running counter read value [35:32]	0x00

Table 211: ldo_status (0x5009_1040)

Bit	Mode	Symbol	Description	Reset
13	R	-	IP1_LDO_RDY 1: IP1_LDO is ready	1'b0
12	R	-	DCDC_RDY 1: DCDC is ready	1'b0
11	R	-	F_LDO_RDY 1: Flash LDO is ready	1'b0
10	R	-	DIG_LDO_RDY 1: DIG LDO is ready	1'b0
9	R	-	RF_LDO_RDY 1: RF LDO is ready	1'b0
8	R	-	XTAL40M_RDY 1: XTAL 40 Mhz clock is ready	1'b0
7	R	-	Reserved	
6	R	-	Reserved	
5	R	-	Reserved	
4	R	-	Reserved	
3	R	-	XTAL_RDY 1: XTAL 32 kHz is ready	1'b0
2	R	-	Reserved	
1	R	-	Reserved	
0	R	-	Represent pin status of RTC_WAKE_UP	

Table 212: ldo_pwr_control (0x5009_1044)

Bit	Mode	Symbol	Description	Reset
29	R/W	-	DCDC_ST_BYP 0: Soft start bypass disable 1: Soft start bypass enable	1'b0
28:24	R/W	-	DCDC_ST_CTRL[4:0] DCDC soft start timing control delay time	5'b01011
21	R/W	-	IP2_MON_PATH_CTRL 0: LDO and low frequency path 1: RF clock path	1'b0

Bit	Mode	Symbol	Description	Reset
20:18	R/W	-	IP2_MON_CTRL For testing purpose	3'b0
17:16	R/W	-	RTC_XTAL32K_GM XTAL 32 kHz gain control	2'b11
15:14	R/W	-	RTC_OSC32K_ICTRL Osc32K sleep current control, 00: min ~ 11: max	2'h0
13:12	R/W	-	RTC_XTAL32K_ICTRL Xtal32K sleep current control, 00: min ~ 11: max	2'b01
11:10	R/W	-	RTC_uLDO_LICTRL uLDO sleep current control, 00: min~ 11: max	2'b01
9:8	R/W	-	RTC_uLDO_HICTRL uLDO speed up control 00: Low speed 11: High speed	2'b11
7:4	R/W	-	RTC_uLDO_VCTRL: uLDO output voltage control 4'b0001 (1.12V) ~ 4'b1111 (0.8V)	4'b0001
1	R/W	-	PDB_TEST_BUF: IP2 test buffer enable	1'b0
0	R/W	-	RTC clock inversion: for test purpose 0: Bypass 1: Inversion	1'b0

Table 213: bor_circuit (0x5009_104C)

Bit	Mode	Symbol	Description	Reset
14	R	-	BR status read 1: Brown Out event occurred	
13	R	-	BL status read 1: Black Out event occurred	
12	R/W	-	BR_HYS_CTRL 0: Hysteresis 100 mV (Default) 1: Hysteresis 150 mV	1'b0
11	R/W	-	BL_HYS_CTRL 0: Hysteresis 100 mV (Default) 1: Hysteresis 150 mV	1'b0
10	R/W	-	Reserved	1'b0
9	R/W	-	BR_OUT_EN (brown out) 0: Disable BR logic 1: Enable BR logic	1'b0
8	R/W	-	BL_OUT_EN (black out) 0: Disable BL logic 1: Enable BL logic	1'b0
7:4	R/W	-	BR_OUT_CTRL Voltage threshold for the Brownout Detector	4'b0111

Bit	Mode	Symbol	Description	Reset
3:0	R/W	-	BL_OUT_CTRL Voltage threshold for the Blackout Detector	4'b0101

Table 214: watchdog_cnt (0x5009_105C)

Bit	Mode	Symbol	Description	Reset
6:5	R	-	WatchDog Count read value	
4:0	R/W	-	Free Running Counter[35:14] bit selection	0x00

10.7 External Interrupt Control Register

External interrupt signal in GPIO Alternative function (see bit[4] in the Table 90) can be configured and set with this register.

Table 215: External Interrupt Control Register Overview

Address	Registers	Description
0x50001200	EXT_INTB_CTRL	External Interrupt Control [7:0]
0x50001204	EXT_INTB_SET	External Interrupt Set [0]

Table 216: EXT_INTB_CTRL (0x50001200)

Bit	Mode	Symbol	Description	Reset
7:2	R/W	-	Pulse duration. (unit: 256 CPU clocks.) Valid when edge mode.	6'b100000
1	R/W	-	Interrupt mode 0: Level mode 1: Edge mode	1'b0
0	R/W		Interrupt Polarity 0: Active low 1: Active high	1'b0

Table 217: EXT_INTB_SET (0x50001204)

Bit	Mode	Symbol	Description	Reset
0	R/W	-	External interrupt set register. When level mode, set '1' for trigger and '0' for clear. When edge mode, just set '1' and will be cleared automatically after pulse width.	1'b0

10.8 ADC Register

DA16200 provides an Aux ADC.

Table 218: ADC Registers Overview

Offset	Register	Description
0x4001_6000	AXADC12B_CTRL	AXADC 12B Control Register
0x4001_6008	ADC_EN_CH	ADC Channel Enable Register
0x4001_600C	XADC_THR_INTR_MASK	Interrupt enable register from threshold level
0x4001_6010	XADC_THR_INTR_CLR	Interrupt clear register from threshold level
0x4001_6014	XADC_INTR_CTRL_FIFO	Interrupt Mask set
0x4001_6018	XADC_INTR_STATUS	Interrupt Status set
0x4001_601C	ADC_DMA_EN	FIFO 3 ~ FIFO 0 DMA enable
0x4001_6020	FIFO0_DATA	FIFO0 DMA data for Channel 0
0x4001_6024	FIFO1_DATA	FIFO1 DMA data for Channel 1
0x4001_6028	FIFO2_DATA	FIFO2 DMA data for Channel 2

0x4001_602C	FIFO3_DATA	FIFO3 DMA data for Channel 3
0x4001_6030	AXADC_RM_SAMPLE	The number of removing initial samples
0x4001_6034	AXADC_STEP_SAMPLE	The number of sampling interval in Auto switching mode
0x4001_6038	ADC12B_INTR_THR_OVER	Over threshold value of interrupt
0x4001_6040	ADC12B_INTR_THR_UNDER	Under threshold value of interrupt
0x4001_6048	ADC12B_INTR_THR_DIFF	Difference threshold value of interrupt
0x4001_6050	FIFO0_DATA_CURR	Current FIFO0 Aux adc12b data
0x4001_6054	FIFO1_DATA_CURR	Current FIFO1 Aux adc12b data
0x4001_6058	FIFO2_DATA_CURR	Current FIFO2 Aux adc12b data
0x4001_605C	FIFO3_DATA_CURR	Current FIFO3 Aux adc12b data
0x4001_6060	TIME_STAMP_CTRL	Time Stamp base count level
0x4001_6064~ 6C		Reserved

Table 219: AXADC12B_CTRL (0x4001_6000)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	0x0
8	R/W	DF	Aux adc12b data format 0: 2's complement 1: Offset binary	0x0
7:5	R/W	TRIM	Trim VREF Voltage for Aux adc12b control	0x0
3:2	R/W	CS	Channel select input for Aux adc12b control signal 0: VIN1 1: VIN2 2,3: Reserved	0x0
1	R/W	POWDN	Power down for Aux adc12b control signal 0: No power down 1: Power down	0x1
0	R/W	RSTB	Reset for Aux adc12b control signal 0: No reset 1: Reset	0x1

Table 220: ADC_EN_CH (0x4001_6008)

Bit	Mode	Symbol	Description	Reset
8:4	R/W	CH_EN	AUX ADC switching mode When set This Reg, must set to "0x000"->"0x1xx" [8] : Switching auto enable [7] : 12-bit 4th channel enable [6] : 12-bit 3rd channel enable [5] : 12-bit 2nd channel enable [4] : 12-bit 1st channel enable	0x01
3:0	-	-	Reserved	0x1

Table 221: XADC_THR_INTR_MASK (0x4001_600C)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	INT_LVL	Interrupt when exceeds a threshold level	0x00

Bit	Mode	Symbol	Description	Reset
			[11] : Threshold Difference interrupt mask of FIFO3 [10] : Threshold Difference interrupt mask of FIFO2 [9] : Threshold Difference interrupt mask of FIFO1 [8] : Threshold Difference interrupt mask of FIFO0 [7] : Under Threshold interrupt mask of FIFO3 [6] : Under Threshold interrupt mask of FIFO2 [5] : Under Threshold interrupt mask of FIFO1 [4] : Under Threshold interrupt mask of FIFO0 [3] : Over Threshold interrupt mask of FIFO3 [2] : Over Threshold interrupt mask of FIFO2 [1] : Over Threshold interrupt mask of FIFO1 [0] : Over Threshold interrupt mask of FIFO0	

Table 222: XADC_THR_INTR_CLR (0x4001_6010)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	INT_CLR	Interrupt when exceeds a threshold level [11] : Threshold Difference interrupt clear of FIFO3 [10] : Threshold Difference interrupt clear of FIFO2 [9] : Threshold Difference interrupt clear of FIFO1 [8] : Threshold Difference interrupt clear of FIFO0 [7] : Under Level interrupt clear of FIFO3 [6] : Under Level interrupt clear of FIFO2 [5] : Under Level interrupt clear of FIFO1 [4] : Under Level interrupt clear of FIFO0 [3] : Over Level interrupt clear of FIFO3 [2] : Over Level interrupt clear of FIFO2 [1] : Over Level interrupt clear of FIFO1 [0] : Over Level interrupt clear of FIFO0	0x00

Table 223: XADC_INTR_CTRL_FIFO (0x4001_6014)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	INT_MASK	Interrupt Mask set bit[7] : Interrupt mask for full level of FIFO 3 bit[6] : Interrupt mask for full level of FIFO 2 bit[5] : Interrupt mask for full level of FIFO 1 bit[4] : Interrupt mask for full level of FIFO 0 bit[3] : Interrupt mask for half level of FIFO 3 bit[2] : Interrupt mask for half level of FIFO 2 bit[1] : Interrupt mask for half level of FIFO 1 bit[0] : Interrupt mask for half level of FIFO 0	0x00

Table 224: XADC_INTR_STATUS (0x4001_6018)

Bit	Mode	Symbol	Description	Reset
19:0	RO	INT_STS	Interrupt Status set bit[19] : Interrupt status for Threshold Difference of FIFO 3 bit[18] : Interrupt status for Threshold Difference of FIFO 2 bit[17] : Interrupt status for Threshold Difference of FIFO 1 bit[16] : Interrupt status for Threshold Difference of FIFO 0 bit[15] : Interrupt status for Threshold Under level of FIFO 3 bit[14] : Interrupt status for Threshold Under level of FIFO 2 bit[13] : Interrupt status for Threshold Under level of FIFO 1 bit[12] : Interrupt status for Threshold Under level of FIFO 0 bit[11] : Interrupt status for Threshold Over level of FIFO 3 bit[10] : Interrupt status for Threshold Over level of FIFO 2	0x00

Bit	Mode	Symbol	Description	Reset
			bit[9] : Interrupt status for Threshold Over level of FIFO 1 bit[8] : Interrupt status for Threshold Over level of FIFO 0 bit[7] : Interrupt status for full level of FIFO 3 bit[6] : Interrupt status for full level of FIFO 2 bit[5] : Interrupt status for full level of FIFO 1 bit[4] : Interrupt status for full level of FIFO 0 bit[3] : Interrupt status for half level of FIFO 3 bit[2] : Interrupt status for half level of FIFO 2 bit[1] : Interrupt status for half level of FIFO 1 bit[0] : Interrupt status for half level of FIFO 0	

Table 225: ADC_DMA_EN (0x4001_601C)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	DMA_EN	FIFO 3 ~ FIFO 0 DMA enable [3] : FIFO 3 0: disable, 1: enable [2] : FIFO 2 0: disable, 1: enable [1] : FIFO 1 0: disable, 1: enable [0] : FIFO 0 0: disable, 1: enable	0x0

Table 226: FIFO0_DATA (0x4001_6020)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO0 DMA data for Aux adc12b channel 0 sampled data Interrupt indicate 4 consecutive sampled data [3:0] bits are filled with zero.	0x00

Table 227: FIFO1_DATA (0x4001_6024)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO1 DMA data for Aux adc12b channel 1 sampled data Interrupt indicate 4 consecutive sampled data [3:0] bits are filled with zero.	0x00

Table 228: FIFO2_DATA (0x4001_6028)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO2 DMA data for Aux adc12b channel 2 sampled data Interrupt indicate 4 consecutive sampled data [3:0] bits are filled with zero.	0x00

Table 229: FIFO3_DATA (0x4001_602C)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO3 DMA data for Aux adc12b channel 3 sampled data Interrupt indicate 4 consecutive sampled data [3:0] bits are filled with zero.	0x00

Table 230: AXADC_RM_SAMPLE (0x4001_6030)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	-	The number of removing initial samples of ASIC aux adc12b	0x10
7:0	-	-	Reserved	0x00

Table 231: FXADC_STEP_SAMPLE (0x4001_6034)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	-	The number of sampling interval of aux adc12B in Auto switching mode 0, 1 = Internal none 2~15 = N-1 interval sampling	0x2
3:0	-	-	Reserved	0x0

Table 232: ADC12B_INTR_THR_OVER (0x4001_6038)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Over threshold value of interrupt	0x00
0	R/W	-	Over threshold enable 0: Disable 1: Enable	0x1

Table 233: ADC12B_INTR_THR_UNDER (0x4001_6040)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Over threshold value of interrupt	0x00
0	R/W	-	Under threshold enable 0: Disable 1: Enable	0x1

Table 234: ADC12B_INTR_THR_DIFF (0x4001_6048)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Difference threshold value of interrupt	0x00
0	R/W	-	Difference threshold enable 0: Disable 1: Enable	0x1

Table 235: FIFO0_DATA_CURR (0x4001_6050)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO0 data of Aux adc12b	0x00

Table 236: FIFO1_DATA_CURR (0x4001_6054)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO1 data of Aux adc12b	0x00

Table 237: FIFO2_DATA_CURR (0x4001_6058)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO2 data of Aux adc12b	0x00

Table 238: FIFO3_DATA_CURR (0x4001_605C)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO3 data of Aux adc12b	0x00

Table 239: TIME_STAMP_CTRL (0x4001_6060)

Bit	Mode	Symbol	Description	Reset
11:8	R/W	-	Time Stamp base count level 12-bit ADC (default = 'd5)	0x5
7:0	-	-	Reserved	0x0

10.9 CRC Register

DA16200 provides a CRC 32 (Cyclic Redundancy Check).

Table 240: CRC32 Registers Overview

Offset	Register	Description
0x5004_0200	CRC_REQ_CTRL_REG	Stop Request of CRC Calculation, active high with auto clear function
0x5004_0204	CRC_OP_EN_REG	Operation Enable of CRC Calculation
0x5004_0208	CRC_CONFIG_REG	Configuration of CRC Calculation Input data
0x5004_020C	CRC_SEED_VAL_REG	CRC seed value
0x5004_0210	CRC_ADDR_MIN_REG	Minimum address to check the bus address range
0x5004_0214	CRC_ADDR_MAX_REG	Maximum address to check the bus address range
0x5004_0218	CRC_PSEUDO_VAL_REG	CRC pseudo value to accumulate manually
0x5004_0220	CRC_CAL_VAL_REG	CRC calculation value
0x5004_0224	CRC_STA_REG	Status of CRC Calculation
0x5004_0228	CRC_CAL_VAL_REV_REG	CRC calculation reversed value

Table 241: CRC_REQ_CTRL_REG (0x5004_0200)

Bit	Mode	Symbol	Description	Reset
2	WO	CRC_REQ_STOP	Stop Request of CRC Calculation, active high with auto clear function	0x0
1	WO	CRC_REQ_START	Start Request of CRC Calculation, active high with auto clear function	0x0
0	WO	CRC_REQ_CLR	Clear Request of CRC Calculation, active high with auto clear function	0x0

Table 242: CRC_OP_EN_REG (0x5004_0204)

Bit	Mode	Symbol	Description	Reset
0	R/W	CRC_OP_EN	Operation Enable of CRC Calculation	0x1

Table 243: CRC_CONFIG_REG (0x5004_0208)

Bit	Mode	Symbol	Description	Reset
27:26	R/W	CRC_OP_TYPE	Operation Type of CRC Calculation 0: CRC-32 1: CRC-16 CCITT 2: CRC-16 IBM	0x0
25	R/W	CRC_CHK_MST	Master Checking Enable of CRC Calculation for **slave path selection**	0x1

Bit	Mode	Symbol	Description	Reset
24	R/W	CRC_CHK_ADDR	Address Checking Enable of CRC Calculation	0x1
20:16	R/W	CRC_MST_TYPE	Master Type of CRC Calculation for slave path selection in Master Checking Enable 0x00 : Slave 0 (unused) 0x05 : Slave 5 (unused) 0x14 : Master 4 (uDMA or kDMA) 0x16 : Master 6 (SSI) 0x17 : Master 7 (fDMA-M0) 0x18 : Master 8 (fDMA-M1) 0x19 : Master 9 (CC-312) 0x1A : Master A (Flash Controller)	0x16
13	R/W	CRC_SWAP_EN	Input Data Swap Enable 0: Normal 1: Byte Swap	0x0
12	R/W	CRC_ENDIAN_TYPE	Input Endian Type 0: Big Endian (if 8bit access : 0->1->2->3->4->5->6->7) 1: Little Endian (if 8bit access : 7->6->5->4->3->2->1->0)	0x0
11	R/W	CRC_DAT_TYPE	Data Type of CRC Calculation 0: Normal Data 1: Header Data (Header bytes are all zero during CRC Calculation)	0x0
10:9	R/W	CRC_PAR_TYPE	Parallel Type of CRC Calculation 00 : 8 bits 01 : 16 bits 10 : 32 bits	0x2
8	R/W	CRC_ACC_TYPE	Access Type of CRC Calculation 0: Read access 1: Write access	0x1
4:0	R/W	CRC_PATH_SEL	Path Selection of CRC Calculation 0x00 : Slave 0 0x05 : Slave 5 0x14 : Master 4 (uDMA or kDMA) 0x16 : Master 6 (SSI) 0x17 : Master 7 (fDMA-M0) 0x18 : Master 8 (fDMA-M1) 0x19 : Master 9 (CC-312) 0x1A : Master A (Flash Controller)	0x17

Table 244: CRC_SEED_VAL_REG (0x5004_020C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_SEED_VAL	CRC seed value	0xFFFF_FFFF

Table 245: CRC_ADDR_MIN_REG (0x5004_0210)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_ADDR_MIN	Minimum address to check the bus address range	0x0

Table 246: CRC_ADDR_MAX_REG (0x5004_0214)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_ADDR_MAX	Maximum address to check the bus address range	0xFFFF_FFFF

Table 247: CRC_PSEUDO_VAL_REG (0x5004_0218)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_PSEUDO_VAL	CRC pseudo value to accumulate manually	0x0

Table 248: CRC_CAL_VAL_REG (0x5004_0220)

Bit	Mode	Symbol	Description	Reset
31:0	RO	CRC_CAL_VAL	CRC calculation value	0x0

Table 249: CRC_STA_REG (0x5004_0224)

Bit	Mode	Symbol	Description	Reset
25:24	RO	CRC_CAL_STA	Status of CRC Calculation 0: Idle 1: Busy 2: Stop 3: Error	0x0
19:0	RO	CRC_CAL_NUM	Number of CRC calculation bytes (Max. 1M Bytes)	0x0

Table 250: CRC_CAL_VAL_REV_REG (0x5004_0228)

Bit	Mode	Symbol	Description	Reset
31:0	RO	CRC_CAL_VAL_REV	CRC calculation reversed value	0x0

10.10 PWM Register

Table 251: PWM Registers Overview

Offset	Register	Description
0x4000_A000	PWM_EN0	PWM #0 signal enable
0x4000_A004	PWM_EN1	PWM #1 signal enable
0x4000_A008	PWM_EN2	PWM #2 signal enable
0x4000_A00C	PWM_EN3	PWM #3 signal enable
0x4000_A010	PWM_MAXCY0	PWM #0 CNT0's max value
0x4000_A014	PWM_MAXCY1	PWM #1 CNT1's max value
0x4000_A018	PWM_MAXCY2	PWM #2 CNT2's max value
0x4000_A01C	PWM_MAXCY3	PWM #3 CNT3's max value
0x4000_A020	PWM_HDUTY0	PWM #0 high signal's threshold value
0x4000_A024	PWM_HDUTY1	PWM #1 high signal's threshold value
0x4000_A028	PWM_HDUTY2	PWM #2 high signal's threshold value

0x4000_A02C	PWM_HDUTY3	PWM #3 high signal's threshold value
0x4000_A030	PWM_MC_OFFS0	PWM #0 setting offset
0x4000_A034	PWM_MC_OFFS1	PWM #1 setting offset
0x4000_A038	PWM_MC_OFFS2	PWM #2 setting offset
0x4000_A03C	PWM_MC_OFFS3	PWM #3 setting offset
0x4000_A040	MC_MODE	0: (HDUTYx >= CNTx) ? 1'b1 : 1'b0; 1: (HDUTYx >= CNTx - MC_OFFSx) ? 1'b1 : 1'b0;

Table 252: PWM_EN0 (0x4000_A000)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN0	PWM #0 signal enable	0x00

Table 253: PWM_EN1 (0x4000_A004)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN1	PWM #1 signal enable	0x00

Table 254: PWM_EN2 (0x4000_A008)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN2	PWM #2 signal enable	0x00

Table 255: PWM_EN3 (0x4000_A00C)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN3	PWM #3 signal enable	0x00

Table 256: PWM_MAXCY0 (0x4000_A010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY0	PWM #0 CNT0's max value	0x00

Table 257: PWM_MAXCY1 (0x4000_A014)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY1	PWM #1 CNT1's max value	0x00

Table 258: PWM_MAXCY2 (0x4000_A018)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY2	PWM #2 CNT2's max value	0x00

Table 259: PWM_MAXCY3 (0x4000_A01C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY3	PWM #3 CNT3's max value	0x00

Table 260: PWM_HDUTY0 (0x4000_A020)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY0	PWM #0 high signal's threshold value	0x00

Table 261: PWM_HDUTY1 (0x4000_A024)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY1	PWM #1 high signal's threshold value	0x00

Table 262: PWM_HDUTY2 (0x4000_A028)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY2	PWM #2 high signal's threshold value	0x00

Table 263: PWM_HDUTY3 (0x4000_A02C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY3	PWM #3 high signal's threshold value	0x00

Table 264: PWM_MC_OFFS0 (0x4000_A030)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS0	PWM #0 setting offset	0x00

Table 265: PWM_MC_OFFS1 (0x4000_A034)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS1	PWM #1 setting offset	0x00

Table 266: PWM_MC_OFFS2 (0x4000_A038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS2	PWM #2 setting offset	0x00

Table 267: PWM_MC_OFFS3 (0x4000_A03C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS3	PWM #3 setting offset	0x00

Table 268: MC_MODE (0x4000_A040)

Bit	Mode	Symbol	Description	Reset
0	R/W	MC_MODE	0: (HDUTYx >= CNTx) ? 1'b1 : 1'b0; 1: (HDUTYx >= CNTx - MC_OFFSx) ? 1'b1 : 1'b0;	0x00

10.11 kDMA Register

The base address of kDMA is 4000_EXXX.

Table 269: kDMA Registers Overview

Offset	Register	Description
0x000	dma_enable	Enable DMA (Write 1: Enable DMA, Write 0: Disable DMA)
0x004	dma_reset	Software reset (Write 1: reset DMA, and automatically return to 0)

0x008	cfg_descriptor_addr	Base address of first task descriptor memory area
0x00C	cfg_channel_enable	Enable a DMA channel (1: Enable channel, 0: Disable channel)
0x010	cfg_irq_done_type	dma_done interrupt type (0: dma_done interrupt occurs when DMA chain is done 1: dma_done interrupt occurs when DMA task is done 2: dma_done interrupt occurs when REQ_MODE is 0 and arbitration period is done 3: Reserved)
0x014	sw_request	Software DMA request (Write 1: send request signal, and automatically return to 0)
0x018	irq_done_chs	Indicator of which channel invokes dma_done
0x01C	irq_done_clr	Clear irq_done_chs (Write 1: clear irq_done_chs, and automatically return to 0)
0x020	irq_err_chs	Indicator of which channel invokes dma_err
0x024	irq_err_clr	Clear irq_err_chs (Write 1: clear irq_done_chs, and automatically return to 0)
0x028	status_dma	Current status of DMA (Pending channel bitmap: Pending channel's bitmap Current active channel: Current operating DMA channel number Current state on FSM: Current state of FSM)
0x02C	status_desc_addr	Address of current task descriptor
0x030	status_counter	Counters of current DMA task (arb_last flag: The flag to check whether the operating arbitration period is the last one of current task arb_done counter: The number of operated arbitration period in current task tf_last flag: The flag to check whether the operating transfer is the last one of current arbitration period tf_done counter: The number of operated transfers in current arbitration period)
0x034	status_descriptor	Current task descriptor
0x038	status_desc_addr_pre	Address of previous task descriptor
0x03C	ahb_hprot_3_to_0	HPROT signal of AHB bus [3] : Modifiable (1: Cacheable, 0: Non-cacheable) [2] : Bufferable (1: Bufferable, 0: Non-bufferable) [1] : Privileged (1: Privileged, 0: User access) [0] : Data/Opcode (1: Data access, 0: Opcode fetch)
0x040	ahb_hprot_7_to_4	
0x044	ahb_hprot_11_to_8	
0x048	ahb_hprot_15_to_12	

Table 270: DMA_ENABLE (0x000)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	
0	R/W	dma_enable	Enable DMA 0: Disable DMA 1: Enable DMA	1'b0

Table 271: DMA_RESET (0x004)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	
0	WO	dma_reset	Software reset (Write 1: reset DMA, and automatically return to 0)	1'b0

Table 272: CFG_DESCRIPTOR_ADDR (0x008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	cfg_descriptor_addr	Base address of first task descriptor memory area	32'd0

Table 273: CFG_CHANNEL_ENABLE (0x00C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	cfg_channel_enable	[15:0] channel number	16'd0

Table 274: CFG_IRQ_DONE_TYPE (0x010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	cfg_irq_done_type	[31:30] channel 15 done type [29:28] channel 14 done type ... [1:0] channel 0 done type	32'd0

Table 275: SW_REQUEST (0x014)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	WO	sw_request	[15:0] channel number	16'd0

Table 276: IRQ_DONE_CHS (0x018)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	RO	Irq_done_chs	[15:0] channel number	16'd0

Table 277: IRQ_DONE_CLR (0x01C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	WO	Irq_done_clr	[15:0] channel number	16'd0

Table 278: IRQ_ERR_CHS (0x020)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	RO	Irq_err_chs	[15:0] channel number	16'd0

Table 279: IRQ_ERR_CLR (0x024)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	WO	Irq_err_clr	[15:0] channel number	16'd0

Table 280: STATUS_DMA (0x028)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	
23:20	RO	state_on_fsm	Current state on FSM	4'd0
19:16	RO	act_channel	Current active channel	4’d0
15:0	RO	pending_ch	Pending channel number	16’d0

Table 281: STATUS_DESC_ADDR (0x02C)

Bit	Mode	Symbol	Description	Reset
31:0	RO	status_desc_addr	Address of current task descriptor	32'd0

Table 282: STATUS_COUNTER (0x030)

Bit	Mode	Symbol	Description	Reset
31	RO	arb_last_flag	The flag to check whether the operating arbitration period is the last one of current task	1’b0
30:16	RO	arb_done_counter	The number of operated arbitration period in current task	15'd0
15	RO	tf_last_flag	The flag to check whether the operating transfer is the last one of current arbitration period	1’b0
14:0	RO	tf_done_counter	The number of operated transfers in current arbitration period	15’d0

Table 283: STATUS_DESCRIPTOR (0x034)

Bit	Mode	Symbol	Description	Reset
31:0	RO	dma_task_descriptor	Current task descriptor	32'd0

Table 284: STATUS_DESC_ADDR_PRE (0x038)

Bit	Mode	Symbol	Description	Reset
31:0	RO	address	Address of previous task descriptor	32'd0

Table 285: AHB_HPROT_3_TO_0 (0x03C)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch3_src_hprot	HPROT signal of AHB bus [3] : Modifiable (1: Cacheable, 0: Non-cacheable) [2] : Bufferable (1: Bufferable, 0: Non-bufferable) [1] : Privileged (1: Privileged, 0: User access)	4’d1
27:24	R/W	ch3_dst_hprot		4’d1
23:20	R/W	ch2_src_hprot		4’d1
19:16	R/W	ch2_dst_hprot		4’d1
15:12	R/W	ch1_src_hprot		4’d1
11:8	R/W	ch1_dst_hprot		4’d1

Bit	Mode	Symbol	Description	Reset
7:4	R/W	ch0_src_hprot	[0] : Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
3:0	R/W	ch0_dst_hprot		4'd1

Table 286: AHB_HPROT_7_TO_4 (0x040)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch7_src_hprot	HPROT signal of AHB bus [3] : Modifiable (1: Cacheable, 0: Non-cacheable) [2] : Bufferable (1: Bufferable, 0: Non-bufferable) [1] : Privileged (1: Privileged, 0: User access) [0] : Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch7_dst_hprot		4'd1
23:20	R/W	ch6_src_hprot		4'd1
19:16	R/W	ch6_dst_hprot		4'd1
15:12	R/W	ch5_src_hprot		4'd1
11:8	R/W	ch5_dst_hprot		4'd1
7:4	R/W	ch4_src_hprot		4'd1
3:0	R/W	ch4_dst_hprot		4'd1

Table 287: AHB_HPROT_11_TO_8 (0x044)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch11_src_hprot	HPROT signal of AHB bus [3] : Modifiable (1: Cacheable, 0: Non-cacheable) [2] : Bufferable (1: Bufferable, 0: Non-bufferable) [1] : Privileged (1: Privileged, 0: User access) [0] : Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch11_dst_hprot		4'd1
23:20	R/W	ch10_src_hprot		4'd1
19:16	R/W	ch10_dst_hprot		4'd1
15:12	R/W	ch9_src_hprot		4'd1
11:8	R/W	ch9_dst_hprot		4'd1
7:4	R/W	ch8_src_hprot		4'd1
3:0	R/W	ch8_dst_hprot		4'd1

Table 288: AHB_HPROT_15_TO_12 (0x048)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch15_src_hprot	HPROT signal of AHB bus [3] : Modifiable (1: Cacheable, 0: Non-cacheable) [2] : Bufferable (1: Bufferable, 0: Non-bufferable) [1] : Privileged (1: Privileged, 0: User access) [0] : Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch15_dst_hprot		4'd1
23:20	R/W	ch14_src_hprot		4'd1
19:16	R/W	ch14_dst_hprot		4'd1
15:12	R/W	ch13_src_hprot		4'd1
11:8	R/W	ch13_dst_hprot		4'd1
7:4	R/W	ch12_src_hprot		4'd1
3:0	R/W	ch12_dst_hprot		4'd1

10.12 SYS_CLOCK Register

The base address of SYS_CLOCK is 5000_3XXX.

Table 289: SYS_CLOCK Registers Overview

Offset	Register	Description
0x000	PLL_CLK_DIV_0_CPU	#0 Divider parameter to generate CPU Clock from PLL output 480MHz (for CPU & Bus Clock) 00 : reserved 01 : 240.000 MHz (=480/2) 02 : 160.000 MHz (=480/3) 03 : 120.000 MHz (=480/4) 04 : 96.000 MHz (=480/5) 05 : 80.000 MHz (=480/6) 06 : 68.571 MHz (=480/7) 07 : 60.000 MHz (=480/8) 08 : 53.333 MHz (=480/9) 09 : 48.000 MHz (=480/10) 0A : 43.636 MHz (=480/11) 0B : 40.000 MHz (=480/12) 0C : 36.923 MHz (=480/13) 0D : 34.286 MHz (=480/14) 0E : 32.000 MHz (=480/15) 0F : 30.000 MHz (=480/16) 10 : 28.235 MHz (=480/17) 11 : 26.667 MHz (=480/18) 12 : 25.263 MHz (=480/19) 13 : 24.000 MHz (=480/20) 14 : 22.857 MHz (=480/21) 15 : 21.818 MHz (=480/22) 16 : 20.870 MHz (=480/23) 17 : 20.000 MHz (=480/24) 18 : 19.200 MHz (=480/25) 19 : 18.462 MHz (=480/26) 1A : 17.778 MHz (=480/27) 1B : 17.143 MHz (=480/28) 1C : 16.552 MHz (=480/29) 1D : 16.000 MHz (=480/30) 1E : 15.484 MHz (=480/31) 1F : 15.000 MHz (=480/32)
0x001	PLL_CLK_DIV_1_XFC	#1 Divider parameter to generate XFC Core Clock from PLL output 480MHz (for XFC Core Clock) XFC Core Clock Frequency must be n multiplication of CPU Clock Freq. (8>=n>=1)
0x002	PLL_CLK_DIV_2_UART	#2 Divider parameter to generate UART Core Clock from PLL output 480MHz (for UART Core Clock 80MHz)
0x003	PLL_CLK_DIV_3_OTP	#3 Divider parameter to generate OTP Core Clock from PLL output 480MHz (for OTP Core Clock 20MHz)
0x004	PLL_CLK_DIV_4_PHY	#4 Divider parameter to generate PHY Top Clock from PLL output 480MHz (for PHY Top Clock 480MHz)
0x005	PLL_CLK_DIV_5_I2S	#5 Divider parameter to generate I2S Master Clock from PLL output 480MHz (for I2S Master Clock) = 480/(PLL_CLK_DIV_5_I2S+1) MHz maximum 240 MHz ~ minimum 15.0 MHz
0X006	PLL_CLK_DIV_6_AUXA	#6 Divider parameter to generate AuxADC Clock from PLL output 480MHz (for AuxADC Clock) = 480/(PLL_CLK_DIV_6_AUXA+1) MHz maximum 240MHz ~ minimum 15.0 MHz
0x007	PLL_CLK_DIV_7_CC312	#2 Divider parameter to generate CC-312 Core Clock from PLL output 480MHz CC-312 Core Clock Frequency must be n multiplication of CPU Clock Freq. (8>=n>=1)
0x010	PLL_CLK_EN_0_CPU	PLL Counter Enable of #0 Divider

0x011	PLL_CLK_EN_1_XFC	PLL Counter Enable of #1 Divider
0x012	PLL_CLK_EN_2_UART	PLL Counter Enable of #2 Divider
0x013	PLL_CLK_EN_3_OTP	PLL Counter Enable of #3 Divider
0x014	PLL_CLK_EN_4_PHY	PLL Counter Enable of #4 Divider
0x015	PLL_CLK_EN_5_I2S	PLL Counter Enable of #5 Divider
0x016	PLL_CLK_EN_6_AUXA	PLL Counter Enable of #6 Divider
0x017	PLL_CLK_EN_7_CC312	PLL Counter Enable of #7 Divider
0x030	SRC_CLK_SEL_0_CPU	Selection signal of clock source #0 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_0)
0x031	SRC_CLK_SEL_1_XFC	Selection signal of clock source #1 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_1)
0x032	SRC_CLK_SEL_2_UART	Selection signal of clock source #2 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_2)
0x033	SRC_CLK_SEL_3_OTP	Selection signal of clock source #3 in the Clock Generator 0: Xtal/2 (20MHz) 1: PLL path (PLL_CLK_DIV_3)
0x035	SRC_CLK_SEL_5_I2S	Selection signal of clock source #5 in the Clock Generator 0: External Clock from GPIO PADs 1: PLL path (PLL_CLK_DIV_5)
0x036	SRC_CLK_SEL_6_AUXA	Selection signal of clock source #6 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_6)
0x037	SRC_CLK_SEL_7_CC312	Selection signal of clock source #7 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_7)
0x070	SRC_CLK_STA_0	Status of current clock source #0 in the Clock Generator 0: Xtal 1: Xtal to PLL 2: PLL 3: PLL to Xtal
0x074	IRQ_CLK_STA_0	Status of current interrupt in the Clock Generator 0: Xtal 1: Xtal to PLL 2: PLL 3: PLL to Xtal
0x085	CLK_DIV_I2S	Last divider parameter to generate I2S Core Clock (MCLK) 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)
0x090	CLK_EN_CPU	Clock enable of CPU Clock
0x091	CLK_EN_XFC	Clock enable of XFC Core Clock
0x092	CLK_EN_UART	Clock enable of UART Core Clock
0x093	CLK_EN_OTP	Clock enable of OTP Core Clock
0x095	CLK_EN_I2S	Clock enable of I2S Core Clock
0x096	CLK_EN_AUXA	Clock enable of AuxADC Core Clock
0x097	CLK_EN_CC312	Clock enable of CC-312 Core Clock

0x0A0	CLK_DIV_PHYBUS	Divider parameter to generate PHY Bus Clock from CPU Clock
0x0A1	CLK_DIV_EMMC	Divider parameter to generate SDeMMC Controller's Core Clock from CPU Clock 0 : 1/(2^0) 1 : 1/(2^1) 2 : 1/(2^2) n : 1/(2^n)
0x0A4	CLK_DIV_AUXA	Last divider parameter to generate AuxADC input clock from AuxADC reference PLL clock. 0 : 1/1 1 : 1/2 2 : 1/3 n : 1/(n+1)
0x0B0	CLK_EN_PHYBUS	Clock enable of PHY Bus
0x0B1	CLK_EN_SDeMMC	Clock enable of SDeMMC
0x0F0	DIFF_CPU_XFC	Ratio difference between CPU Clock and Flash Controller's Core Clock 00_0000 CPU:XFC=1:2^0 00_0001 CPU:XFC=1:2^1 00_0010 CPU:XFC=1:2^2 ….. 00_1011 CPU:XFC=1:2^7 10_0001 CPU:XFC=1:2^-1 10_0010 CPU:XFC=1:2^-2 ….. 10_0111 CPU:XFC=1:2^-15
0x100	c_pipe_mst2ints	Enable Registers to use pipelined paths from AHB Bus Masters to Internal SRAM [00] : AHB Bus Master #0 (CPU DCode) [01] : AHB Bus Master #1 (CPU ICode) [02] : AHB Bus Master #2 (CPU System) [03] : AHB Bus Master #3 (MAC DMA) [04] : AHB Bus Master #4 (uDMA/kDMA) [05] : AHB Bus Master #5 (SDeMMC) [06] : AHB Bus Master #6 (SPI/I2C Slave) [07] : AHB Bus Master #7 (Fast DMA M0) [08] : AHB Bus Master #8 (Fast DMA M1) [09] : AHB Bus Master #9 (CC-312 DMA) [10] : AHB Bus Master #A (XFC DMA) [11] : AHB Bus master #B (RW HSU) [12] : AHB Bus master #C (SDIO Slave) [13] : AHB Bus master #D (DBGT) [14] : AHB Bus master #E (Secure DMA) [15] : Reserved
0x104	c_pipe_ints2mst	Enable Registers to use pipelined paths from Internal SRAM to AHB Bus Masters
0x108	c_pipe_mst2mskr	Enable Registers to use pipelined paths from AHB Bus Masters to MaskROM
0x10C	c_pipe_mskr2mst	Enable Registers to use pipelined paths from MaskROM to AHB Bus Masters
0x110	c_pipe_mst2retm	Enable Registers to use pipelined paths from AHB Bus Masters to RetentionMem
0x114	c_pipe_retm2mst	Enable Registers to use pipelined paths from RetentionMem to AHB Bus Masters

0x120	c_pipe_mst2cfgs	Enable Registers to use pipelined paths to Configuration Registers [00] : CC-312 Env. CFGs [01] : Sys_Common CFGs (Common & Analog IPs) [02] : Sys_CPU CFGs [03] : Sys_ClkRst CFGs (Clock & Reset) [04] : Sys_ProtC CFGs (Protection Controller) [05] : Sys_AM2D CFGs (AHB Master to DMA) [06] : Sys_ClkGating [07] : Reserved
0x130	CLK_SET_WAIT_CPU	[0] Waiting control signal of CPU(or XFC) clock setting 0: Non-waiting 1: Waiting until XFC idle [1] force XFC clock to CPU clock [2] force CC-312 clock to CPU clock

Table 290: PLL_CLK_DIV_0_CPU (0x000)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_0_CPU	#0 Divider parameter to generate CPU Clock from PLL output 480MHz (for CPU & Bus Clock) 00 : Reserved 01 : 240.000 MHz (=480/2) 02 : 160.000 MHz (=480/3) 03 : 120.000 MHz (=480/4) 04 : 96.000 MHz (=480/5) 05 : 80.000 MHz (=480/6) 06 : 68.571 MHz (=480/7) 07 : 60.000 MHz (=480/8) 08 : 53.333 MHz (=480/9) 09 : 48.000 MHz (=480/10) 0A : 43.636 MHz (=480/11) 0B : 40.000 MHz (=480/12) 0C : 36.923 MHz (=480/13) 0D : 34.286 MHz (=480/14) 0E : 32.000 MHz (=480/15) 0F : 30.000 MHz (=480/16) 10 : 28.235 MHz (=480/17) 11 : 26.667 MHz (=480/18) 12 : 25.263 MHz (=480/19) 13 : 24.000 MHz (=480/20) 14 : 22.857 MHz (=480/21) 15 : 21.818 MHz (=480/22) 16 : 20.870 MHz (=480/23) 17 : 20.000 MHz (=480/24) 18 : 19.200 MHz (=480/25) 19 : 18.462 MHz (=480/26) 1A : 17.778 MHz (=480/27) 1B : 17.143 MHz (=480/28) 1C : 16.552 MHz (=480/29) 1D : 16.000 MHz (=480/30) 1E : 15.484 MHz (=480/31) 1F : 15.000 MHz (=480/32)	5'h05

Table 291: PLL_CLK_DIV_1_XFC (0x001)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_1_XFC	#1 Divider parameter to generate XFC Core Clock from PLL output 480MHz (for XFC Core Clock) XFC Core Clock Frequency must be n multiplication of CPU Clock Freq. (8>=n>=1)	5'h02

Table 292: PLL_CLK_DIV_2_UART (0x002)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_2_UART	#2 Divider parameter to generate UART Clock from PLL output 480MHz (for UART Clock)	5'h05

Table 293: PLL_CLK_DIV_3_OTP (0x003)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R	PLL_CLK_DIV_3_OTP	#3 Divider parameter to generate OTP Clock from PLL output 480MHz (for OTP Clock)	5'h17

Table 294: PLL_CLK_DIV_4_PHY (0x004)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R	PLL_CLK_DIV_4_PHY	#4 Divider parameter to generate PHY Clock from PLL output 480MHz (for PHY Clock)	5'h00

Table 295: PLL_CLK_DIV_5_I2S (0x005)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_5_I2S	#5 Divider parameter to generate I2S Clock from PLL output 480MHz (for I2S Clock)	5'h09

Table 296: PLL_CLK_DIV_6_AUXA (0x006)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_6_AUXA	#6 Divider parameter to generate AuxADC Clock from PLL output 480MHz (for AuxADC Clock) = 480/(PLL_CLK_DIV_6_AUXA+1) MHz maximum 240MHz ~ minimum 15.0 MHz	5'h1F

Table 297: PLL_CLK_DIV_7_CC312 (0x007)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	
4:0	R/W	PLL_CLK_DIV_7_CC312	#7 Divider parameter to generate CC-312 Core Clock from PLL output 480MHz	5'h05

Bit	Mode	Symbol	Description	Reset
			CC-312 Core Clock Frequency must be n multiplication of CPU Clock Freq. (8>=n>=1)	

Table 298: PLL_CLK_EN_0_CPU (0x010)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_0_CPU	PLL Counter Enable of #0 Divider	1'b0

Table 299: PLL_CLK_EN_1_XFC (0x011)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_1_XFC	PLL Counter Enable of #1 Divider	1'b0

Table 300: PLL_CLK_EN_2_UART (0x012)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_2_UART	PLL Counter Enable of #2 Divider	1'b0

Table 301: PLL_CLK_EN_3_OTP (0x013)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_3_OTP	PLL Counter Enable of #3 Divider	1'b0

Table 302: PLL_CLK_EN_4_PHY (0x014)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_4_PHY	PLL Counter Enable of #4 Divider	1'b0

Table 303: PLL_CLK_EN_5_I2S (0x015)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_5_I2S	PLL Counter Enable of #5 Divider	1'b0

Table 304: PLL_CLK_EN_6_AUXA (0x016)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	PLL_CLK_EN_6_AUXA	PLL Counter Enable of #6 Divider	1'b0

Table 305: PLL_CLK_EN_7_CC312 (0x017)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	

Bit	Mode	Symbol	Description	Reset
0	R/W	PLL_CLK_EN_7_CC312	PLL Counter Enable of #7 Divider	1'b0

Table 306: SRC_CLK_SEL_0_CPU (0x030)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_0_CPU	Selection signal of clock source #0 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_0)	1'b0

Table 307: SRC_CLK_SEL_1_XFC (0x031)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_1_XFC	Selection signal of clock source #1 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_1)	1'b1

Table 308: SRC_CLK_SEL_2_UART (0x032)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_2_UART	Selection signal of clock source #2 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_2)	1'b1

Table 309: SRC_CLK_SEL_3_OTP (0x033)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_3_OTP	Selection signal of clock source #3 in the Clock Generator 0: Xtal/2 (20MHz) 1: PLL path (PLL_CLK_DIV_3)	1'b0

Table 310: SRC_CLK_SEL_5_I2S (0x035)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_5_I2S	Selection signal of clock source #5 in the Clock Generator 0: External Clock from GPIO PADs 1: PLL path (PLL_CLK_DIV_5)	1'b0

Table 311: SRC_CLK_SEL_6_AUXA (0x036)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	

Bit	Mode	Symbol	Description	Reset
0	R/W	SRC_CLK_SEL_6_AUXA	Selection signal of clock source #6 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_6)	1'b1

Table 312: SRC_CLK_SEL_7_CC312 (0x037)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	SRC_CLK_SEL_7_CC312	Selection signal of clock source #7 in the Clock Generator 0: Xtal (40MHz) 1: PLL path (PLL_CLK_DIV_7)	1'b0

Table 313: SRC_CLK_STA_0 (0x070)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	
1:0	R	SRC_CLK_STA_0	Status of current clock source #0 in the Clock Generator 0: Xtal 1: Xtal to PLL 2: PLL 3: PLL to Xtal	2'h0

Table 314: IRQ_CLK_STA_0 (0x074)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	
1:0	R	IRQ_CLK_STA_0	Status of current interrupt in the Clock Generator 0: Xtal 1: Xtal to PLL 2: PLL 3: PLL to Xtal	2'h0

Table 315: CLK_DIV_I2S (0x085)

Bit	Mode	Symbol	Description	Reset
7:3	-	-	Reserved	
2:0	R/W	CLK_DIV_I2S	Last divider parameter to generate I2S Core Clock (MCLK) 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)	3'h0

Table 316: CLK_EN_CPU (0x090)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_CPU	Clock enable of CPU Clock	1'b1

Table 317: CLK_EN_XFC (0x091)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_XFC	Clock enable of XFC Core Clock	1'b0

Table 318: CLK_EN_UART (0x092)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_UART	Clock enable of UART Core Clock	1'b0

Table 319: CLK_EN_OTP (0x093)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_OTP	Clock enable of OTP Core Clock	1'b1

Table 320: CLK_EN_I2S (0x095)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_I2S	Clock enable of I2S Core Clock	1'b0

Table 321: CLK_EN_AUXA (0x096)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_AUXA	Clock enable of AuxADC Core Clock	1'b0

Table 322: CLK_EN_CC312 (0x097)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_CC312	Clock enable of CC-312 Core Clock	1'b1

Table 323: CLK_DIV_PHYBUS (0x0A0)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	
3:0	R	CLK_DIV_PHYBUS	Divider parameter to generate PHY Bus Clock from CPU Clock	4'h0

Table 324: CLK_DIV_EMMC (0x0A1)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	
3:0	R/W	CLK_DIV_EMMC	Divider parameter to generate SDeMMC Controller's Core Clock from CPU Clock 0: 1/(2^0) 1: 1/(2^1) 2: 1/(2^2)	4'h0

Bit	Mode	Symbol	Description	Reset
			n: 1/(2^n)	

Table 325: CLK_DIV_AUXA (0x0A4)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	
9:0	R/W	CLK_DIV_AUXA	Last divider parameter to generate AuxADC input clock from AuxADC reference PLL clock. 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)	10'h3E7

Table 326: CLK_EN_PHYBUS (0x0B0)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_PHYBUS	Clock enable of PHY Bus	1'b0

Table 327: CLK_EN_SDeMMC (0x0B1)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	
0	R/W	CLK_EN_SDeMMC	Clock enable of SDeMMC	1'b0

Table 328: DIFF_CPU_XFC (0x0F0)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	
5:0	R	DIFF_CPU_XFC	Ratio difference between CPU Clock and Flash Controller's Core Clock 00_0000 CPU:XFC=1:2^0 00_0001 CPU:XFC=1:2^1 00_0010 CPU:XFC=1:2^2 ..... 00_1011 CPU:XFC=1:2^7 10_0001 CPU:XFC=1:2^-1 10_0010 CPU:XFC=1:2^-2 ..... 10_0111 CPU:XFC=1:2^-15	6'h00

Table 329: c_pipe_mst2ints (0x100)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_mst2ints	Enable Registers to use pipelined paths from AHB Bus Masters to Internal SRAM [00] : AHB Bus Master #0 (CPU DCode) [01] : AHB Bus Master #1 (CPU ICode)	16'h0000

Bit	Mode	Symbol	Description	Reset
			[02] : AHB Bus Master #2 (CPU System) [03] : AHB Bus Master #3 (MAC DMA) [04] : AHB Bus Master #4 (uDMA/kDMA) [05] : AHB Bus Master #5 (SDeMMC) [06] : AHB Bus Master #6 (SPI/I2C Slave) [07] : AHB Bus Master #7 (Fast DMA M0) [08] : AHB Bus Master #8 (Fast DMA M1) [09] : AHB Bus Master #9 (CC-312 DMA) [10] : AHB Bus Master #A (XFC DMA) [11] : AHB Bus master #B (RW HSU) [12] : AHB Bus master #C (SDIO Slave) [13] : AHB Bus master #D (DBGT) [14] : AHB Bus master #E (Secure DMA) [15] : Reserved	

Table 330: c_pipe_ints2mst (0x104)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_ints2mst	Enable Registers to use pipelined paths from Internal SRAM to AHB Bus Masters	16'h0000

Table 331: c_pipe_mst2mskr (0x108)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_mst2mskr	Enable Registers to use pipelined paths from AHB Bus Masters to MaskROM	16'h0000

Table 332: c_pipe_mskr2mst (0x10C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_mskr2mst	Enable Registers to use pipelined paths from MaskROM to AHB Bus Masters	16'h0000

Table 333: c_pipe_mst2retm (0x110)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_mst2retm	Enable Registers to use pipelined paths from AHB Bus Masters to RetentionMem	16'h0000

Table 334: c_pipe_retm2mst (0x114)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_retm2mst	Enable Registers to use pipelined paths from RetentionMem to AHB Bus Masters	16'h0000

Table 335: c_pipe_mst2cfgs (0x120)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15:0	R/W	c_pipe_mst2cfgs	Enable Registers to use pipelined paths to Configuration Registers [00] : CC-312 Env. CFGs [01] : Sys_Common CFGs (Common & Analog IPs) [02] : Sys_CPU CFGs [03] : Sys_ClkRst CFGs (Clock & Reset) [04] : Sys_ProtC CFGs (Protection Controller) [05] : Sys_AM2D CFGs (AHB Master to DMA) [06] : Sys_ClkGating [07] : Reserved	16'h0000

Table 336: CLK_SET_WAIT_CPU (0x130)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	
2	R/W	CLK_SET_WAIT_CPU[2]	Force CC-312 clock to CPU clock	1'b0
1	R/W	CLK_SET_WAIT_CPU[1]	Force XFC clock to CPU clock	1'b0
0	R/W	CLK_SET_WAIT_CPU[0]	Waiting control signal of CPU (or XFC) clock setting 0: Non-waiting 1: Waiting until XFC idle	1'b1

10.13 Watchdog Register

The base address of Watchdog is 4000_8XXX.

Table 337: Watchdog Registers Overview

Offset	Register	Description
0x000	WDOGLOAD	Watchdog Load Register
0x004	WDOGVALUE	Watchdog Value Register
0x008	WDOGCONTROL	Watchdog Control Register
0x00C	WDOGINTCLR	Watchdog Clear Interrupt Register
0x010	WDOGRIS	Watchdog Raw Interrupt Status Register
0x014	WDOGMIS	Watchdog Interrupt Status Register
0xC00	WDOGLOCK	Watchdog Lock Register
0xF00	WDOGITCR	Watchdog Integration Test Control Register
0xF04	WDOGITOP	Watchdog Integration Test Output Set Register

Table 338: WDOGLOAD (0x000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WDOGLOAD	The WDOGLOAD register contains the value where the counter starts decrementing. When	32'hFFFFFFFF

Bit	Mode	Symbol	Description	Reset
			this register is written, the count is immediately restarted from the new value. The minimum valid value for WDOGLOAD is 1.	

Table 339: WDOGVALUE (0x004)

Bit	Mode	Symbol	Description	Reset
31:0	RO	WDOGVALUE	The WDOGVALUE register gives the current value of the decrementing counter.	32'hFFFFFFFF

Table 340: WDOGCONTROL (0x008)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved, read UNDEFINED, must read as 0s	
1	R/W	RESEN	Enable watchdog reset output, WDOGRES. Acts as a mask for the reset output. Set to 1 to enable the reset, or to 0 to disable the reset.	1'b0
0	R/W	INTEN	Enable the interrupt event, WDOGINT. Set to 1 to enable the counter and the interrupt, or to 0 to disable the counter and interrupt. Reloads the counter from the value in WDOGLOAD when the interrupt is enabled, after previously being disabled.	1'b0

Table 341: WDOGINTCLR (0x00C)

Bit	Mode	Symbol	Description	Reset
-	WO	WDOGINTCLR	A write of any value to the WDOGINTCLR register clears the watchdog interrupt, and reloads the counter from the value in WDOGLOAD	-

Table 342: WDOGRIS (0x010)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s	
0	RO	Raw Watchdog Interrupt	Raw interrupt status from the counter	1'b0

Table 343: WDOGMIS (0x010)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s	
0	RO	Watchdog Interrupt	Enabled interrupt status from the counter.	1'b0

Table 344: WDOGLOCK (0xC00)

Bit	Mode	Symbol	Description	Reset
31:1	R/W	Enable register writes	Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value.	31'h00000000
0	R/W	Register write enable status	0 Write access to all other registers is enabled. 1 Write access to all other registers is disabled.	0x0

Table 345: WDOGITCR (0xF00)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s	
0	RW	Integration Test Mode Enable	When set to 1, places the watchdog into integration test mode.	1'b0

Table 346: WDOGITOP (0xF04)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	
1	WO	Integration Test WDOGINT value	Value output on WDOGINT when in integration test mode.	1'b0
0	WO	Integration Test WDOGRES value	Value output on WDOGRES when in integration test mode.	1'b0

10.14 Timer Register

There are two Timers in DA162000. The base address of each Timer is:

- Timer0: 4000_0XXX
- Timer1: 4000_1XXX

Note that all timers have the same bit map.

Table 347: Timer Registers Overview

Offset	Register	Description
0x000	CTRL	Timer Control Register
0x004	VALUE	Timer Value Register
0x008	RELOAD	Timer Reload Value Register
0x00C	INTSTATUS INTCLEAR	Timer Interrupt Register. Write one to clear

Table 348: CTRL (0x000)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	
3	R/W	CTRL[3]	Timer Interrupt Enable	1'b0
2	R/W	CTRL[2]	Select External Input as clock	1'b0
1	R/W	CTRL[1]	Select External Input as enable	1'b0
0	R/W	CTRL[0]	Enable	1'b0

Table 349: VALUE (0x004)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	VALUE	Current Value	32'h00000000

Table 350: RELOAD (0x008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RELOAD	Reload value. A write to this register sets the current value after it reaches 0.	32'h00000000

Table 351: INTSTATUS/INTCLEAR (0x00C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	
-	R/W	INTSTATUS INTCLEAR	Timer interrupt. Write one to clear.	1'b0

11 Applications Schematic

11.1 Typical Application: QFN, 3.3 V Flash

Figure 58 shows the schematics for an application that uses the DA16200 in 3.3 V Flash mode.

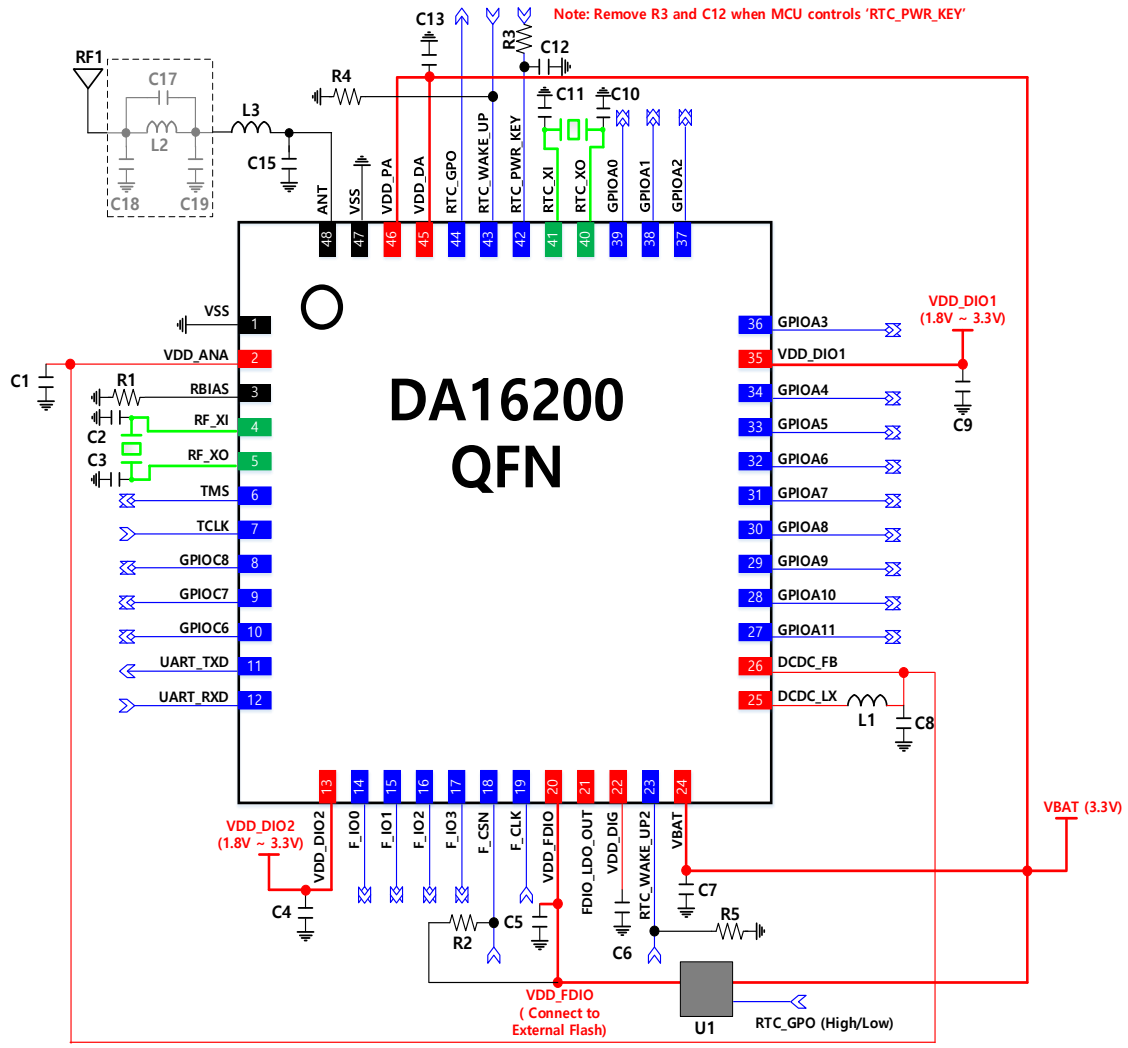

Figure 58: Typical Application – QFN, 3.3 V Flash

The power supply of the External Flash memory is the same as VDD_FDIO.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200.

Remove R3 and C12 when an MCU controls 'RTC_PWR_KEY'.

Table 352 lists the components for an application that uses the DA16200 QFN in 3.3 V Flash mode.

Table 352: Components for DA16200 QFN, 3.3 V Flash Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ (1 %)	

Quantity	Part Reference	Value	Description
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
5	C1, C4, C5, C7, C9	1 µF	
1	C6	470 nF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 uF	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1uF. See Section 6.1 for more information.
2	R4, R5	4.7 kΩ	
1	C13	4.7µF	
1	C15	DNI	Optional
1	L3	2.2 nH	
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional
1	U1		Optional, load switch for disconnecting VBAT for VDD_FDIO

(Use any 5 % tolerance)

Table 353: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

11.2 Typical Application: QFN, 1.8 V Flash

Figure 59 shows the schematics for an application that uses the DA16200 QFN in 1.8 V Flash mode.

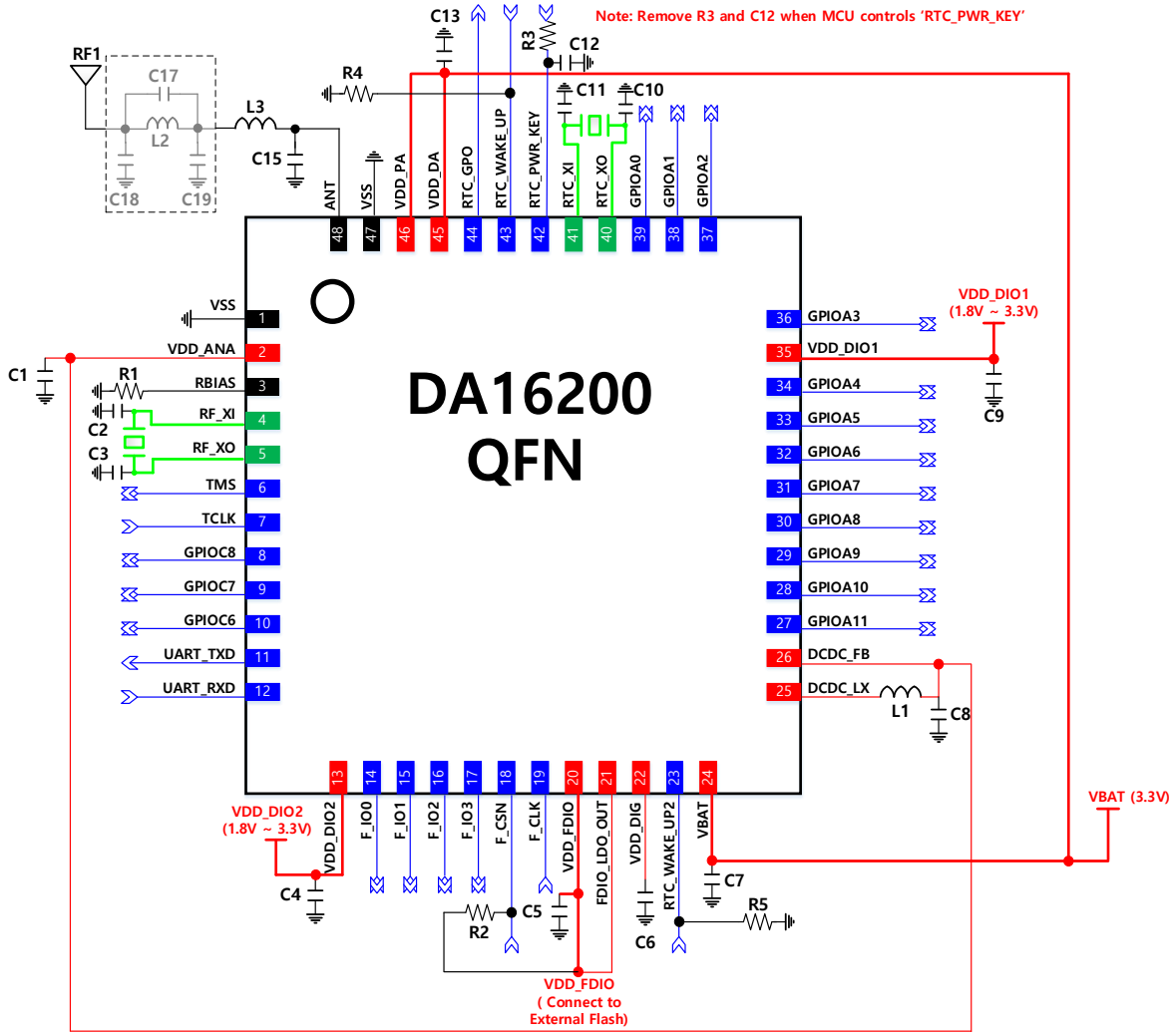

Figure 59: Typical Application – QFN, 1.8 V Flash

The power supply of the External Flash memory is the same as VDD_FDIO.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200.

Remove R3 and C12 when an MCU controls 'RTC_PWR_KEY'.

Table 354 lists the components for an application that uses the DA16200 QFN in 1.8 V Flash mode.

Table 354: Component for DA16200 QFN, 1.8 V Flash Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ (1 %)	
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
5	C1, C4, C5, C7, C9	1 µF	
1	C6	470 nF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. For detail information, see Section 6.1
1	C12	1 uF	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1uF. For detail information, see Section 6.1
2	R4, R5	4.7 kΩ	
1	C13	4.7 µF	
1	C15	DNI	Optional
1	L3	2.2 nH	
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5 % tolerance)

Table 355: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

11.3 Typical Application: fcCSP,1.8 V Flash Normal Power Mode

Figure 60 shows the schematics for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

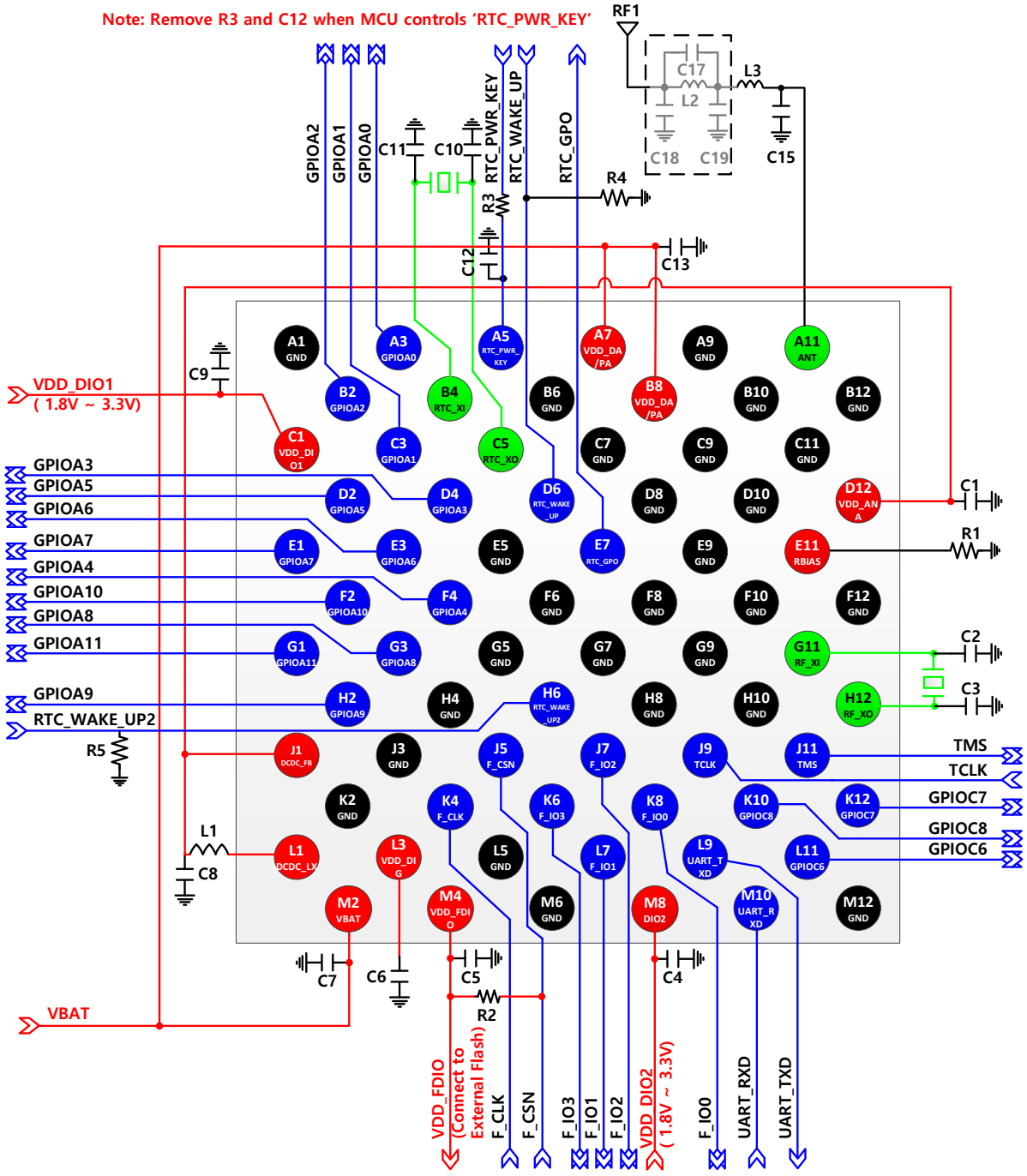

Figure 60: Typical Application – fcCSP, 1.8 V Flash, Normal Power Mode

The power supply of the External Flash memory is the same as VDD_FDIO.

3.3 V External Flash memory can also be used in this Application. A switch must be used to prevent the addition of flash memory current consumption to DA16200.

Please contact Customer support team for details.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls 'RTC_PWR_KEY'.

Table 356 lists the components for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

Table 356: Component for DA16200 fcCSP, 1.8 V Flash, Normal Power Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ (1 %)	
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
1	C6	470 nF	
4	C1, C4, C5, C9	1 µF	
1	C7	2.2 µF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 uF	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1uF. See Section 6.1 for more information.
1	R4, R5	4.7 kΩ	
1	C13	4.7 µF	
1	C15	0.5 pF	Normal power mode
1	L3	2.7 nH	Normal power mode
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5 % tolerance)

Table 357: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO (Note 1)	F_IO[3:0], F_CSN, F_CLK

Note 1 VDD_FDIO is internally connected to FDIO_LDO_OUT.

11.4 Typical Application: fcCSP,1.8 V Flash Low Power Mode

Figure 61 shows the schematics for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

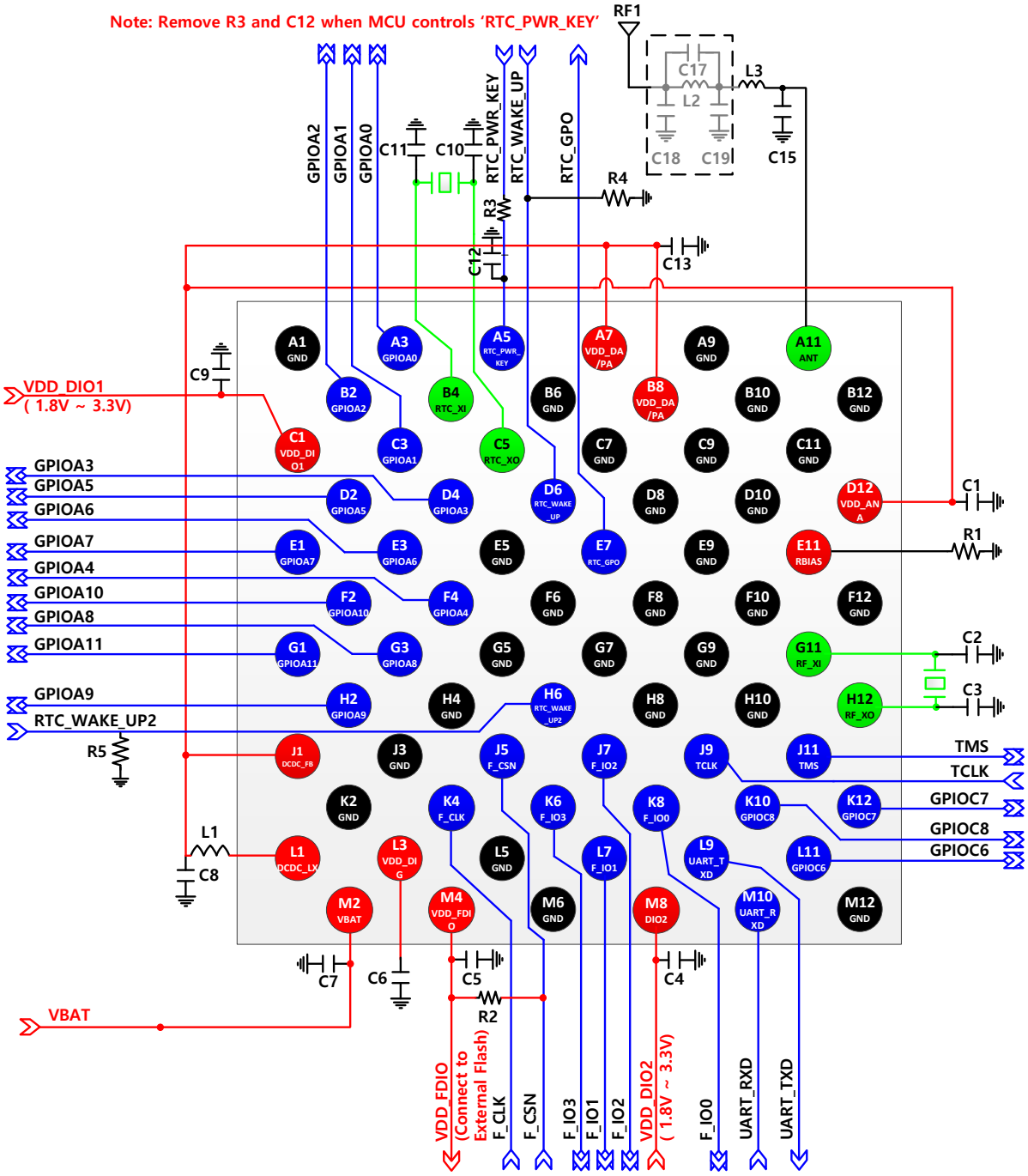

Figure 61: Typical Application – fcCSP, 1.8 V Flash, Low Power Mode

The power supply of the External Flash memory is the same as VDD_FDIO.

3.3 V External Flash memory can also be used in this Application. A switch must be used to prevent the addition of flash memory current consumption to DA16200.

Please contact Customer support team for details.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls 'RTC_PWR_KEY'.

Table 358 lists the components for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

Table 358: Component for DA16200 fcCSP, 1.8 V Flash, Low Power Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ (1 %)	
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
1	C6	470 nF	
4	C1, C4, C5, C9	1 µF	
1	C7	2.2 µF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 uF	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1uF. See Section 6.1 for more information.
1	R4, R5	4.7 kΩ	
1	C13	4.7 µF	
1	C15	DNI	Low power mode
1	L3	2.2 nH	Low power mode
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5 % tolerance)

Table 359: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO (Note 1)	F_IO[3:0], F_CSN, F_CLK

Note 1 VDD_FDIO is internally connected to FDIO_LDO_OUT.

12 Package Information

12.1 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60 % RH before the solder reflow process.

QFN and fcCSP packages are qualified for MSL 3.

Table 360: Moisture Sensitivity Level

Moisture Sensitivity Level (MSL)	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85 %RH

12.2 Top View: QFN and fcCSP

Figure 62: DA16200 48-Pin QFN Package

Figure 63: DA16200 72-Pin fcCSP Package

12.3 Dimension: 48-Pin QFN

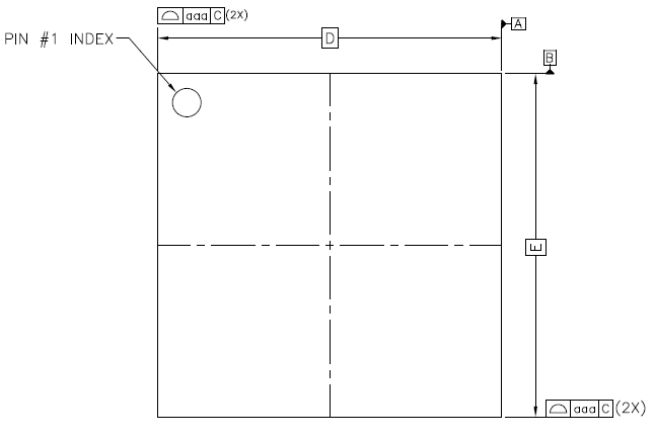

Figure 64: Top View

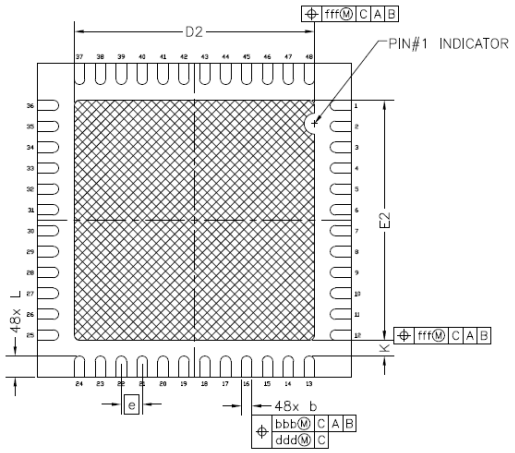

Figure 65: Bottom View

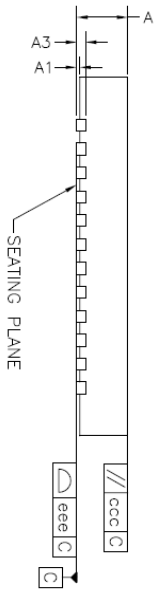

Figure 66: Side View

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20		
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 67: DA16200 48-Pin QFN Package Dimensions

12.4 Dimension: 72-Pin fcCSP

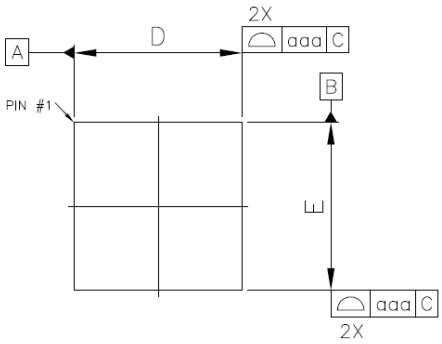

Figure 68: Top View

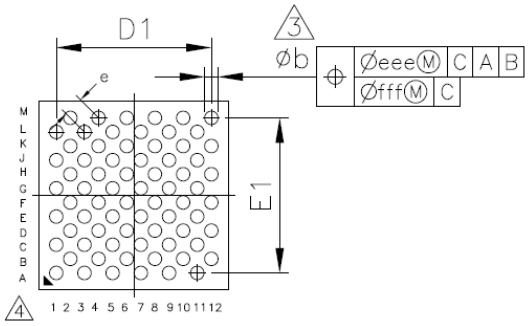

Figure 69: Bottom View

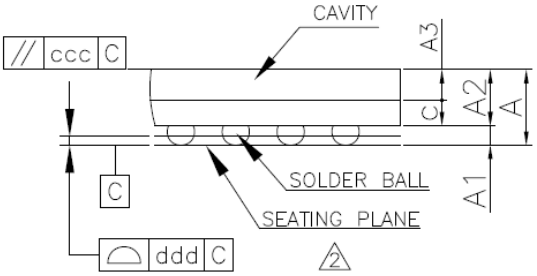

Figure 70: Side View

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.54	0.61	0.68
A1	0.11	0.16	0.21
A2	0.40	0.45	0.50
A3	0.25	0.28	0.31
c	0.14	0.17	0.20
D	3.73	3.80	3.87
E	3.73	3.80	3.87
D1	---	3.11	---
E1	---	3.11	---
e	---	0.40	---
b	0.22	0.27	0.32
aaa	0.07		
ccc	0.10		
ddd	0.08		
eee	0.10		
fff	0.05		
MD/ME	12/12		

Figure 71: DA16200 72-Pin fcCSP Package Dimensions

12.5 Land Pattern: 48-Pin QFN

Unit: Millimeters (mm)

Pad: Metal mask = 1:1

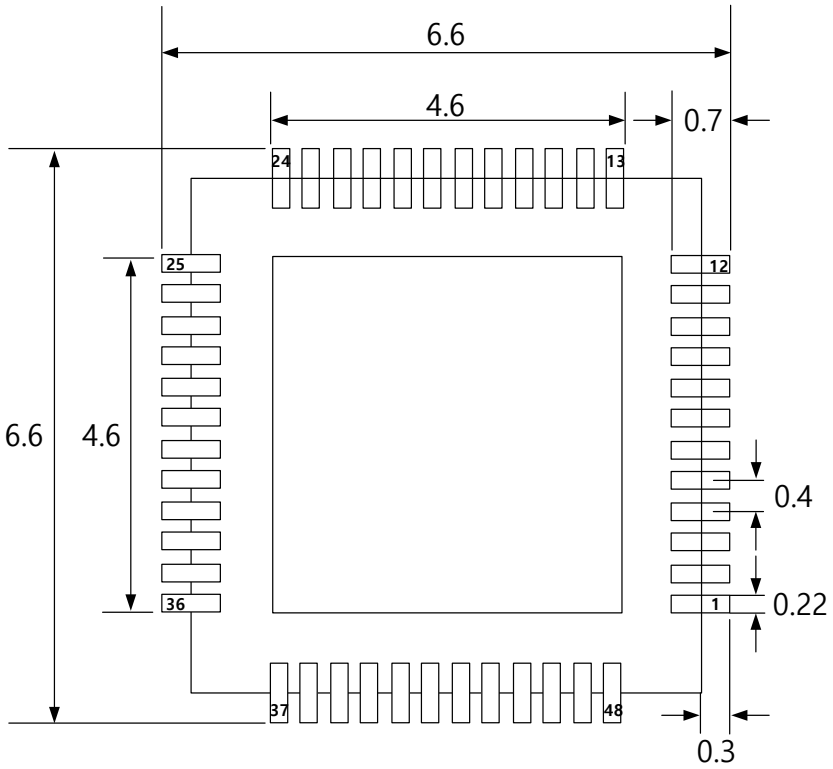

Figure 72: DA16200 48-Pin QFN Land Pattern

12.6 Land Pattern: 72-Pin fcCSP

Unit: Millimeters (mm)

Pad: Metal mask = 1:1

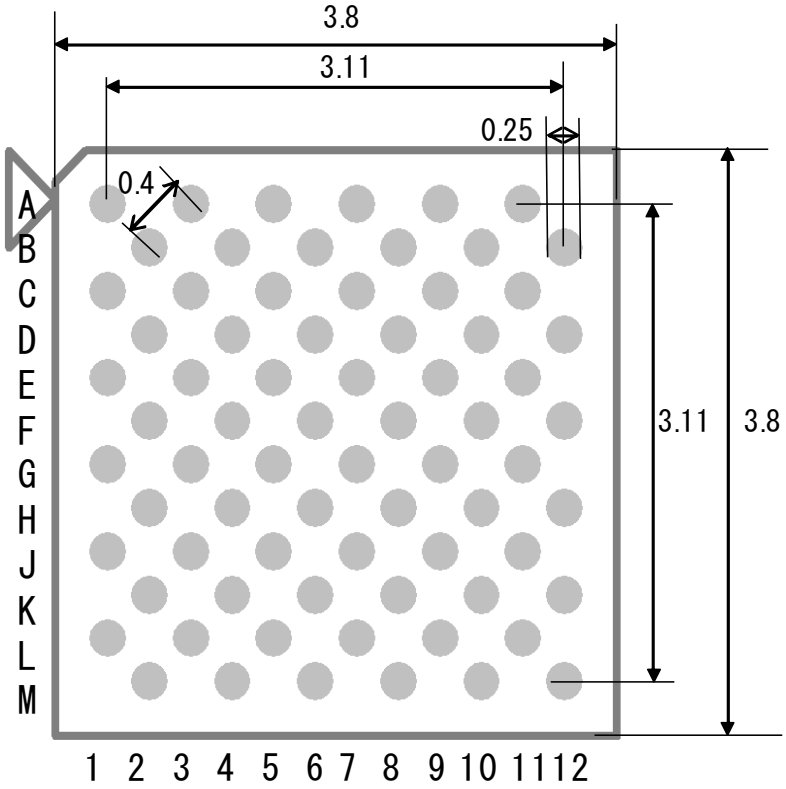

Figure 73: DA16200 72-Pin FcCSP Land Pattern

12.7 Soldering Information

12.7.1 Recommended Condition for Reflow Soldering

Figure 74 shows the typical process flow to install surface mount packages to the PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacturer should be followed to determine the proper reflow profile. Figure 74 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 30 to 60 seconds.

Since solder joints are not exposed in QFN packages, any retouch is not possible and the whole package has to be removed if the surface mount process results in shorts or opens. Furthermore, rework of QFN packages can be a challenge due to their small size. In most applications, QFNs will be installed on smaller, thinner, and denser PCBs, and introduces further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following steps only provide a guideline and a starting point for the development of a successful rework process for the QFN packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement
5. Component attachment

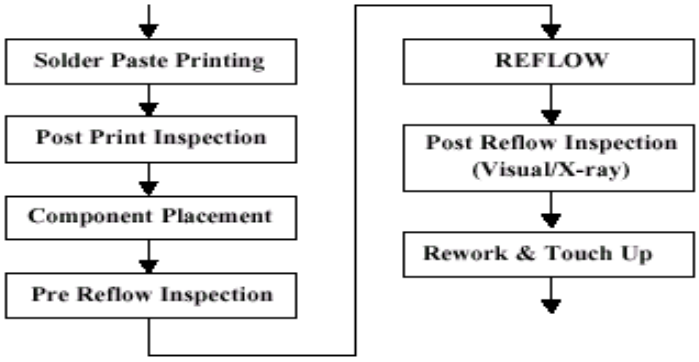

Figure 74: Typical PCB Mounting Process Flow

Table 361: Typical Reflow Profile (Lead Free): J-STD-020C

Profile Feature	Lead Free SMD
Average ramp up rate (Ts_{max} to T_p)	3 °C/s Max.
Preheat	
• Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{max} to Ts_{min})	• 150 °C • 200 °C • 60 to 180 seconds
Time maintained above	
• Temperature (T_L) • Time (t_L)	• 217 °C • 60 to 150 seconds
Peak/Classification temperature (T_p)	260 °C
Time within 5 °C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6 °C/s Max.
Time from 25 °C to peak temperature	8 minutes Max.

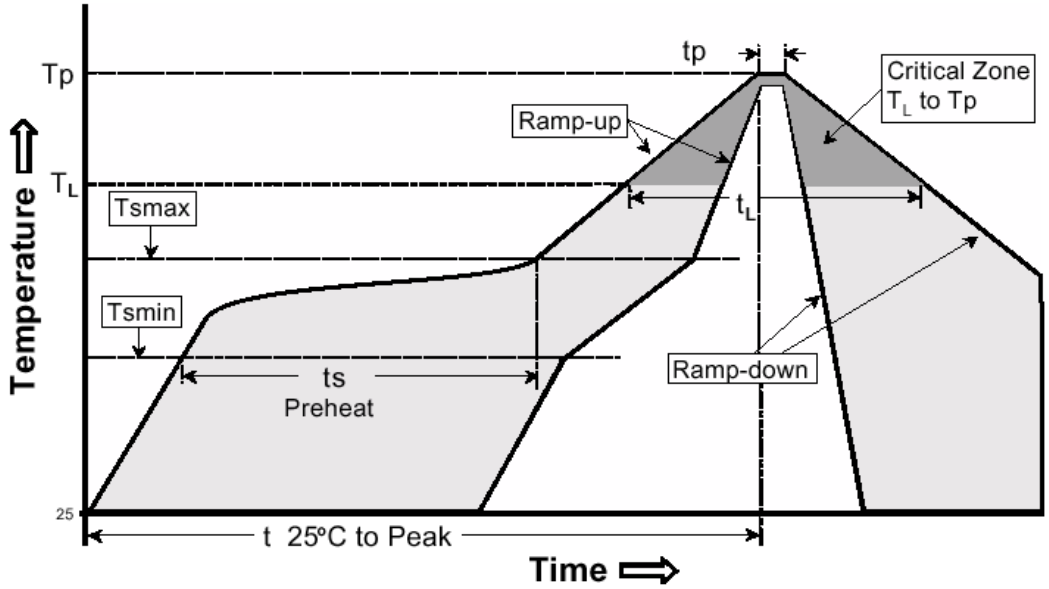

Figure 75: Reflow Condition

13 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, visit https://www.renesas.com/kr/en/products/wireless-connectivity/wi-fi/low-power-wi-fi or contact your local sales representative.

Table 362: Ordering Information (Samples)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA16200-00000A32	QFN48	6 × 6	Reel	100/500
DA16200-00001A32	QFN48	6 × 6	Reel	100/500
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	100/500
DA16200-00001F22	fcCSP72	3.8 × 3.8	Reel	100/500

Table 363: Ordering Information (Production)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA16200-00000A32	QFN48	6 × 6	Reel	3000
DA16200-00001A32	QFN48	6 × 6	Reel	3000
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	4000
DA16200-00001F22	fcCSP72	3.8 × 3.8	Reel	4000

Part Number Legend:

DA16200-RRXXXYYZ

RR: Chip revision number

YY: package code (A3: QFN48, F2: fcCSP72)

Z: packing method (1: Tray, 2: Reel, A: Mini-Reel)

Revision History

Revision	Date	Description

3.7	12-Jul-2023	• Removed Variant 001 details
		• Updated the reference section
		• Added Register Maps:
		  ○ ADC Register
		  ○ CRC Register
		  ○ PWM Register
		  ○ kDMA Register
		  ○ SYS_CLOCK Register
		  ○ Watchdog Register
		  ○ Timer Register
		• Updated Table 3 and Table 4
		• Updated Figure 3 and 6.3.3
		• Changed the format: figure 58/figure 59 to table 131 and table 132

3.6	04-Jan-2023	• Section 7.5.1, 9.8.4, Table 29 added details for sleep modes • Updated operating temperature in Key Features list • Updated Table 5 to add storage temperature range and adjusted min/max voltages
3.5	13-Jun-2022	• Section 7.3.1.2 Corrected the internal SRAM address range • Section 7.4.2 Added note about Sleep mode 2 &3 for retention I/O • Section 9.3 and Section 10.5 Added note about SPI slave half-duplex and clock speed calculation • Table 33 Changed to Chacha20 and Poly1305 • Table 53 Removed Input Tolerance
3.4	17-Jan-2022	• Section 4.3 Updated Pinout Multiplexing • Section 5.8 Updated Clock Electrical Characteristics • Section 9.3 fixed typo • Section 9.4 Added SDIO interface needs pull-up resistors description and Figure 32 • Section 9.5.3 Added I2C Interface Pull-up • Section 9.12 Updated SWD part Table 61 • Section 11.3 and 11.4 Updated Description • Update to the operating temperature range • Updates to for variant 001. (OTP Size, BT Coex, BOR registers) • Table 9 Updated the Guaranteed logic High level V_{IH} to 2,3V
3.3	03-Fab-2021	• Table 1 Updated Pinout Description • Section 6.1 Added Note for Power on Sequence and Updated Table 26 and Figure 11 • Section 9.7.3 Fixed typo • Section 10 Updated RC Delay Description (Table 61, Table 63, Table 65, Table 67 and Figure 56, Figure 57, Figure 58, Figure 59)

Revision	Date	Description
3.2	28-Sep-2020	• Section 6.3 Updated Sleep mode Description • Removed F_xx pins in Interface Parts. • Section 4.3 (Table 3) Updated Pin Multiplexing • Section 9.8 (Table 52) Updated ADC Reference Voltage • Section 9.5.1 and 9.5.2 Updated I2C Speed Description • Section 9.5 Updated I2C interface (Table 43) and (Table 45) • Section 9.7.1 and 9.7.2 Added, I2S Description, Block Diagram, and Clock Scheme • Section 9.8.2 Table 52 Swapped SNDR, SNR value
3.1	3-Jul-2020	• Section 3, Modified Description to Network subsystem layer. • Section 3, Figure 2 Modified Hardware Block diagram • Section 4.2 (Table 1), Reset state changed to Initial state. • Section 4.3 (Table 3) Updated Pin multiplexing. • Section 5.2 (Table 5) Updated FDIO_LDO_OUT value • Section 5.3 Updated Electrical Characteristics • Section 5.4.2 (Table 14) Updated fcCSP TX min/max value • Section 5.5 Updated Current Consumption value • Section 6.2 Added Description and Updated Power management block diagram (Figure 12). • Section 6.3 Updated Sleep mode Description • Section 7.4 (Table 28) Updated RTC_PWR_KEY description and Remove one sentence which leads to misunderstanding. • Section 9.5.1 (Table 43),(Table 45) Updated I2C Speed • Section 9.9.1 Added Diversity Description and (Figure 46) • Section 9.10.3 Added UART Baud rate Description • Section 10.1, 10.2 Updated QFN Application Schematic (Figure 56),(Figure 57) and Description. • Section 10.3, 10.4 Updated fcCSP Application Schematic (Figure 58),(Figure 59) and Description, (Table 65), (Table 67). And Added note after table IO Power Domain • Page 93 Updated Description about Reach and RoHS Compliance
3.0	26-Mar-2020	• Final release
2.9	11-Feb-2020	• Feature, Wi-Fi Alliance certification: Detailed added • Section 5.4.1 and 5.4.2 measurement condition CH1 added • Section 9.10.1 RS-232 added • Section 9.10.3 Hardware Flow Control added • Section 9.10.4 Interrupts added • Table 3 Pin Multiplexing changed • Section 11.1 MSL added • Figure 54. DA16200 fcCSP Package Top view added • Application circuit (QFN, fcCSP) BOM changed • Feature deleted: DPD function support • Rx and Tx min/max value added for the QFN package (Table 12 and Table 14) • Rx and Tx min/max value added for the fcCSP package (Table 13 and Table 15) • Table 17 and Table 20 updated • ESD ratings added for the QFN and fcCSP packages in Table 21 and Table 22

Revision	Date	Description
2.3	5-Sep-2019	• Pin name "RTC_SEN_OUT" changed to "RTC_GPO" • Pull-down resistor added in Figure50, Figure51, Figure52 • QFN48 package "RTC_WAKE_UP" and "RTC_WAKE_UP2" • fcCSP72 package "RTC_WAKE_UP" • Ordering information sample and production pack quantity updated • Application circuit revised in QFN and fcCSP package • RTC_WAKE_UP pull-down resistor added
2.2	12-Aug-2019	• Added Figure 71: DA16200 72-Pin fcCSP Land Pattern • AC characteristics and current consumption of fcCSP data updated in Table 13, Table 15, and Table 18 • Ordering information added
2.1	30-Jul-2019	• Added "3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP" in package type in key features • Added Figure 5, Figure 8, and Figure 10 • Added pin numbers for fcCSP package in Table 1, Table 28, Table 34, Table 38, Table 40, Table 42, Table 44, Table 46, Table 48, Table 53, Table 56, and Table 60 • Added "GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD" in the description of Pin13/M8 in Table 1 • Added "GPIOA0~GPIOA11" in the description of Pin35/C1 in Table 1 • Added "fcCSP GND Pin A1,A9,B6,B10,B12,C7,C9,C11,D8,D10,F6,F8,F10,F12,G5,G7,G9, H4,H8,H10,J3,K2,L5,M6,M12,E5" in Table 1 • In Table 3 SPI master contents updated • Added information on fcCSP pins in section 5.1 and 5.2 • Added Table 13, Table 15, and Table 18 • Added section 10.3 • Updated section 11.1 to include information on fcCSP • Added section 11.4 • Changed the caption of Table 27 to "OTP Map"
2.0	03-Jul-2019	Preliminary datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

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