

27A, 600V, UFS Series N-Channel IGBTs with Anti-Parallel Hyperfast Diode

December 1997

Features

- 27A, 600V, $T_C = 25^\circ\text{C}$
- 600V Switching SOA Capability
- Typical Fall Time 112ns at $T_J = 150^\circ\text{C}$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60B3D	TO-220AB	12N60B3D
HGTG12N60B3D	TO-247	12N60B3D
HGT1S12N60B3D	TO-262AA	12N60B3D
HGT1S12N60B3DS	TO-263AB	12N60B3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g. HGT1S12N60B3DS9A.

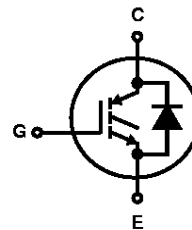
Description

This family of MOS gated high voltage switching devices combine the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C . The IGBT used is the development type TA49171. The diode used in anti-parallel with the IGBT is the development type TA49188.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

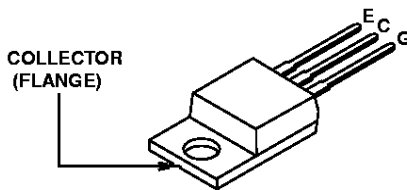
Formerly developmental type TA49173.

Symbol

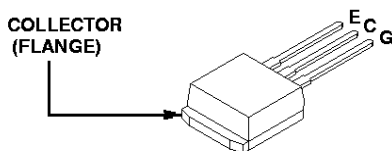


Packaging

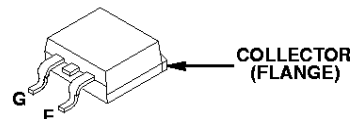
JEDEC TO-220AB (ALTERNATE VERSION)



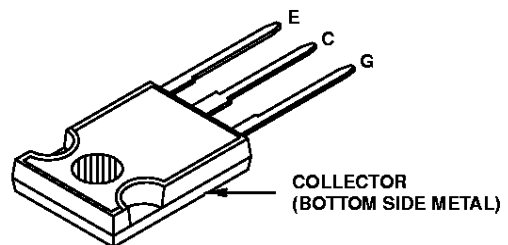
JEDEC TO-262AA



JEDEC TO-263AB



JEDEC STYLE TO-247



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS	UNITS
Collector to Emitter Voltage	BV_{CES}	600 V
Collector Current Continuous	I_{C25}	27 A
At $T_C = 110^\circ\text{C}$	I_{C110}	12 A
Collector Current Pulsed (Note 1)	I_{CM}	110 A
Gate to Emitter Voltage Continuous	V_{GES}	± 20 V
Gate to Emitter Voltage Pulsed	V_{GEM}	± 30 V
Switching Safe Operating Area at $T_J = 150^\circ\text{C}$, Figure 2	SSOA	96A at 600V
Maximum Power Dissipation	P_D	104 W
Linear Derating Factor		0.83 $\text{W}/^\circ\text{C}$
Reverse Voltage Avalanche Energy	E_{ARV}	100 mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, see Techbrief 334	T_{pkg}	260 $^\circ\text{C}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 12\text{V}$	t_{SC}	5 μs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10\text{V}$	t_{SC}	10 μs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Pulse width limited by maximum junction temperature.
- $V_{CE(PK)} = 360\text{V}$, $T_J = 125^\circ\text{C}$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu\text{A}$, $V_{GE} = 0\text{V}$	600	-	-	V	
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^\circ\text{C}$	-	-	250	μA
			$T_C = 150^\circ\text{C}$	-	-	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15\text{V}$	$T_C = 25^\circ\text{C}$	-	1.6	2.1	V
			$T_C = 150^\circ\text{C}$	-	1.7	2.5	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu\text{A}$, $V_{CE} = V_{GE}$	4.5	4.9	6.0	V	
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20\text{V}$	-	-	± 250	nA	
Switching SOA	SSOA	$T_J = 150^\circ\text{C}$, $R_G = 25\Omega$, $V_{GE} = 15\text{V}$ $L = 100\mu\text{H}$, $V_{CE} = 600\text{V}$	96	-	-	A	
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5 BV_{CES}$	-	7.3	-	V	
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5 BV_{CES}$	$V_{GE} = 15\text{V}$	-	51	60	nC
			$V_{GE} = 20\text{V}$	-	68	78	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^\circ\text{C}$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8 BV_{CES}$ $V_{GE} = 15\text{V}$ $R_G = 25\Omega$ $L = 1\text{mH}$ Test Circuit - (Figure 19)	-	26	-	ns	
Current Rise Time	t_{rI}		-	23	-	ns	
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	150	-	ns	
Current Fall Time	t_{fI}		-	62	-	ns	
Turn-On Energy (Note 4)	E_{ON1}		-	150	-	μJ	
Turn-On Energy (Note 4)	E_{ON2}		-	304	350	μJ	
Turn-Off Energy (Note 3)	E_{OFF}		-	250	350	μJ	
Current Turn-On Delay Time	$t_{d(ON)I}$		IGBT and Diode at $T_J = 150^\circ\text{C}$ $I_{CE} = I_{C110}$ $V_{CE} = 0.8 BV_{CES}$ $V_{GE} = 15\text{V}$ $R_G = 25\Omega$ $L = 1\text{mH}$ Test Circuit - (Figure 19)	-	22	-	ns
Current Rise Time	t_{rI}			-	23	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	280	295	ns
Current Fall Time	t_{fI}	-		112	175	ns	
Turn-On Energy (Note 4)	E_{ON1}	-		165	-	μJ	
Turn-On Energy (Note 4)	E_{ON2}	-		500	525	μJ	
Turn-Off Energy (Note 3)	E_{OFF}	-		660	800	μJ	

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_{EC}	$I_{EC} = 12\text{A}$	-	1.7	2.1	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 12\text{A}, dI_{EC}/dt = 200\text{A}/\mu\text{s}$	-	32	40	ns
		$I_{EC} = 1.0\text{A}, dI_{EC}/dt = 200\text{A}/\mu\text{s}$	-	23	30	ns
Thermal Resistance Junction To Case	$R_{\theta JC}$	IGBT	-	-	1.2	$^\circ\text{C}/\text{W}$
		Diode	-	-	1.9	$^\circ\text{C}/\text{W}$

NOTES:

- Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0\text{A}$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.
- Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 19.

Typical Performance Curves (Unless Otherwise Specified)

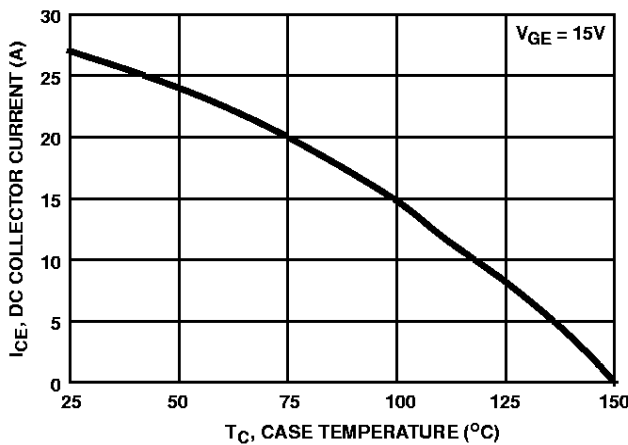


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

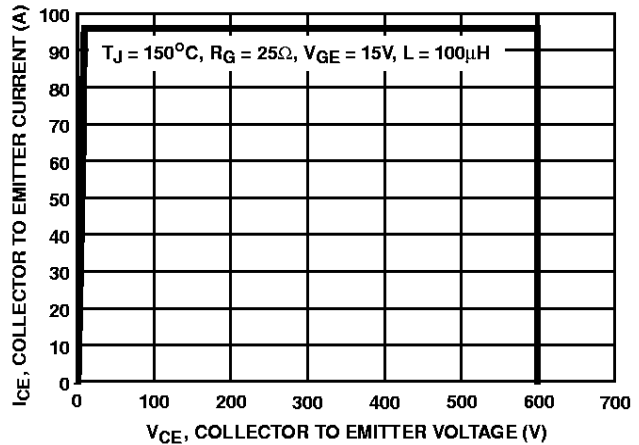


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

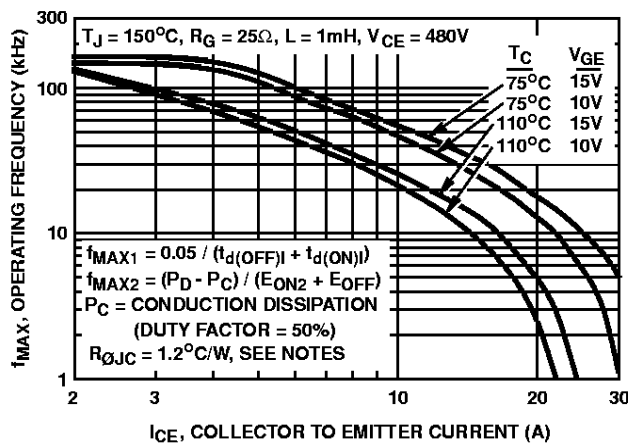


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

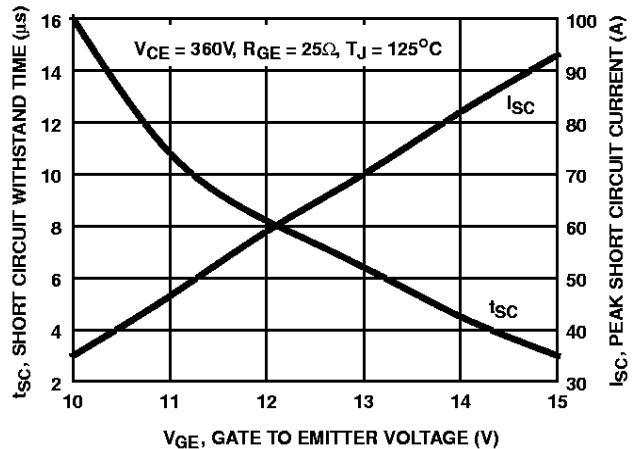


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Unless Otherwise Specified) (Continued)

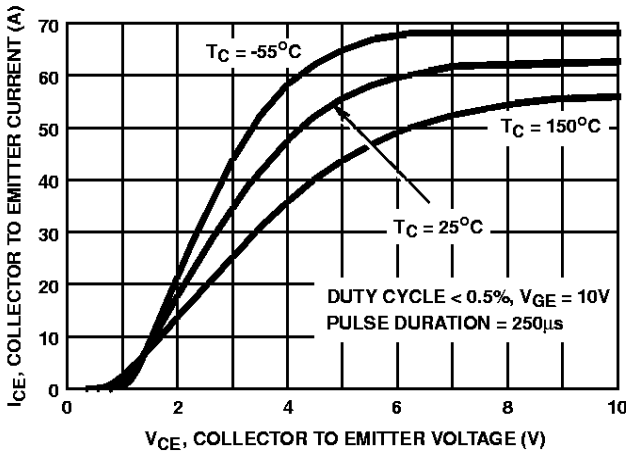


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

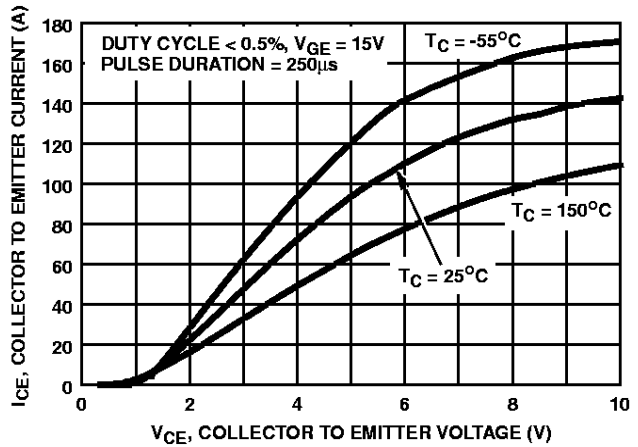


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

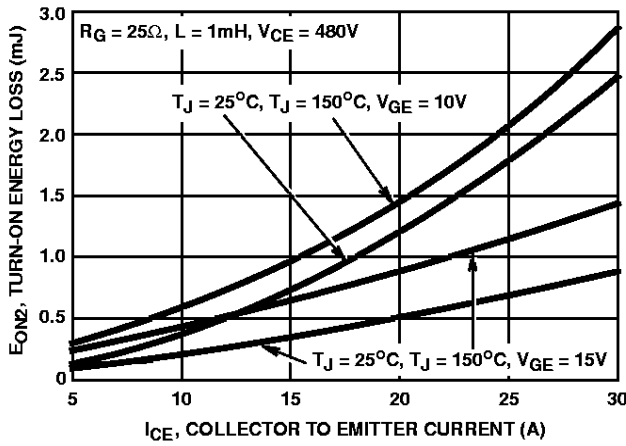


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

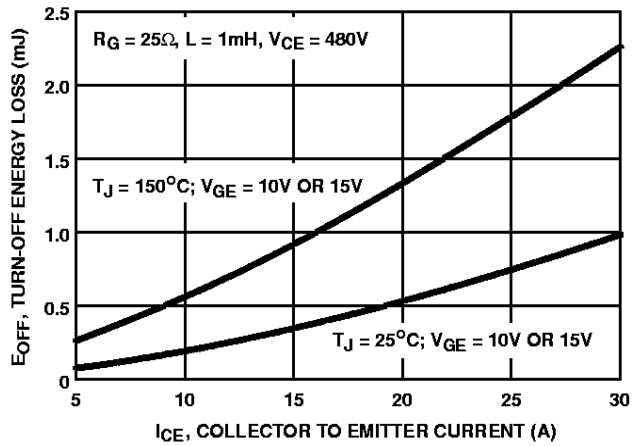


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

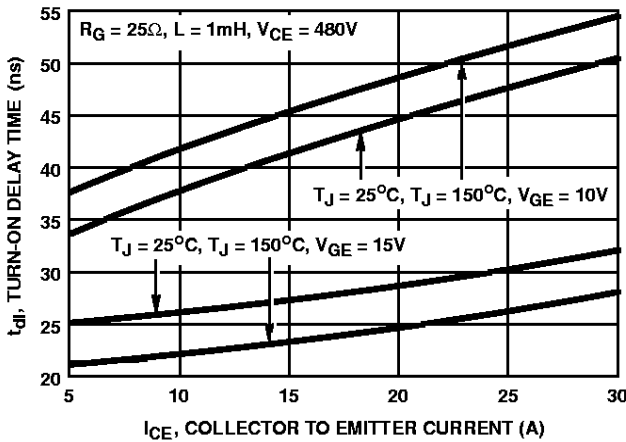


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

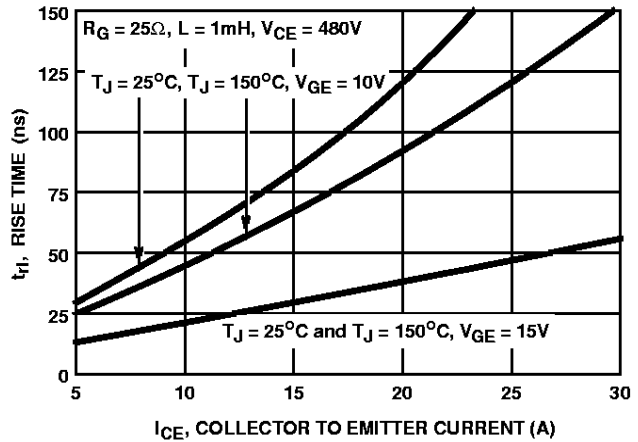


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves (Unless Otherwise Specified) (Continued)

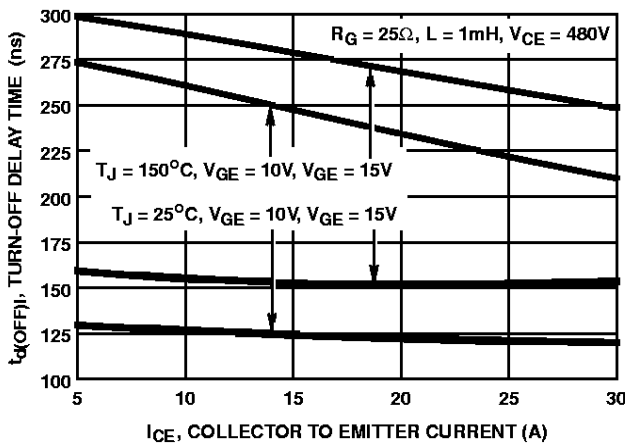


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

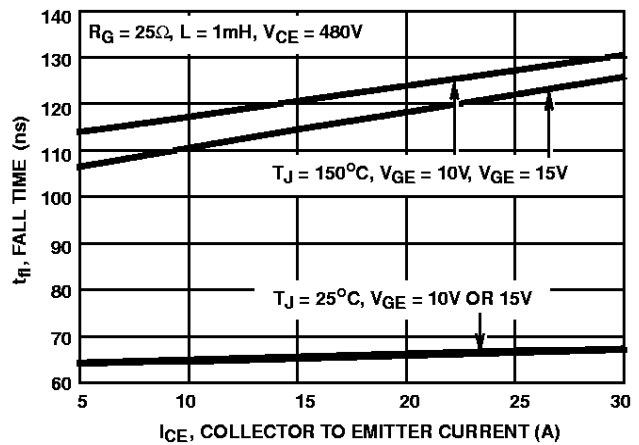


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

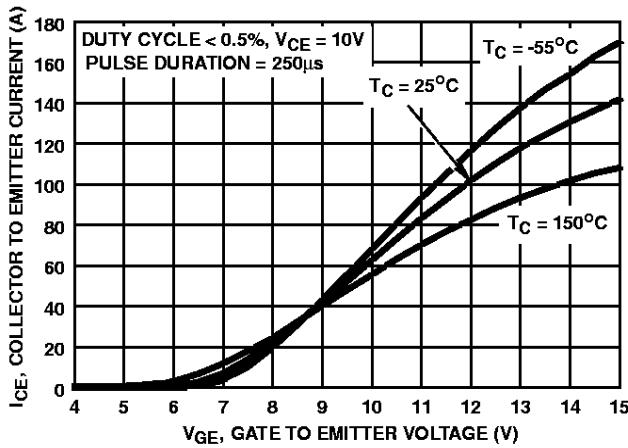


FIGURE 13. TRANSFER CHARACTERISTIC

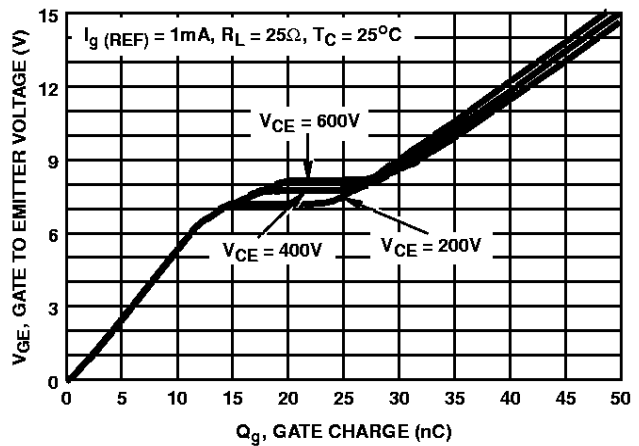


FIGURE 14. GATE CHARGE WAVEFORMS

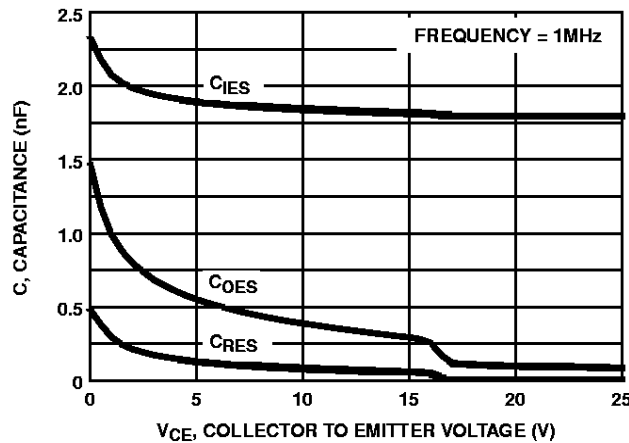


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR TO EMITTER VOLTAGE

Typical Performance Curves (Unless Otherwise Specified) (Continued)

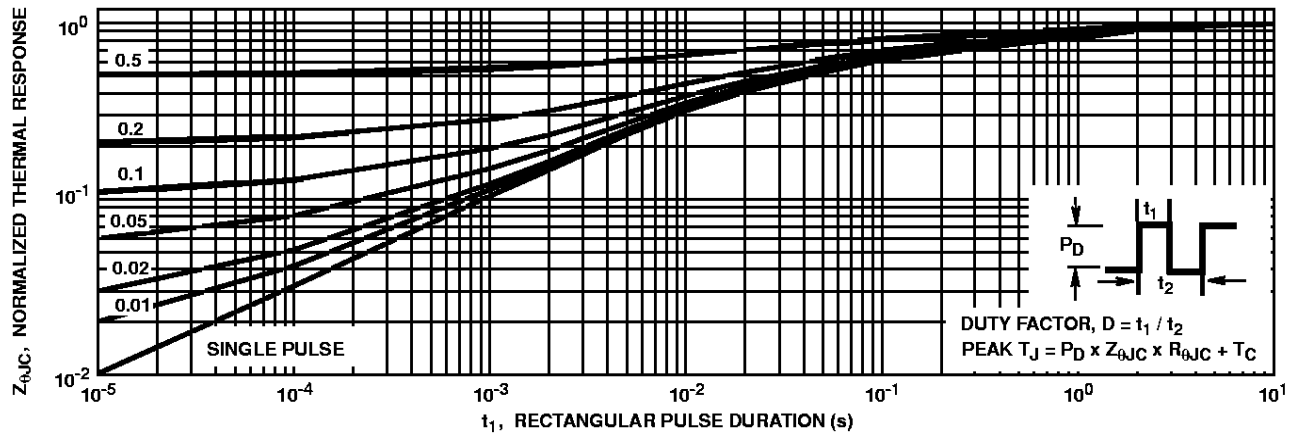


FIGURE 16. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

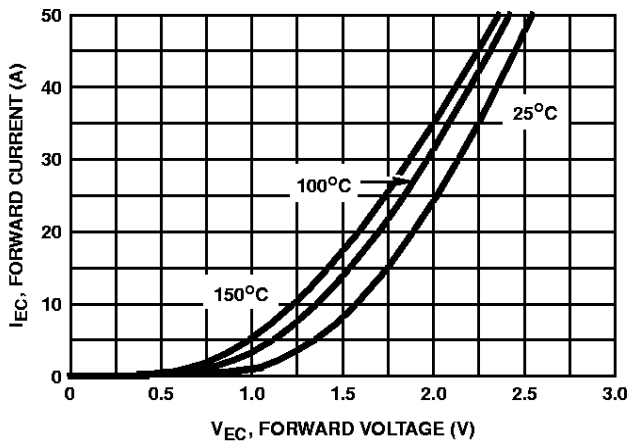


FIGURE 17. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

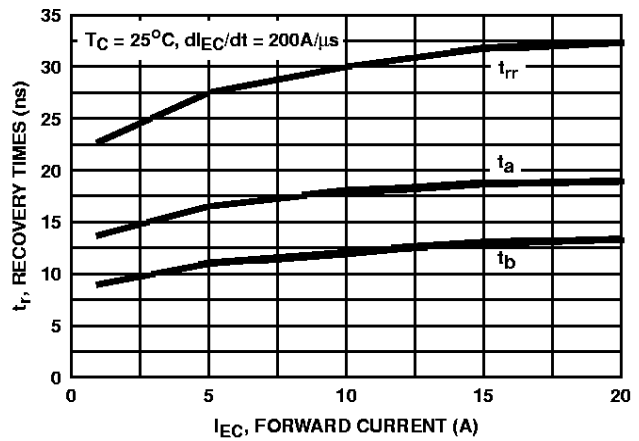


FIGURE 18. RECOVERY TIMES vs FORWARD CURRENT

Test Circuit and Waveforms

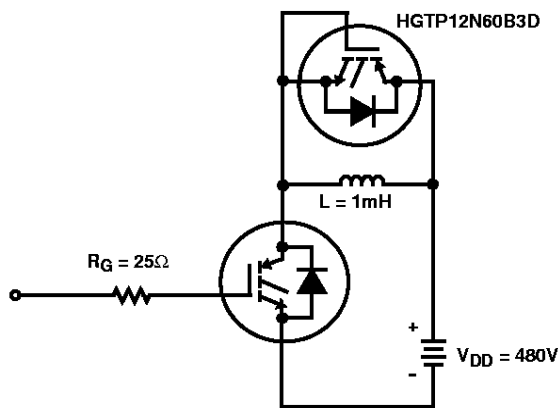


FIGURE 19. INDUCTIVE SWITCHING TEST CIRCUIT

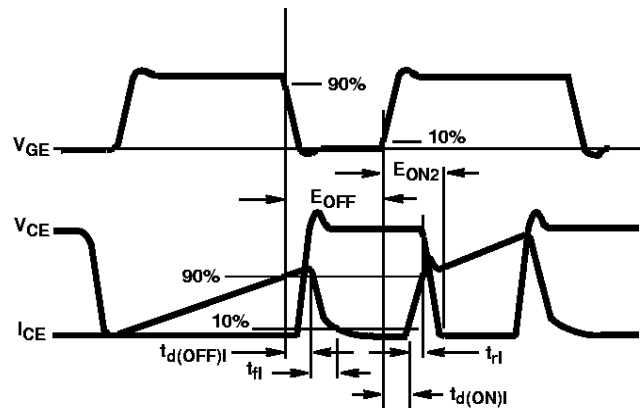


FIGURE 20. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM} . Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2} ; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)} + t_{d(ON)})$. Dead-time (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)}$ and $t_{d(ON)}$ are defined in Figure 20. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX} . $t_{d(OFF)}$ is important when controlling output ripple under a lightly loaded condition.

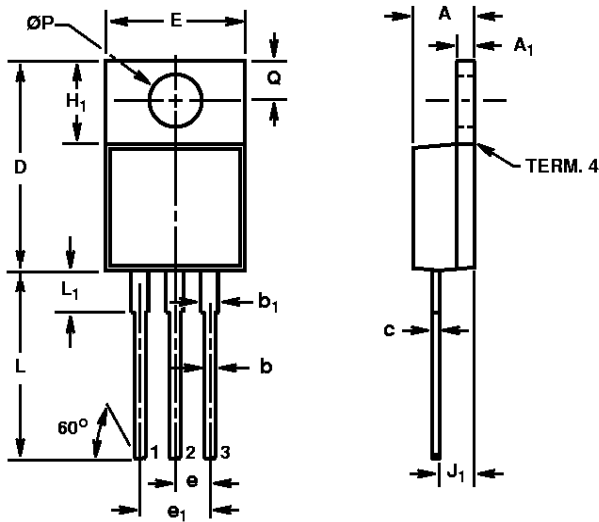
f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D . A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 20. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF} ; i.e., the collector current equals zero ($I_{CE} = 0$).

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

TO-220AB (Alternate Version)

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



- LEAD 1 - GATE
- LEAD 2 - COLLECTOR
- LEAD 3 - EMITTER
- TERM. 4 - COLLECTOR

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	2, 4
b	0.030	0.034	0.77	0.86	2, 4
b ₁	0.045	0.055	1.15	1.39	2, 4
c	0.018	0.022	0.46	0.55	2, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	3
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

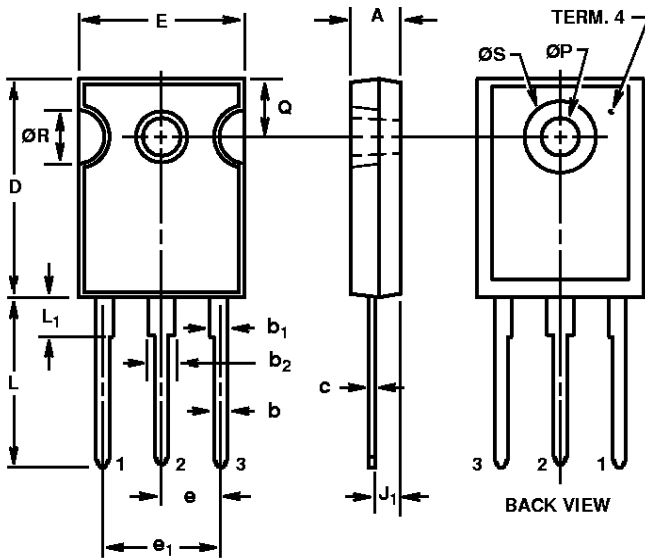
NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Dimension (without solder).
3. Solder finish uncontrolled in this area.
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 7-97.

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



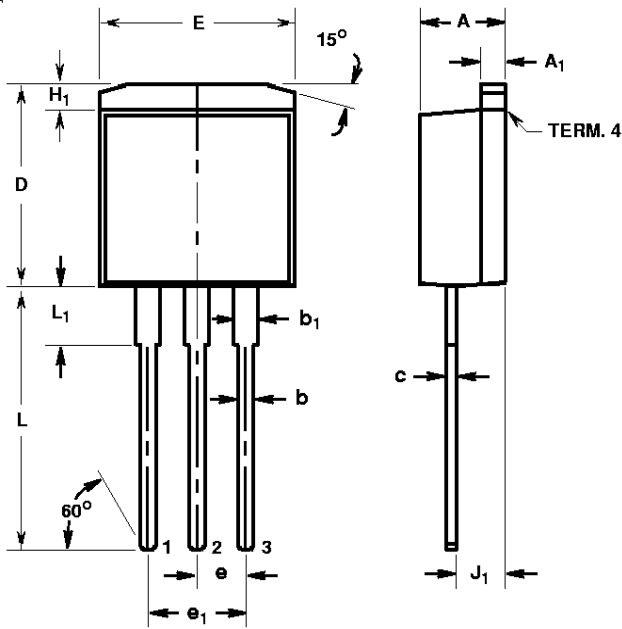
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



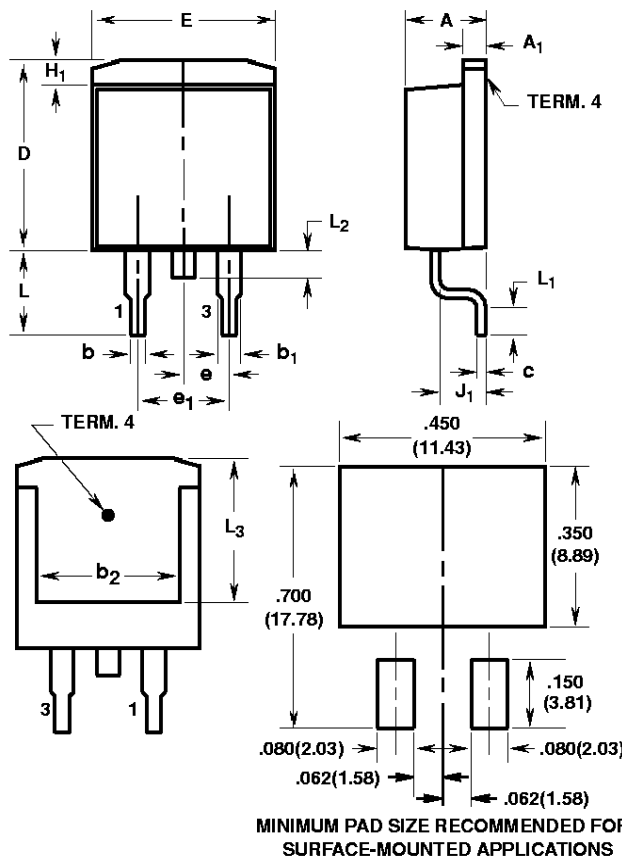
- LEAD 1 - GATE
- LEAD 2 - COLLECTOR
- LEAD 3 - EMITTER
- TERM. 4 - COLLECTOR

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

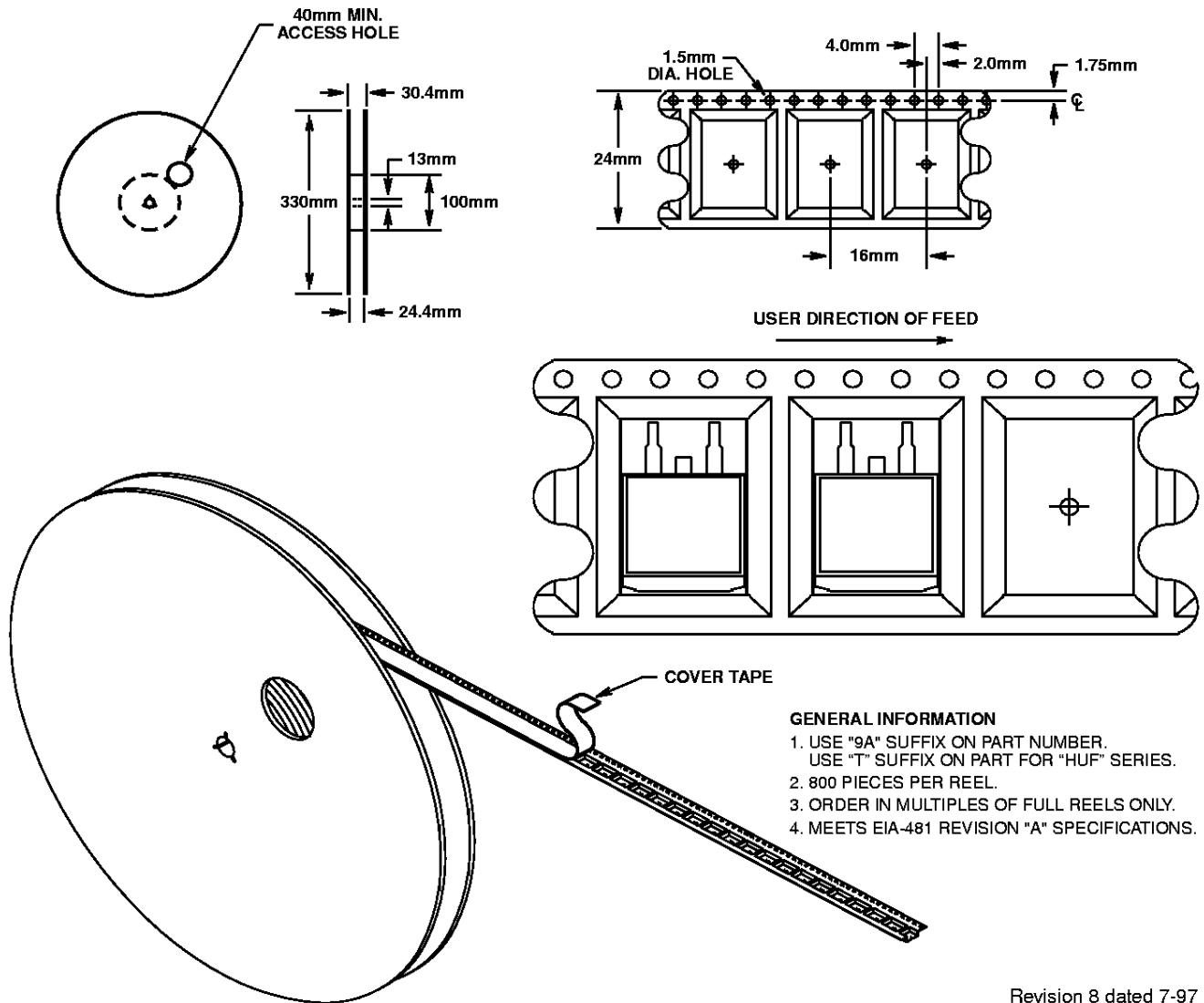
NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 8 dated 7-97.

HGTG12N60B3D, HGTP12N60B3D, HGT1S12N60B3D, HGT1S12N60B3DS

TO-263AB

24mm TAPE AND REEL



- GENERAL INFORMATION**
1. USE "9A" SUFFIX ON PART NUMBER.
USE "T" SUFFIX ON PART FOR "HUF" SERIES.
 2. 800 PIECES PER REEL.
 3. ORDER IN MULTIPLES OF FULL REELS ONLY.
 4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 8 dated 7-97

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For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA
 Harris Semiconductor
 P. O. Box 883, Mail Stop 53-210
 Melbourne, FL 32902
 TEL: 1-800-442-7747
 (407) 729-4984
 FAX: (407) 729-5321

EUROPE
 Harris Semiconductor
 Mercure Center
 100, Rue de la Fusee
 1130 Brussels, Belgium
 TEL: (32) 2.724.2111
 FAX: (32) 2.724.22.05

ASIA
 Harris Semiconductor PTE Ltd.
 No. 1 Tannery Road
 Cencon 1, #09-01
 Singapore 1334
 TEL: (65) 748-4200
 FAX: (65) 748-0400

