

# MC14069UB

## Hex Inverter

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

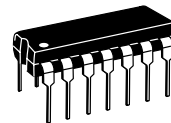
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



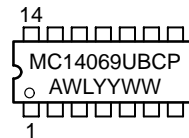
ON Semiconductor™

<http://onsemi.com>

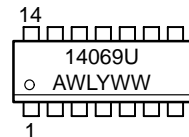
### MARKING DIAGRAMS



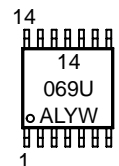
PDIP-14  
P SUFFIX  
CASE 646



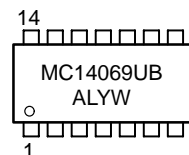
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



EIAJ SO-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14069UBCP	PDIP-14	2000/Box
MC14069UBD	SOIC-14	2750/Box
MC14069UBDR2	SOIC-14	2500/Tape & Reel
MC14069UBDT	TSSOP-14	96/Rail
MC14069UBDTEL	TSSOP-14	2000/Tape & Reel
MC14069UBDTR2	TSSOP-14	2500/Tape & Reel
MC14069UBF	EIAJ SO-14	See Note 1.
MC14069UBFEL	EIAJ SO-14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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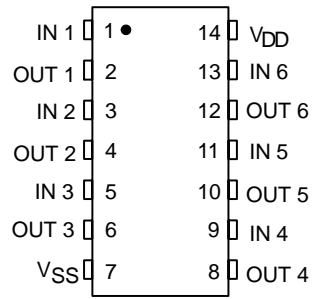


Figure 1. Pin Assignment

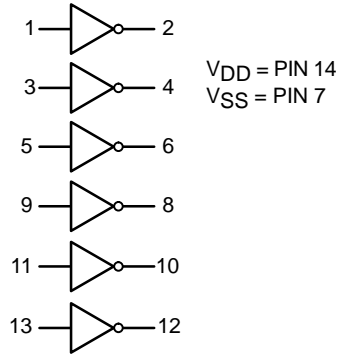
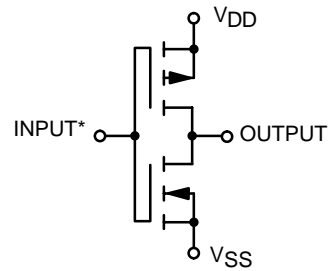


Figure 3. Logic Diagram



\*Double diode protection on all inputs not shown

Figure 2. Circuit Schematic

(1/6 of circuit shown)

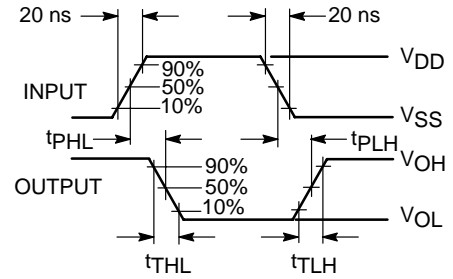
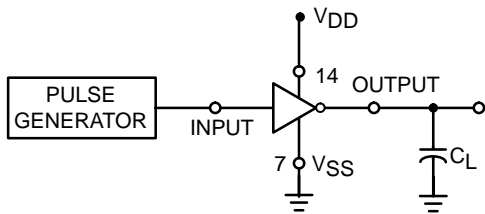


Figure 4. Switching Time Test Circuit and Waveforms

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub>  V <sub>in</sub> = 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Gate) (C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /6							μAdc
		10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /6							
		15	I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub> /6							
Output Rise and Fall Times (5.) (C <sub>L</sub> = 50 pF) t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.60 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.40 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	—	—	—	100	200	—	—	ns
		10	—	—	—	50	100	—	—	
		15	—	—	—	40	80	—	—	
		15	—	—	—	40	80	—	—	
Propagation Delay Times (5.) (C <sub>L</sub> = 50 pF) t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 20 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 22 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 17 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	—	—	—	65	125	—	—	ns
		10	—	—	—	40	75	—	—	
		15	—	—	—	30	55	—	—	
		15	—	—	—	30	55	—	—	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.