November 2001

FAIRCHILD
SEMICONDUCTOR®

Si6466DQ

20V N-Channel PowerTrench® MOSFET

General Description

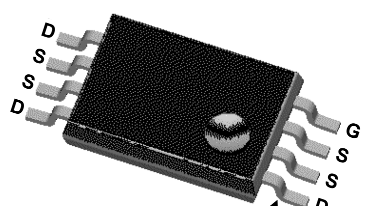
This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (2.5V to 12V).

Applications

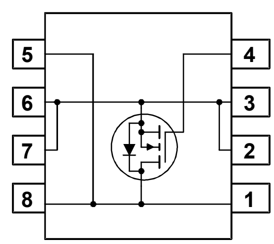
- Battery protection
- DC/DC conversion
- Power management
- Load switch

Features

- 7.8 A, 20 V $R_{DS(ON)}$ = 15 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 22 mΩ @ V_{GS} = 2.5 V
- Extended V_{GSS} range (±12V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



TSSOP-8



Absolute Maximum Ratings
T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1)	7.8	A
	– Pulsed		30	
P_D	Power Dissipation	(Note 1a)	1.4	W
		(Note 1b)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	87	°C/W
		(Note 1b)	114	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6466	Si6466DQ	13''	16mm	3000 units

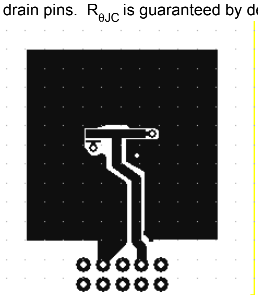
Electrical Characteristics

T_A = 25°C unless otherwise noted

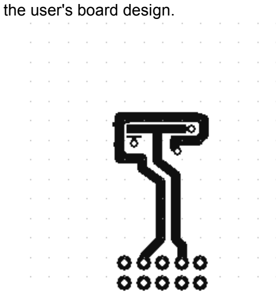
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J=55°C			25	
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–3.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 7.8 A V_{GS} = 2.5 V, I_D = 6.3 A		12 19	15 22	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.8 A		33		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1320		pF
C_{oss}	Output Capacitance			396		pF
C_{rss}	Reverse Transfer Capacitance			211		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn–On Rise Time			12	22	ns
$t_{d(off)}$	Turn–Off Delay Time			30	48	ns
t_f	Turn–Off Fall Time			11	20	ns
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.5 A, dI_F/dt = 100A/µs		23	80	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 7.8 A, V_{GS} = 4.5 V		14	20	nC
Q_{gs}	Gate–Source Charge			3		nC
Q_{gd}	Gate–Drain Charge			4.5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.7	1.1	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 87°C/W when mounted on a 1in^2 pad of 2 oz copper.



b) 114°C/W when mounted on a minimum pad of 2 oz copper.

c) Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

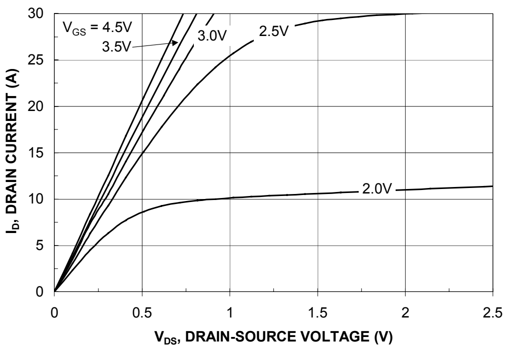


Figure 1. On-Region Characteristics.

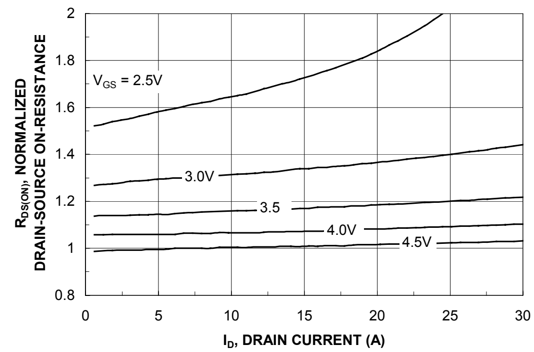


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

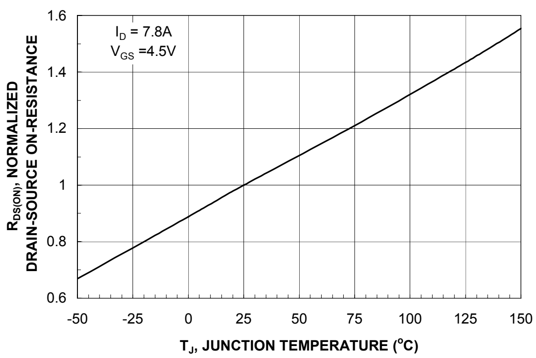


Figure 3. On-Resistance Variation with Temperature.

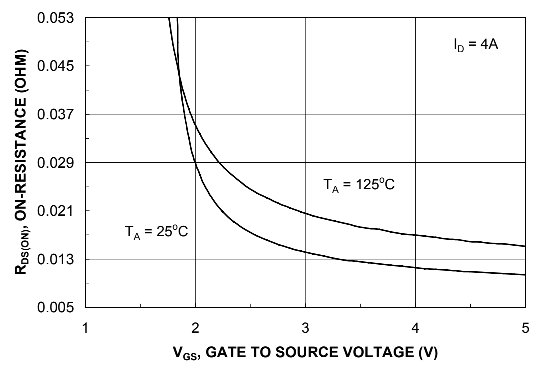


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

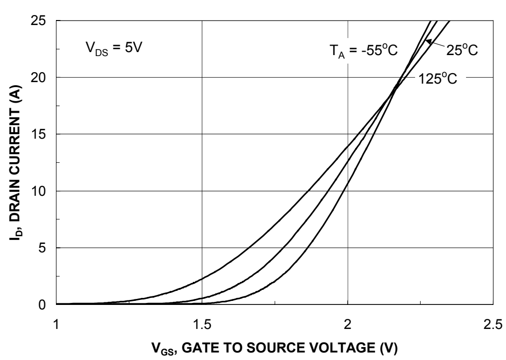


Figure 5. Transfer Characteristics.

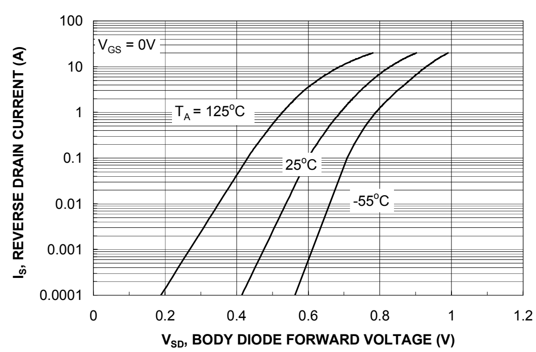


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

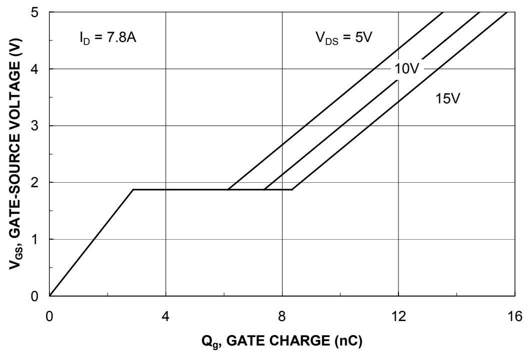


Figure 7. Gate Charge Characteristics.

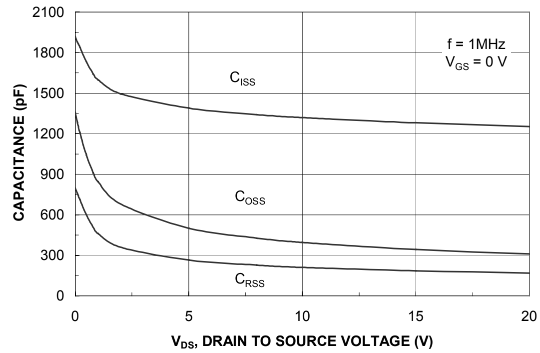


Figure 8. Capacitance Characteristics.

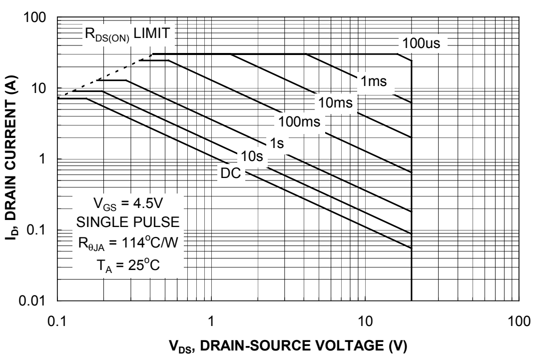


Figure 9. Maximum Safe Operating Area.

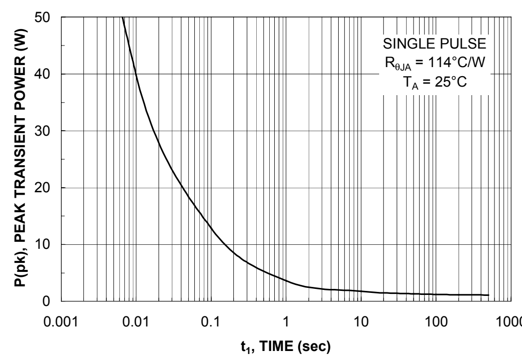


Figure 10. Single Pulse Maximum Power Dissipation.

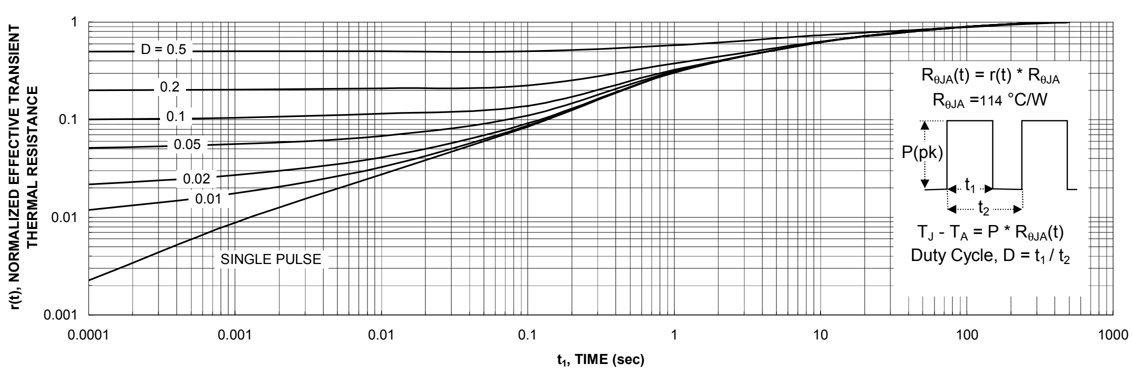


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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Definition of Terms

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General description

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Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Package marking	Packing method
SI6466DQ	Full Production	$0.81	TSSOP	8	$Y&3 6466	TAPE REEL

* 1,000 piece Budgetary Pricing

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