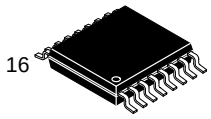
NCV75215

Ultrasonic Parking Distance Measurement ASSP

ON Semiconductor®

www.onsemi.com



TSSOP−16
CASE 948F

General Description

The NCV75215 ASSP is intended to operate with a piezoelectric ultrasonic transducer to provide time-of-flight measurement of an obstacle distance during vehicle parking. The high-sensitivity, low-noise operation allows detection from 0.25 m up to 4.5 m for a standard 75 mm pole. Actual minimum distance is determined by the length of reverberations. Under ideal conditions, with perfectly tuned and matched external circuitry, a minimum distance of 0.2 m is achievable. Actual detection range depends on a piezoelectric ultrasonic transducer and external analog parts.

The device drives the ultrasonic transducer with a programmable frequency via a transformer. The received echo is amplified and converted to a digital signal, filtered, detected and the magnitude is compared to a time-dependent threshold which is stored in an internal RAM. Distance to the obstacle is determined by the time measured from a transmission burst to echo recognition.

A bidirectional I/O Line is used to communicate with a master (ECU). The master issues I/O Line commands to the NCV75215 and data are reported back via the same line.

Features

- Measurement Distance Range from 0.25 m to 4.5 m (depends on External Parts)
- Acoustic Noise Monitoring
- Transducer Resonant Period Measurement
- Diagnosis of Transducer Performance
- Junction Temperature Monitoring and Thermal Shutdown
- Transducer Center Frequency Range from 35 to 90 kHz
- Direct and Indirect Measurement Modes
- EEPROM Memory for Configuration Setting and User Data
- Rx Gain Adjustable in 0.5 dB Steps in the Range from 50 to 110 dB
- Time-dependent Threshold Values for the Sensitivity Control
- Dynamic (Time-dependent) Gain Control
- Tx Current Range Adjustable from 50 mA to 350 mA
- Programmable Ultrasonic Burst Length
- On-chip Bidirectional I/O Line
- Small TSSOP16 Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- These are Pb-free Devices

Typical Applications

- Automotive Park Assist
- Ultrasonic Distance Measurements

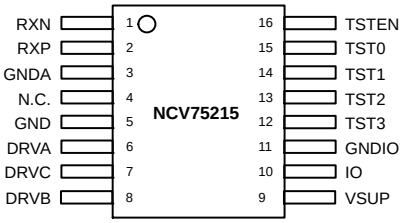
MARKING DIAGRAM

In accordance with:

US:
7620021 Mark Specifications − for ceramic, plastic and tape−automated bond packages

Europe:
16020 Standard Marking Specification

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV75215DB001R2G*	TSSOP−16 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

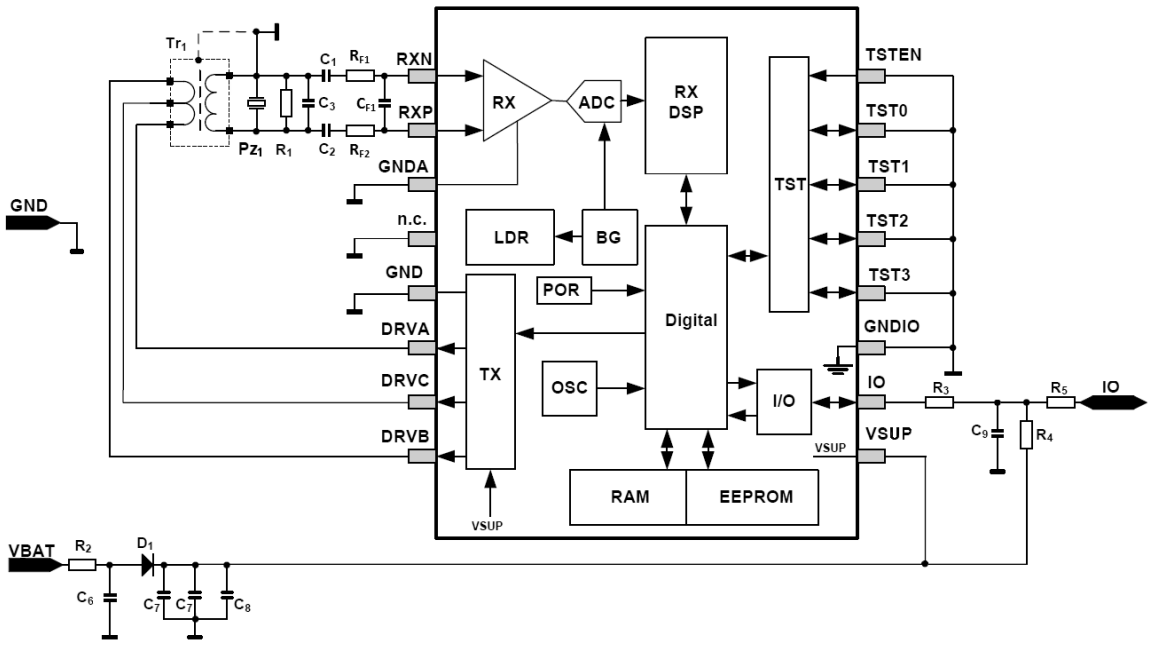


Figure 1. Application Schematic Diagram

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Name	Description	Typical Value	Units	Rating	Tolerance	Comment
R1	Resonator Damping	Optimal value	kΩ		5 %	Value depends on used transducer & transformer
R2	Battery Filter Resistor	100	Ω	Note ⇒	5 %	Power rating according to required EMC robustness
R3	I/O Line Protection	470	Ω	Note ⇒	5 %	It may be omitted but system ESD robustness is reduced Power rating according to required EMC robustness
R4	I/O Line Pull Up	10	kΩ	100 mW	5 %	Optional. It is not used if I/O Line internal pull-up resistor is enabled (see Config RAM item IO_PUP_ENA)
R5	I/O Line High Frequency Protection	47	Ω	Note ⇒	5 %	Optional It improves high frequency EMC robustness Power rating according to required EMC robustness
RF1 RF2	Input EMC Filter Resistor (Note 1)	100	Ω	Note ⇒	5 %	Optional It improves high frequency EMC robustness Power rating according to required EMC robustness
C1	Receiver Input Coupling	680	pF	100 V	10 %	
C2	Receiver Input Coupling	680	pF	100 V	10 %	
C3	Serial and Parallel Resonances Matching	optimal value	pF	100 V	5 %	Value depends on used transducer & transformer
CF1	Input EMC Filter Capacitor (Note 1)	10	pF	50 V	10 %	Optional It improves high frequency EMC robustness
C6	Battery Filter Capacitor	100	nF	50 V	10 %	
C7	Tank Capacitor for Transmitting Current	22	μF	35 V	10 %	2x ceramic type capacitor

1. Some of RF1, RF2 and CF1 components may be omitted. Use them according to required EMC robustness.

Table 1. RECOMMENDED EXTERNAL COMPONENTS (continued)

Name	Description	Typical Value	Units	Rating	Tolerance	Comment
C8	VBAT HF Filter	100	nF	50 V	10 %	
C9	I/O Line Capacitor	330	pF	50 V	10 %	Standard I/O Line slope (60 μs) IO_SLP_FAST = 0
C9	I/O Line Capacitor	100	pF	50 V	10 %	Fast I/O Line slope (20 μs) IO_SLP_FAST = 1
Tr1	Push-pull Transformer	Transducer specific	mH	100V	5%	
PZ1	Ultrasonic Transducer	MA40MF14−1B MA55AF15−07NA MA48AF15−07N	kHz	100V	the lower the better	muRata series
D1	Reverse Polarity Protection	BAS321	−	50 V	−	

1. Some of RF1, RF2 and CF1 components may be omitted. Use them according to required EMC robustness.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Type	Description
1	RXN (Note 2)	Input	Analog Receiver Negative Input
2	RXP	Input	Analog Receiver Positive Input
3	GNDA	Ground	Analog Ground
4	n.c.	n.c.	Pin not connected
5	GND	Ground	TX Ground, Digital Ground
6	DRVA	Output	Driver Output A
7	DRVC	Output	Driver Output C (Center of winding)
8	DRVB	Output	Driver Output B
9	VSUP	Power Supply	Main Power Supply
10	IO	Input/Output	I/O Line Bidirectional Interface to Master ECU
11	GNDIO	Ground	I/O Line Ground
12	TST3	Input/Output	Test pin 3/Custom Diagnostic Interface
13	TST2	Input/Output	Test pin 2/Custom Diagnostic Interface
14	TST1	Input/Output	Test pin 1/Custom Diagnostic Interface
15	TST0	Input/Output	Test pin 0/Custom Diagnostic Interface
16	TSTEN (Note 3)	Input	Manufacturer Test Mode Enable

2. Both receiver inputs are equal. Anyone of them can be used for signal input and the other for ground reference. But, using outer package pin for signal input may result in worse EMC robustness.
3. TSTEN pin has to be always grounded in customer application. There is no customer functionality.

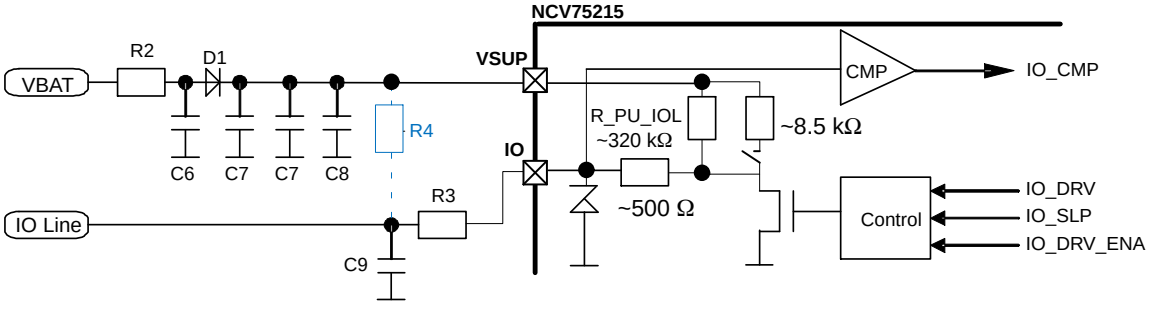


Figure 2. I/O Line Driver Structure and External Network

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Units
Supply Voltage Range VSUP (Note 4)	V_{SUP}	−0.3 to 40	V
I/O Line Voltage Range	V_{IO}	−5 to 40	V
I/O Line Voltage Range (T_A = 25°C)	$V_{IO,A}$	−15 to 40	V
I/O Line Voltage Range (t_{PULSE} < 1 second, T_A = 25°C)	$V_{IO,PA}$	−30 to 40	V
Transmitter DRVA, DRVB voltage	V_{DRV}	−0.3 to (2 × V_{SUP} + 0.3) or 40	V
Transmitter DRVC voltage	V_{DRV}	−0.3 to (V_{SUP} + 0.3) or 40	V
Receiver Input P, N Voltage	V_{RXP}, V_{RXN}	−0.3 to 0.3	V
Testmode Pin Voltage	V_{TST0} − V_{TST3}	0 to (V_{DD} + 0.3) or 3.6	V
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	TSTG	−40 to 125	°C
ESD Capability, Human Body Model (Note 5)	ESDHBM	2	kV
ESD Capability, Charge Device Model, All Pins (Note 5)	ESDCDM−O	500	V
ESD Capability, Charge Device Model, Corner Pins (Note 5)	ESDCDM−E	750	V
Latch-up Immunity at 25°C (Note 5)	LU25C	200	mA
Latch-up Immunity at 125°C (Note 5)	LU125C	100	mA
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note6)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch-up Current Maximum Rating: per JEDEC standard JESD78
6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 4. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Units
Thermal Characteristics, TSSOP16 (Note 7) Thermal Resistance, Junction-to-Air (Note 8)	$R_{\theta JA}$	135	°C/W

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz. copper thickness and FR4 PCB substrate.

Table 5. RECOMMENDED OPERATING RANGES

Symbol	Description	Min	Typ	Max	Units
VSUP	DC Supply Voltage	6	12	18	V
VIO	I/O Line Voltage	0		VSUP (Note 9)	V
T_A	Ambient Temperature under Bias	−40		85	°C
T_J	Junction Temperature under Bias	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

9. VSUP minimum voltage level might decrease the transmit burst ultrasonic power, it is external circuitry dependent. Transducer equivalent serial resistance is transformed on DRVA,B,C ASSP inputs and might be too high to satisfy both minimum VSUP and maximum TX current. In such a case, transmit driving current proportionally declines.

Table 6. ELECTRICAL CHARACTERISTICS

(V_{SUP} = 6 V to 18 V, T_A = −40°C to 85°C, external devices as in application circuit of Figure 1.)

Symbol	Description	Min	Typ	Max	Units
I_{VSUP}	Total VSUP Current Consumption (Normal Mode, No Transmission)			8	mA
I_{VSUP, LOW_PWR}	Total VSUP Current Consumption (Low Power Mode)			1	mA
t_{WAKE}	Wake-up Time from Low Power Mode to Normal Mode			1	ms
RECEIVER AMPLIFIER					
RX_{R_IN}	Receiver Input Resistance		87		kΩ
RX_{C_IN}	Receiver Input Capacitance		100		pF
RX_{GAIN}	Programmable Receiver Gain	50		110	dB
RX_{GSTEP}	Receiver Gain Step		0.5		dB
RX_{NSTEP}	Receiver Number of Gain Steps		127		
RX_{SENS}	Receiver Sensitivity at Maximum Gain	12			μV_{PP}
RX_{BW}	Receiver Bandwidth	35		90	kHz
TRANSDUCER DRIVER					
TX_{CURR}	Programmable Transmitter Current	50		350	mA
TX_{CSTEP}	Transmitter Current Step		4.76		mA
TX_{NSTEP}	Transmitter Number of Current Steps		63		
TX_{SPREC}	Transmitter Current Tolerance	−20		20	%
SUPPLY VOLTAGE AND ITS MONITORING					
VDD	Internal VDD Supply Voltage	3.15	3.3	3.5	V
VDD_{POR}	VDD Level for Power-on-Reset	2.7		3.1	V
$VSUP_{UV}$	VSUP Level for Power-on-Reset Release at Start-up, Under-voltage Threshold	5.1		5.7	V
$VSUP_{OV}$	VSUP Level for TX Driver Disable (to Protect Drivers), Over-voltage Threshold	18		20	V
INTERNAL OSCILLATOR					
F_{OSC}	Internal Oscillator Frequency	9.7	10	10.3	MHz
I/O LINE INTERFACE					
IO_{ILV}	Threshold Voltage for Digital Low	0.3	0.33	0.36	VSUP
IO_{IHV}	Threshold Voltage for Digital High	0.62	0.66	0.7	VSUP
IO_{OLV}	Output Voltage Low at I/O Pin (I_{OUT} = 1 mA, Internal Pull-up Activated, R4 Not Used)	0.4	0.65	1	V
$IO_{SR, STD}$	Output Slew Rate (Standard I/O Line Slope)	0.2	0.5	0.8	V/μs
$IO_{SR, FAST}$	Output Slew Rate (Fast I/O Line Slope)	1	1.7	2.5	V/μs
IO_{SCC}	I/O Short Circuit Current	10		50	mA
IO_{PU}	Fixed Internal Pull-up Resistor (R_PU_IOL)	200	320	450	kΩ
$IO_{PU, SEL}$	Selectable Internal Pull-up Resistor	6	8.5	11	kΩ
TEMPERATURE MEASUREMENT AND SHUTDOWN					
T_{MR}	Temperature Measurement Range	−60		150	°C
T_{MRES}	Temperature Measurement Resolution		1		°C
T_{A41}	Temperature Measurement Accuracy at T_J = 42°C	−7		7	°C
T_{A125}	Temperature Measurement Accuracy at T_J = 125°C	−10		10	°C
T_{A40-}	Temperature Measurement Accuracy at T_J = −40°C	−10		10	°C
T_{SD}	Thermal Shutdown	140		190	°C
EEPROM					
EE_{RT}	Data Retention Time	15			year
EE_{WE}	Write Endurance	100			cycles
EE_{RE}	Refresh and Read Endurance	1M			cycles

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DIGITAL FUNCTIONALITY DESCRIPTION

The digital circuitry consists of the following blocks:

- RST_GEN − based on POR (power-on reset) signals, generates internal reset of digital blocks
- CLK_GEN − generates CLK_IO_LINE and CLK_EEPROM from internal oscillator
- CFG_MEM − configuration parameters storage for the chip functionality (EEPROM shadow RAM)
- EEPROM_CTRL − EEPROM controller for accessing EEPROM memory
- I/O_LINE_CTRL − protocol and application layer for communication with I/O Line master (ECU) via I/O Line
- DSP_TOP − ultrasonic receiver and transmitter control, digital signal processing for ultrasonic receiver

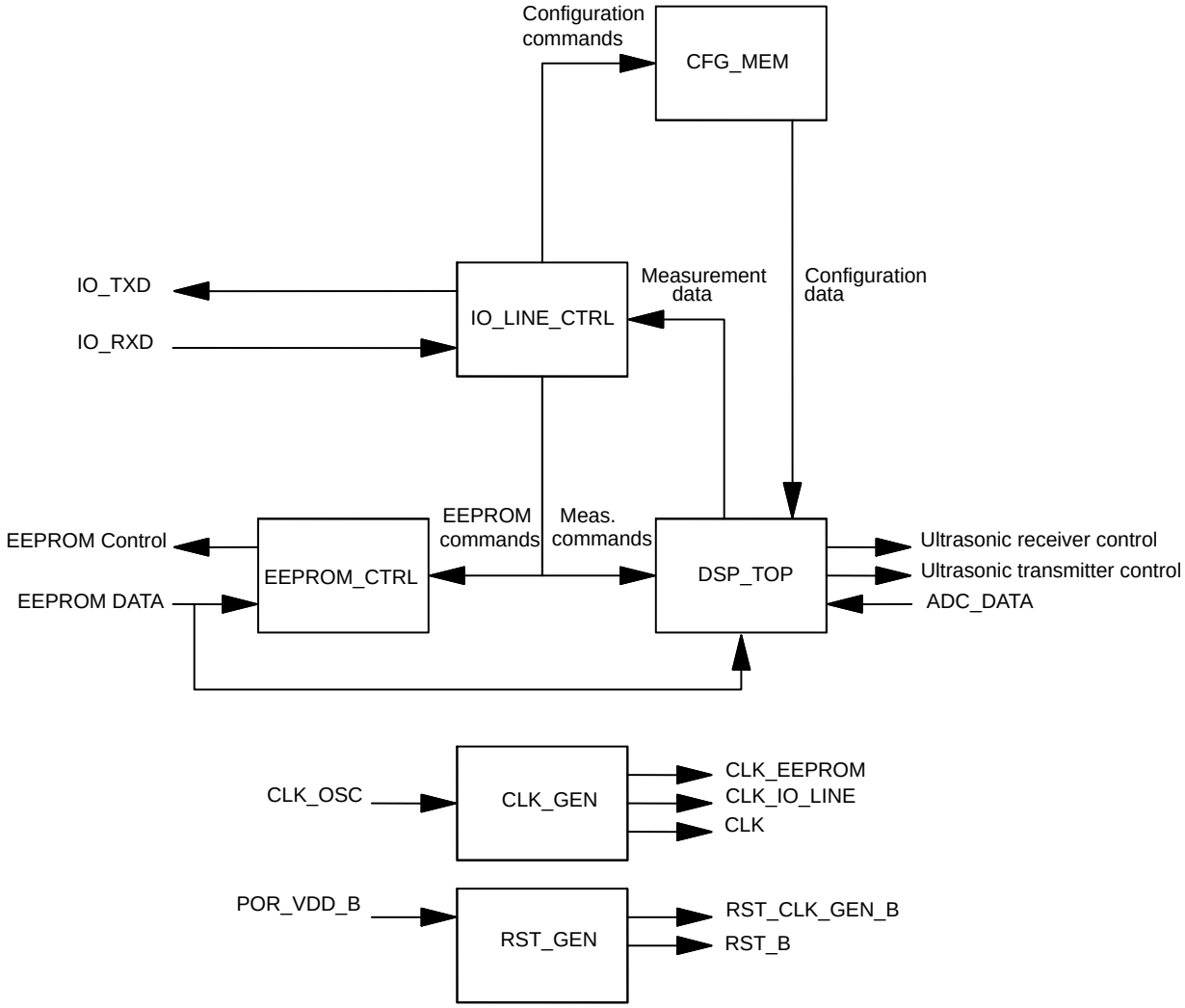


Figure 3. Digital Block Diagram

RST_GEN (Reset Generator)

It generates internal reset signals according to VSUP and VDD levels. In case of thermal shutdown all major blocks, such as RX, TX, and IO_LINE, go to power-down mode. This means that the chip doesn't communicate via I/O Line and its functionality is blocked. Functionality is restored when temperature falls back to a safe level.

CLK_GEN (Clock Generator)

This block generates the timing and internal clock signals based on an on-chip clock oscillator nominally running at 10 MHz (100 ns period).

DSP_TOP (Digital Signal Processing)

This block contains the core of the digital functionality of the NCV75215. The signal from ultrasonic transducer is amplified, converted to digital and fed to DSP_TOP. Then, it is digitally processed and compared to a time-dependent threshold. The echo is reported on I/O Line when the signal magnitude exceeds the threshold. Distance to the obstacle can be determined from the time of the echo arrival. This block also controls transmission and reception at the ultrasonic transducer frequency. A simplified internal diagram of DSP_TOP module is depicted in Figure 4.

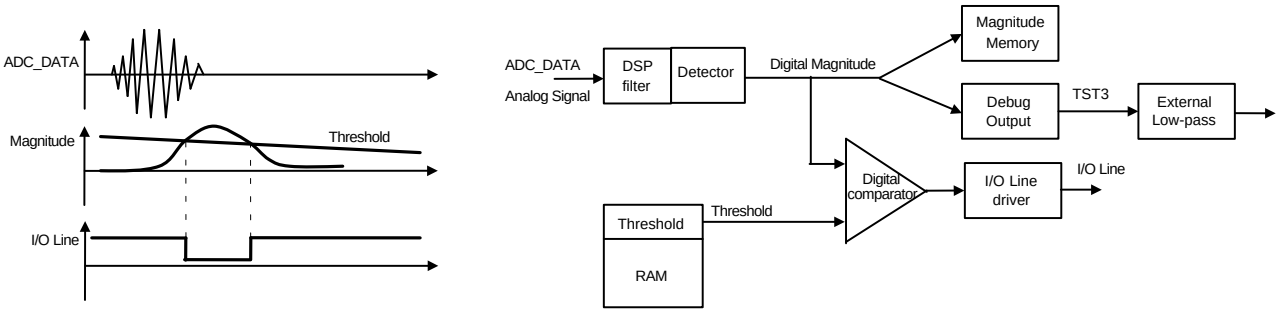


Figure 4. Block Diagram of DST TOP Module (Simplified)

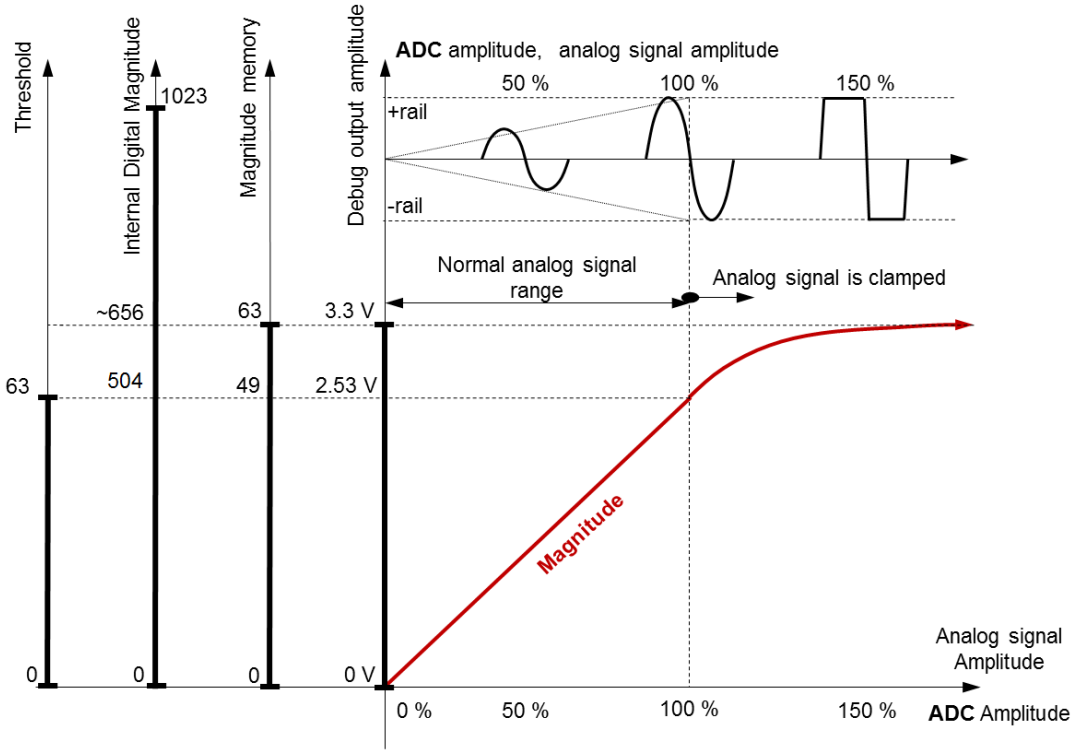


Figure 5. Understanding Internal Digital Magnitude, Thresholds and Debug Amplitude (the Processing is Fully Digital; Voltages Apply to PDM Debugging Outputs TST2 and TST3)

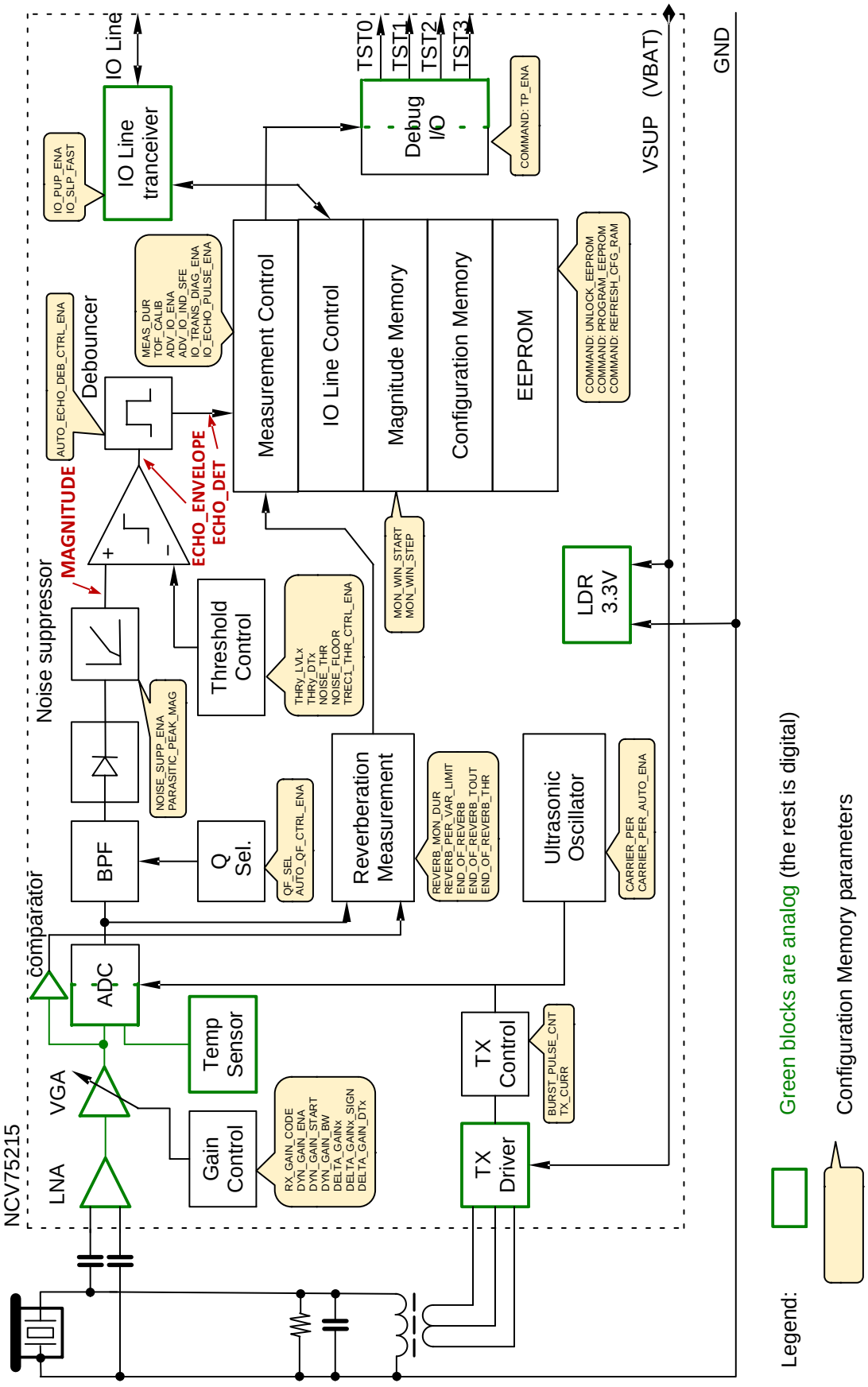


Figure 6. Block Diagram from Signal Processing Point of View

CFG_MEM (Configuration Memory)

Bit structure of configuration memory is described in Table 7. EEPROM Refresh is executed during reset and reset values of CFG_MEM cells are preloaded from EEPROM when available. For CFG_MEM locations not associated to the EEPROM, default value is preloaded after reset.

Data is transferred over I/O Line LSBit first and lowest sub-index first (in case of data arrays).

Table 7. STRUCTURE OF CONFIGURATION MEMORY

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
0	Measured Junction Temperature	TEMP [7:0]	8	Junction temperature code		Actual value	R only
1	Sensor Status (sub-index 0)	SENSOR_STATUS [7:0]	8	Refer to Encoding of Sensor Status Section		Actual value	R only
	Measured Reverberation Period (sub-index 1)	MEASURED_ REVERB_PER [10:0]	11	1−LSB ~ 25 ns		0 (Note 12)	R only
2a Accessible only when TX_RX_PER_ENA = 0	Carrier TX / RX Period	CARRIER_PER [10:0]	11	1−LSB ~ 25 ns Transmission & Reverberation: TX_CARRIER_PER = CARRIER_PER + 2 × DTX_PER Reception: RX_CARRIER_PER = CARRIER_PER + 2 × DRX_PER Valid range: <30 kHz, 95 kHz>	Yes		R/W
2b Accessible only when TX_RX_PER_ENA = 1	Delta TX Period (sub-index 0)	DTX_PER [7:0]	8	1−LSB ~ 50 ns Two's complement signed number Range: <−6.4 μs, 6.35 μs> See CARRIER_PER for explanation		0	R/W
	Delta Rx Period (sub-index 1)	DRX_PER [7:0]	8	The same coding as DTX_PER See CARRIER_PER for explanation		0	R/W
3	TX Burst Pulse Count	BURST_PULSE_ CNT [4:0]	5	Number of TX pulses (0...31) 0: TX driver is not activated 1: 1 × TX pulse … 31: 31 × TX pulses		16	R/W
4	Measurement Duration	MEAS_DUR [3:0]	4	0 – T_{SNDx} and T_{RECx} I/O Line commands disabled (default) 1 – 6 ms, 2 – 12 ms 3 – 18 ms, 4 – 24 ms 5 – 30 ms, 6 – 36 ms 7 – 42 ms, 8 – 48 ms 9 – 54 ms, 10 – 60 ms other values – 60 ms		0	R/W
5	THR1	THR1_LVL0 [5:0] / DT0 [3:0] … THR1_LVL11 / DT11	120	Thresholds – THR1 table See section THRESHOLDS		THR1_ LVLx = 32 DTx = 0	R/W
6	THR2	THR2_LVL0 [5:0] / DT0 [3:0] … THR2_LVL11 / DT11	120	Thresholds – THR2 table See section THRESHOLDS		THR2_ LVLx = 32 DTx = 0	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
7	Static RX Gain Code (sub-index 0)	RX_GAIN_CODE [6:0]	7	RX Gain Code 1−LSB ~ 0.476 dB	Yes		R/W
	Dynamic Gain Control Enable (sub-index 1)	DYN_GAIN_ENA	1	Enables / disables dynamic gain	Yes		R/W
	Noise Threshold (sub-index 2)	NOISE_THR [5:0]	6	Threshold applied during noise monitoring		32	R/W
	Noise Floor (sub-index 3)	NOISE_FLOOR [5:0]	6	All thresholds below NOISE_FLOOR[5:0] are clamped to NOISE_FLOOR[5:0]. Signal below NOISE_FLOOR[5:0] is considered as noise. The same coding as thresholds.		4	R/W
8	Dynamic Gain – Delta Gain #0 (sub-index 0)	DELTA_GAIN0 [6:0]	7	See DYNAMIC GAIN section. Range 0…127		0	R/W
	Dynamic Gain – Delta Gain Sign #0 (sub-index 1)	DELTA_GAIN0_SIGN	1	See DYNAMIC GAIN section. 0…positive, 1…negative		0	R/W
	Dynamic Gain – Delta Gain #1 (sub-index 2)	DELTA_GAIN1 [6:0]	7	See DYNAMIC GAIN section. Range 0…127		0	R/W
	Dynamic Gain – Delta Gain Sign #1 (sub-index 3)	DELTA_GAIN1_SIGN	1	See DYNAMIC GAIN section. 0…positive, 1…negative		0	R/W
	Dynamic Gain – Delta Gain #2 (sub-index 4)	DELTA_GAIN2 [6:0]	7	See DYNAMIC GAIN section. Range 0…127		0	R/W
	Dynamic Gain – Delta Gain Sign #2 (sub-index 5)	DELTA_GAIN2_SIGN	1	See DYNAMIC GAIN section. 0…positive, 1…negative		0	R/W
	Dynamic Gain – Delta Gain #3 (sub-index 6)	DELTA_GAIN3 [6:0]	7	See DYNAMIC GAIN section. Range 0…127		0	R/W
	Dynamic Gain – Delta Gain Sign #3 (sub-index 7)	DELTA_GAIN3_SIGN	1	See DYNAMIC GAIN section. 0…positive, 1…negative		0	R/W
	Dynamic Gain – Delta Gain #4 (sub-index 8)	DELTA_GAIN4 [6:0]	7	See DYNAMIC GAIN section. Range 0…127		0	R/W
	Dynamic Gain – Delta Gain Sign #4 (sub-index 9)	DELTA_GAIN4_SIGN	1	See DYNAMIC GAIN section. 0…positive, 1…negative		0	R/W
	Dynamic Gain – Delta Time Code #0 (sub-index 10)	DELTA_GAIN_DT0 [3:0]	4	See DYNAMIC GAIN section.		0	R/W
	Dynamic Gain – Delta Time Code #1 (sub-index 11)	DELTA_GAIN_DT1 [3:0]	4	See DYNAMIC GAIN section.		0	R/W
	Dynamic Gain – Delta Time Code #2 (sub-index 12)	DELTA_GAIN_DT2 [3:0]	4	See DYNAMIC GAIN section.		0	R/W
	Dynamic Gain – Delta Time Code #3 (sub-index 13)	DELTA_GAIN_DT3 [3:0]	4	See DYNAMIC GAIN section.		0	R/W
	Dynamic Gain – Delta Time Code #4 (sub-index 14)	DELTA_GAIN_DT4 [3:0]	4	See DYNAMIC GAIN section.		0	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
8	Dynamic Gain Control Start (sub-index 15)	DYN_GAIN_START [3:0]	4	DYN_GAIN_START × 204.8 μs		0	R/W
	Dynamic Gain – Filter BW (sub-index 16)	DYN_GAIN_BW [1:0]	2	See DYNAMIC GAIN section.		0	R/W
9	Generic User Data	USER_DATA [119:0]	120	120 bits of user data. User can select any structure. The chip doesn't internally use this data.	Yes		R/W
10	Reverberation / Decay Monitoring Window Duration (sub-index 0)	REVERB_MON_DUR [7:0]	8	1−LSB ~ 25.6 μs	Yes		R/W
	Current Adjustment (sub-index 1)	TX_CURR [5:0]	6	Default value is pre-loaded after POR.	Yes		R/W
	Reverberation Period Variation Limit (sub-index 2)	REVERB_PER_ VAR_LIMIT [1:0]	2	0 – 2.34 % 1 – 5.4 % 2 – 8.2 % 3 – 12.5 %	Yes		R/W
	Monitoring Window Start (sub-index 3)	MON_WIN_START [11:0]	12	Start time of echo magnitude logging into measurement memory 1−LSB ~ 25.6 μs		0	R/W
	Monitoring Window Step (sub-index 4)	MON_WIN_STEP [1:0]	2	Magnitude sampling period 0: 25.6 μs 1: 51.2 μs 2: 102.4 μs 3: 204.8 μs		1	R/W
	Automatic Carrier Period Control (sub-index 5)	CARRIER_PER_ AUTO_ENA	1	When 1: CARRIER_PER is used as carrier period for 1st ultrasonic measurement only resp. each time CARRIER_PER is updated. Following measurements will drive TX with measured MEASURED_REVERB_PER automatically only if difference between CARRIER_PER and measured reverberation period is less than REVERB_PER_VAR_LIMIT otherwise CARRIER_PER is used. In case of indirect measurement the CARRIER_PER will be exclusively used for echo reception. When 0: TX_CARRIER_PER resp. RX_CARRIER_PER is used.	Yes		R/W
	Noise Suppression Enable (sub-index 6)	NOISE_SUPP_ENA	1	Echo magnitude is suppressed if it is below noise background level	Yes		R/W
10	ToF Calibration (sub-index 7)	TOF_CALIB [5:0]	6	The time is subtracted from measured ToF prior storing it into the measurement result registers. It needs to be adjusted for selected Q factor. 1−LSB ~ 25.6 μs	Yes		R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
	Reverberation Debounce Time (sub-index 8)	END_OF_REVERB [1:0]	2	Debounce time is improving robustness towards chattering phenomena 0: 60 μs 1: 100 μs 2: 140 μs 3: 180 μs		1	R/W
	DSP Filter Q Factor Selection (sub-index 9)	QF_SEL [1:0]	2	0: Q = 5 1: Q = 10 2: Q = 20 3: Q = depending on number of TX pulses **TX pulses** **Q** 0…11 5 12…23 10 24…31 20		1	R/W
	DSP Filter Auto Q Factor Control Enable (sub-index 10)	AUTO_QF_CTRL_ ENA	1	0: Fixed Q factor according to QF_SEL [1:0] 1: Q is automatically switched at 14.8 ms after start of measurement **QF_SEL** **Q start** **Q after 14.8 ms** 0 5 10 1 5 20 2 10 20 3 5 Depends on TX pulses		0	R/W
	Automatic Echo Debounce Time Control Enable (sub-index 11)	AUTO_ECHO_DEB_ CTRL_ENA	1	0: Fixed 60 μs 1: Fixed 60 μs is automatically switched to 200 μs at 14.8 ms after start of measurement		0	R/W
	Internal I/O Line Pull-up Enable (sub-index 12)	IO_PUP_ENA	1	0: Internal I/O Line pull-up disabled 1: Internal I/O Line pull-up enabled	Yes		R/W
	I/O Line Slope Control (sub-index 13)	IO_SLP_FAST	1	0: Standard I/O Line slope (60 μs) 1: Fast I/O Line slope (20 μs)	Yes		R/W
	Advance I/O Line Protocol Enable (sub-index 14)	ADV_IO_ENA	1	0: Standard I/O Line protocols 1: Advanced I/O Line protocol Please, see index 13 & 14 for more details.		0	R/W
	T_{REC1} Threshold Control Enable (sub-index 15)	TREC1_THR_CTRL_ ENA	1	0: T_{REC1} utilizes THR1 curve 1: T_{REC1} utilizes fixed threshold NOISE_THR and fixed static gain RX_GAIN_CODE. SENSOR_STATUS [0] (Acoustic Noise Flag) is ORed with SENSOR_STATUS[0] of following T_{SND1}/T_{SND2} resp. T_{REC2}.		0	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
10	End of Reverberation Time-out (sub-index 16)	END_OF_REVERB_ TOUT [5:0]	6	Time-out of end-of-reverberation. In presence of high noise, the signal magnitude at analog front-end may avoid proper detection of end-of-reverberation. Detection of end-of-reverberation is mandatory prior to start of echo detection. This function stops end-of-reverberation measurement by time-out. **Improper use may lead to fake echo detection (reverberation detected as echo).** 1−LSB ~ 51.2 μs It is measured from TX end, end-of-reverberation time-out = TX end + END_OF_REVERB_TOUT[5:0]× 51.2 μs SENSOR_STATUS[5] is set in case the reverberation time-out is detected.		39 (~2 ms)	R/W
	Advanced I/O Line Indirect Measurement Skip First Echo (sub-index 17)	ADV_IO_IND_SFE	1	0: ToF1 = 1st echo; ToF2 = 2nd echo 1: ToF1 = 2nd echo; ToF2 = 3rd echo (valid for advanced I/O Line indirect measurement mode only) Comment: In case of indirect measurement, 1st echo is echo from sensor performing direct measurement. This option is valid for indirect measurement only.		1	R/W
	I/O Line Transducer Diagnostic Reporting Enable (sub-index 18)	IO_TRANS_DIAG_ ENA	1	0: Reporting of transducer diagnostic at I/O Line disabled 1: Reporting of transducer diagnostic at I/O Line enabled Comment: Transducer diagnostic is always enabled when Advanced I/O Line protocol is enabled (ADV_IO_ENA = 1)		1	R/W
	End of Reverberation Threshold (sub-index 19)	END_OF_REVERB_ THR	1	0: 75% of full-scale 1: 50% of full-scale		0	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
10	I/O Line 99.2 μs Echo Duration Enabled (sub-index 20)	IO_ECHO_PULSE_ ENA	1	0: Disabled 1: Enabled, valid only when ADV_IO_ENA = 0. When enabled, echo is always reported by 99.2 μs pulse on I/O Line. Measurement is stopped If I/O Line is pulled low for at least 350 μs during active measurement. Once active measurement is stopped, I/O Line has to be released to idle state (high) for at least T_{DEB} time to re-enable the detection of next I/O Line command. In case of T_{SNDx}, I/O Line is driven low for 99.2 μs at the detected end of reverberations, then I/O Line is again driven low for 99.2 μs each time when valid echo is detected (this is identical with T_{RECx}). Min. time is 99.2 μs between two echoes in this mode. If distance between echoes is less than 99.2 μs just single echo is reported. Comment: This mode enables fully programmable measurement duration (by stopping of on-going measurement) while it is still transparently propagating detected echo (ToF) on I/O Line.		0	R/W
	Parasitic Echo Peak Magnitude to Suppress at the End of Reverberations (sub-index 21)	PARASITIC_PEAK_ MAG [1:0]	2	0: Parasitic echo peak suppression is disabled at the end of reverberations 1: Parasitic echo peak low suppression 2: Parasitic echo peak medium suppression 3: Parasitic echo peak high suppression		0	R/W
	Index 2 Format Selection (sub-index 22)	TX_RX_PER_ENA	1	0: Selects format 2a 1: Selects format 2b		0	R/W
	Index 14 Format Selection (sub-index 23)	WIDTH_PEAK_ENA	1	0: Selects format 14a 1: Selects format 14b		0	R/W
11	Super Read/Write Index	n.a. (Note 10)		READ: Sequential read of the following indexes in the following order: 2a, 7. RX_GAIN_CODE, 7. DYN_GAIN_ENA, 10 (items initialized from EEPROM only) WRITE: Sequential write to the following indexes in the following order: 2a, 3, 4, 7, 10		n.a.	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
12	Magnitude Data	MEAS_DATA0 [5:0] … MEAS_DATA59 [5:0]	360	Sampled echo magnitude. Echo magnitude logging is controlled by parameters MON_WIN_START and MON_WIN_STEP. MEAS_DATA0 = echo magnitude at time MON_WIN_START × 25.6 μs … MEAS_DATA59 = echo magnitude at time MON_WIN_START × 25.6 μs + 59 × LUT[MON_WIN_STEP]		n.a.	R only
13	Measurement Results – Short This index is only functional when ADV_IO_ENA = 1. Otherwise, there is no response for this index.	MEAS_RES_SHR_SENSOR_STATUS [7:0] (sub-index 0)	8	Refer to Encoding of Sensor Status Section		n.a.	R only
		MEAS_RES_SHR_TOF1 [9:0] (sub-index 1)	10	ToF1 – time of 1st echo 1−LSB ~ 51.2 μs ToF = floor (echo detection time) – (TOF_CALIB × 25.6 μs) Echo time − 1st (ToF1) rising edge of ECHO_DET signal after detected end of reverberation ToF1 = 0 in case the echo is not detected		0	R only
14a Accessible only when WIDTH_PEAK_ENA = 0	Measurement Results – Long This index is only functional when ADV_IO_ENA = 1. Otherwise, there is no response for this index.	MEAS_RES_LNG_SENSOR_STATUS [7:0] (sub-index 0)	8	Refer to Encoding of Sensor Status Section		n.a	R only
		MEAS_RES_LNG_TOF1 [9:0] (sub-index 1)	10	ToF1 – time of 1st echo 1−LSB ~ 51.2 μs See index 13. ToFx = 0 in case when any echo is not detected		0	R only
		MEAS_RES_LNG_TOF2 [9:0] (sub-index 2)	10	ToF2 – time of 2nd echo		0	R only

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
14b Accessible only when WIDTH_PEAK_ENA = 1	Measurement Results – Long This index is only functional when ADV_IO_ENA = 1. Otherwise, there is no response for this index.	MEAS_RES_LNG_ SENSOR_STATUS [7:0] (sub-index 0)	8	Refer to Encoding of Sensor Status Section		n.a	R only
		MEAS_RES_LNG_ TOF1 [9:0] (sub-index 1)	10	ToF1 – time of 1st echo 1−LSB ~ 51.2 μs See index 13. ToFx = 0 in case when any echo is not detected		0	R only
		MEAS_RES_LNG_ PEAK1 [5:0] (sub-index 2)	6	Maximal magnitude of 1st echo. The same encoding as echo magnitude in MEAS_DATA. In case of no echo, it is 0.		0	R only
		MEAS_RES_LNG_ WIDTH1 [5:0] (sub-index 3)	6	Width of 1st echo. 1−LSB ~ 12.8 μs In case of no echo, it is 0.		0	R only
15	Command Byte (Write) IC Revision ID (Read)	CMD[7:0] / IC_ID_xx[7:0]	8	See Data communication section. WRITE: CMD [7:0] … command byte READ: IC_ID_xx [7:4]: Full mask version Allowed range from 1 to15. IC_ID_xx [3:0]: Metal tune version Allowed range from 1 to15. Comment: 1st silicon version is IC_ID_xx = 0x11 hex		IC_ID_xx [7:0]	R/W

10. n.a. = not applicable
11. Configuration memory start-up values:

EEPROM Column Value in Table 1	Configuration Memory Item Start-up Value
Yes	The value is preloaded from EEPROM at start-up.
–	Default value is loaded at start-up or actual value is reported (read only items).

12. MEASURED_REVERB_PER values:

MEASURED_REVERB_PER Value	Value Meaning
0	The period not measured.
1	The period measurement failed because of low signal.
Others	Measured period.

ENCODING OF SENSOR_STATUS [7:0] REGISTER

SENSOR_STATUS [0] = Acoustic Noise Flag

Flag is set if an acoustic noise is above the noise threshold (NOISE_THR) in noise monitoring time window.

Flag is automatically cleared by any measurement.

SENSOR_STATUS [1] = VSUP Under-voltage or Over-voltage during TX

Flag is set if VSUP voltage is below under-voltage threshold or crosses the over-voltage threshold during TX. If the VSUP voltage is higher than over-voltage threshold before TX, then the flag is not set.

In any case when over-voltage was detected during TX, transmission is automatically stopped, but measurement normally continues.

Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [2] = TX Period Update Required

Flag is set if MEASURED_REVERB_PER is outside the range set by REVERB_PER_VAR_LIMIT and CARRIER_PER. Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

Flag is set after POR.

SENSOR_STATUS [3] = TX Period Update Direction

Flag indicates if MEASURED_REVERB_PER is greater than CARRIER_PER.

Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [4] = Unexpected Decay Time (decay time too short)

Flag is set if transducer decay time (reverberation) is shorter than REVERB_MON_DUR time.

Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [5] = End of Reverberation Time-out

Flag is set if transducer decay time is longer than end-of-reverberation time-out (TX end + END_OF_REVERB_TOUT * 51.2 μs). Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [6] = THS_ERROR Flag (Thermal Shutdown Error)

Flag is set if thermal shutdown is detected. Flag is automatically cleared by any measurement.

SENSOR_STATUS [7] = EEPROM Two-Bit Error *or* **EEPROM CRC Error** *or* **POR flag**

EEPROM Two-Bit Error Flag:

Flag is updated by refreshing Configuration RAM from EEPROM (at start-up or initialized by Refresh Configuration RAM from EEPROM command). Flag is set if two-bit error is detected at any EEPROM address (single-bit error is automatically corrected by ECC code).

EEPROM CRC Error Flag:

Flag is updated by refreshing Configuration RAM from EEPROM (at start-up or initialized by Refresh Configuration RAM from EEPROM command). EEPROM data (ECC bits not included) CRC code is automatically calculated and stored into EEPROM as a part of Program EEPROM process. CRC stored in EEPROM is compared with CRC calculated during Refresh Configuration RAM from EEPROM process. Flag is set if stored and calculated CRC don't match. CRC is also protected by ECC.

The CRC8−C2 polynomial is $x^8+x^5+x^3+x^2+x+1$. The initial value is "1111_1111" binary.

POR Flag:

The flag is set at POR and it is cleared-by-read.

NOTES: a.) If flags are updated in case of direct (transmit and receive) measurement only, they are kept unchanged in case of indirect (receive only) measurement.

b.) Clear-by-read flags are cleared by reading of Configuration RAM index 1.

CONFIGURATION MEMORY DETAILED DATA STRUCTURES

Table 8. INDEX 0 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	TEMPERATURE_CODE [0]
	…	…
	7	TEMPERATURE_CODE [7]

Table 9. INDEX 1 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	…	…
	7	SENSOR_STATUS [7]
1	8	MEASURED_REVERB_PER [0]
	…	…
	15	MEASURED_REVERB_PER [7]
2	16	MEASURED_REVERB_PER [8]
	17	MEASURED_REVERB_PER [9]
	18	MEASURED_REVERB_PER [10]

Table 10. INDEX 2A DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	CARRIER_PER [0]
	…	…
	7	CARRIER_PER [7]
1	8	CARRIER_PER [8]
	9	CARRIER_PER [9]
	10	CARRIER_PER [10]

Table 11. INDEX 2B DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	DTX_PER [0]
	…	…
	7	DTX_PER [7]
1	8	DRX_PER [0]
	…	…
	15	DRX_PER [7]

Table 12. INDEX 7 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	RX_GAIN_CODE [0]
	…	…
	6	RX_GAIN_CODE [6]
	7	DYN_GAIN_ENA

Table 12. INDEX 7 DATA STRUCTURE (Data are transferred LSBit first.) (continued)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
1	8	NOISE_THR [0]
	…	…
	13	NOISE_THR [5]
	14	NOISE_FLOOR [0]
	15	NOISE_FLOOR [1]
2	16	NOISE_FLOOR [2]
	17	NOISE_FLOOR [3]
	18	NOISE_FLOOR [4]
	19	NOISE_FLOOR [5]

Table 13. INDEX 10 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	REVERB_MON_DUR [0]
	…	…
	7	REVERB_MON_DUR [7]
1	8	TX_CURR [0]
	…	…
	13	TX_CURR [5]
	14	REVERB_PER_VAR_LIMIT [0]
	15	REVERB_PER_VAR_LIMIT [1]
2	16	MON_WIN_START [0]
	…	…
	23	MON_WIN_START [7]
3	24	MON_WIN_START [8]
	…	
	27	MON_WIN_START [11]
	28	MON_WIN_STEP [0]
	29	MON_WIN_STEP [1]
	30	CARRIER_PER_AUTO_ENA
	31	NOISE_SUPP_ENA
4	32	TOF_CALIB [0]
	…	…
	37	TOF_CALIB [5]
	38	END_OF_REVERB [0]
	39	END_OF_REVERB [1]
5	40	QF_SEL [0]
	41	QF_SEL [1]
	42	AUTO_QF_CTRL_ENA
	43	AUTO_ECHO_DEB_CTRL_ENA
	44	IO_PUP_ENA
	45	IO_SLP_FAST
	46	ADV_IO_ENA
	47	TREC1_THR_CTRL_ENA

Table 13. INDEX 10 DATA STRUCTURE (Data are transferred LSBit first.) (continued)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
6	48	END_OF_REVERB_TOUT [0]
	…	…
	53	END_OF_REVERB_TOUT [5]
	54	ADV_IO_IND_SFE
	55	IO_TRANS_DIAG_ENA
7	56	END_OF_REVERB_THR
	57	IO_ECHO_PULSE_ENA
	58	PARASITIC_PEAK_MAG [0]
	59	PARASITIC_PEAK_MAG [1]
	60	TX_RX_PER_ENA
	61	WIDTH_PEAK_ENA

Table 14. INDEX 12 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	MEAS_DATA0 [0]
	…	…
	5	MEAS_DATA0 [5]
	6	MEAS_DATA1 [0]
	7	MEAS_DATA1 [1]
1	8	MEAS_DATA1 [2]
	…	…
	11	MEAS_DATA1 [5]
	12	MEAS_DATA2 [0]
	…	…
	15	MEAS_DATA2 [3]
2	16	MEAS_DATA2 [4]
	17	MEAS_DATA2 [5]
	18	MEAS_DATA3 [0]
	…	…
	23	MEAS_DATA3 [5]
…	…	…
44	352	MEAS_DATA58 [4]
	353	MEAS_DATA58 [5]
	354	MEAS_DATA59 [0]
	…	…
	359	MEAS_DATA59 [5]

NOTES:

- The content of registers MEAS_DATA0..59 is undefined and lost if I/O Line short to VBAT/GND is detected during reading from configuration memory index 12.
- The registers are updated during measurement. They can be read as many times as required, but their content is lost when any index data write transfer is issued on I/O Line.

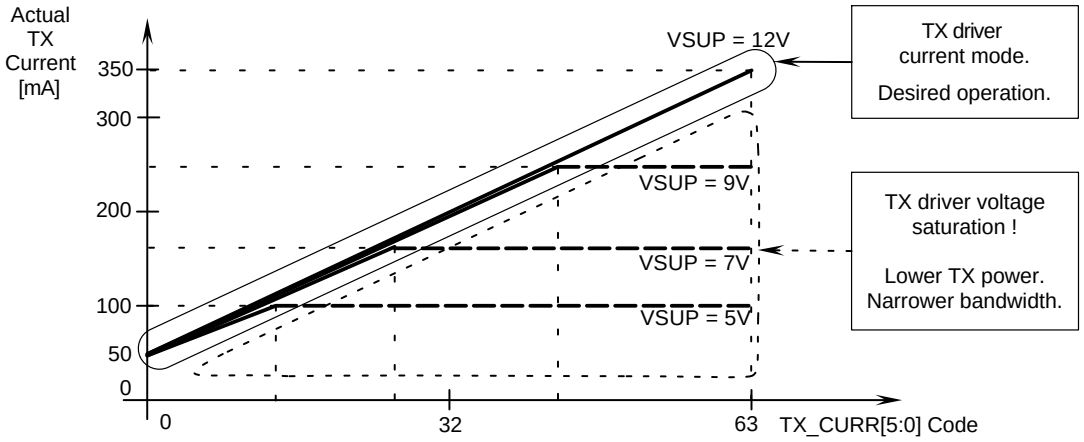


Figure 7. An EXAMPLE of TX Driver Current Characteristics

Figure 7 depicts an EXAMPLE of TX driver current characteristic. The characteristic doesn't depend on NCV75215 but it depends on utilized transformer and the piezo impedance transformed to primary winding.

Table 15. INDEX 13 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	…	…
	7	SENSOR_STATUS [7]
1	8	MEAS_RES_SHR_TOF1 [0]
	…	…
	15	MEAS_RES_SHR_TOF1 [7]
2	16	MEAS_RES_SHR_TOF1 [8]
	17	MEAS_RES_SHR_TOF1 [9]

Table 16. INDEX 14A DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	…	…
	7	SENSOR_STATUS [7]
1	8	MEAS_RES_LNG_TOF1 [0]
	…	…
	15	MEAS_RES_LNG_TOF1 [7]
2	16	MEAS_RES_LNG_TOF1 [8]
	17	MEAS_RES_LNG_TOF1 [9]
	18	MEAS_RES_LNG_TOF2 [0]
	..	…
	23	MEAS_RES_LNG_TOF2 [5]
3	24	MEAS_RES_LNG_TOF2 [6]
	...	…
	27	MEAS_RES_LNG_TOF2 [9]

Table 17. INDEX 14B DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	…	…
	7	SENSOR_STATUS [7]
1	8	MEAS_RES_LNG_TOF1 [0]
	…	…
	15	MEAS_RES_LNG_TOF1 [7]
2	16	MEAS_RES_LNG_TOF1 [8]
	17	MEAS_RES_LNG_TOF1 [9]
	18	MEAS_RES_LNG_PEAK1 [0]
	..	…
	23	MEAS_RES_LNG_PEAK1 [5]
3	24	MEAS_RES_LNG_WIDTH1 [0]
	...	…
	29	MEAS_RES_LNG_WIDTH1 [5]

TEMPERATURE MEASUREMENT

It is possible to monitor junction temperature by reading configuration memory index 0.

Table 18. JUNCTION TEMPERATURE CONVERSION

Junction Temperature	TEMP[7:0] − Config. Mem. Idx 0
−60	16
−40	36
−20	56
0	76
20	95
40	116
60	136
80	156
100	176
120	197
140	217
160	238
170	248

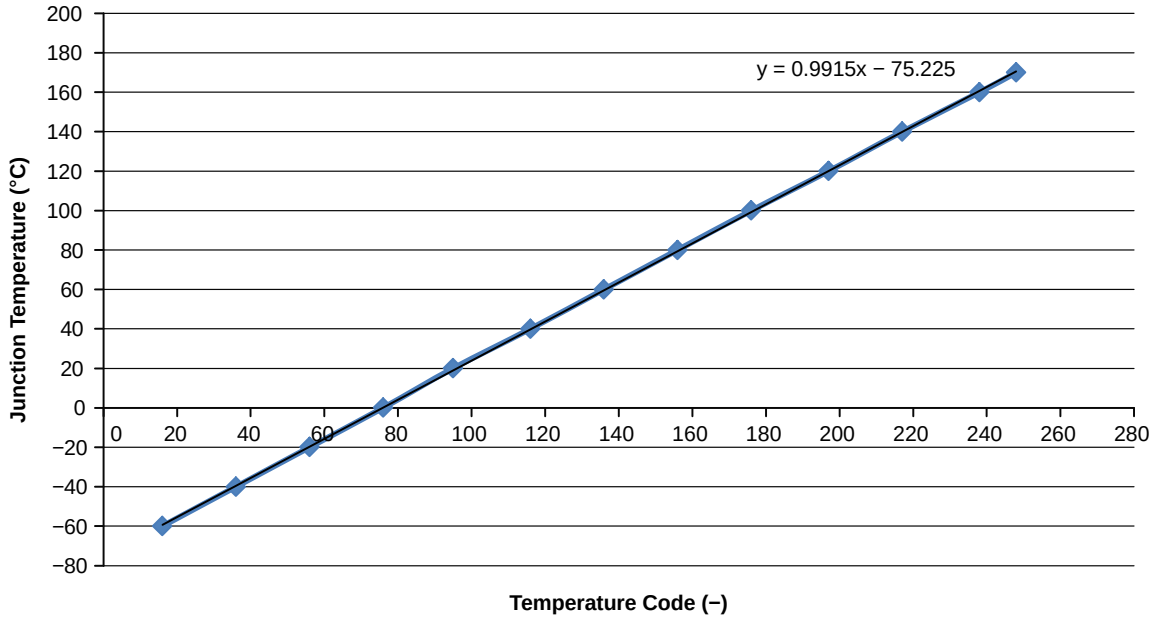


Figure 8. Junction Temperature Transfer Function

THRESHOLDS

DSP Filter Threshold (signal magnitude threshold) is controlled by values in 1 of 2 threshold Look-Up Tables (THR1 or THR2). The last threshold interval ends at 60ms (measured from the beginning of TX Ultrasonic transmission). Each threshold table consists of 12 data pairs. Each pair contains threshold level (6 bit) and delta time code (4 bit), which defines a time for linear interpolation to the particular threshold level. Threshold levels are interpreted using linear scale.

Table 19. THRESHOLD TABLE SELECTION

Command Pulse (Measurement Type)	Threshold Table Used
T_{SND1} or T_{REC1}	THR1
T_{SND2} or T_{REC2}	THR2

Table 20. THRESHOLD LEVELS THRx_LVLy[5:0]
(Note 13)

Value	Interpretation
0	Lowest threshold level
…	…
63 (0x3F)	Highest threshold level (equivalent of full ADC range signal)

Table 21. THRESHOLD DELTA TIME THRx_DTy[3:0]
(Note 13)

THRx_DTy Code	Delta Time [μs]	THRx_DTy Code	Delta Time [μs]
0	100	8	1600
1	200	9	2000
2	300	10	2400
3	400	11	3200
4	600	12	4000
5	800	13	5200
6	1000	14	6400
7	1200	15	8000

13. x stands for index 1 or 2
y stands for index from 0 to 11

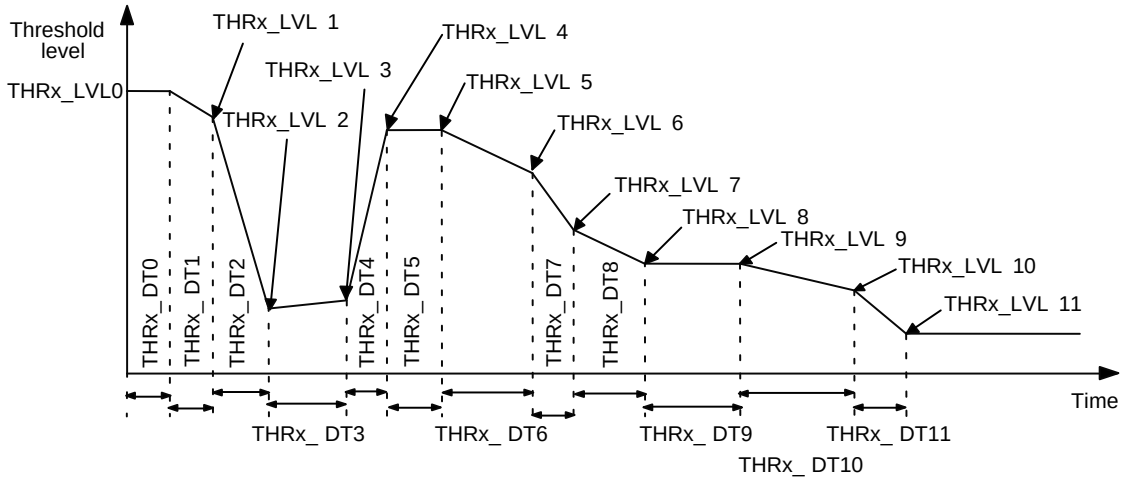


Figure 9. Threshold Curve Example

Threshold levels are piecewise approximated inside the thresholds intervals.

THR1_LVL11[5:0] resp. THR2_LVL11[5:0] threshold is applied until end of measurement if last delta time expires prior end of measurement.

NOISE_THR[5:0] is used during noise monitoring (the same threshold for both direct and indirect measurement).

Table 22. THRESHOLD TABLE DATA IN CONFIGURATION MEMORY (INDEX 5 AND 6)
(Data are transferred LSBit first)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	THRx_LVL0 [0]
	…	…
	5	THRx_LVL0 [5]
	6	THRx_LVL3 [0]
	7	THRx_LVL3 [1]
1	8	THRx_LVL1 [0]
	…	…
	13	THRx_LVL1 [5]
	14	THRx_LVL3 [2]
	15	THRx_LVL3 [3]
2	16	THRx_LVL2 [0]
	…	…
	21	THRx_LVL2 [5]
	22	THRx_LVL3 [4]
	23	THRx_LVL3 [5]
…	…	…
6	48	THRx_LVL8 [0]
	…	…
	53	THRx_LVL8 [5]
	54	THRx_LVL11 [0]
	55	THRx_LVL11 [1]
7	56	THRx_LVL9 [0]
	…	…
	61	THRx_LVL9 [5]
	62	THRx_LVL11 [2]
	63	THRx_LVL11 [3]
8	64	THRx_LVL10 [0]
	…	…
	69	THRx_LVL10 [5]
	70	THRx_LVL11 [4]
	71	THRx_LVL11 [5]
9	72	THRx_DT0 [0]
	…	…
	75	THRx_DT0 [3]
	76	THRx_DT1 [0]
	…	…
	79	THRx_DT1 [3]
…	…	…
14	112	THRx_DT10 [0]
	…	…
	115	THRx_DT10 [3]
	116	THRx_DT11 [0]
	…	…
	119	THRx_DT11 [3]

DYNAMIC GAIN

Dynamic gain curve principle is depicted in Figure 10. It is similar to threshold interpolation algorithm.

See Table 1 index 8 for dynamic gain parameters. Other details are depicted in Figure 10.

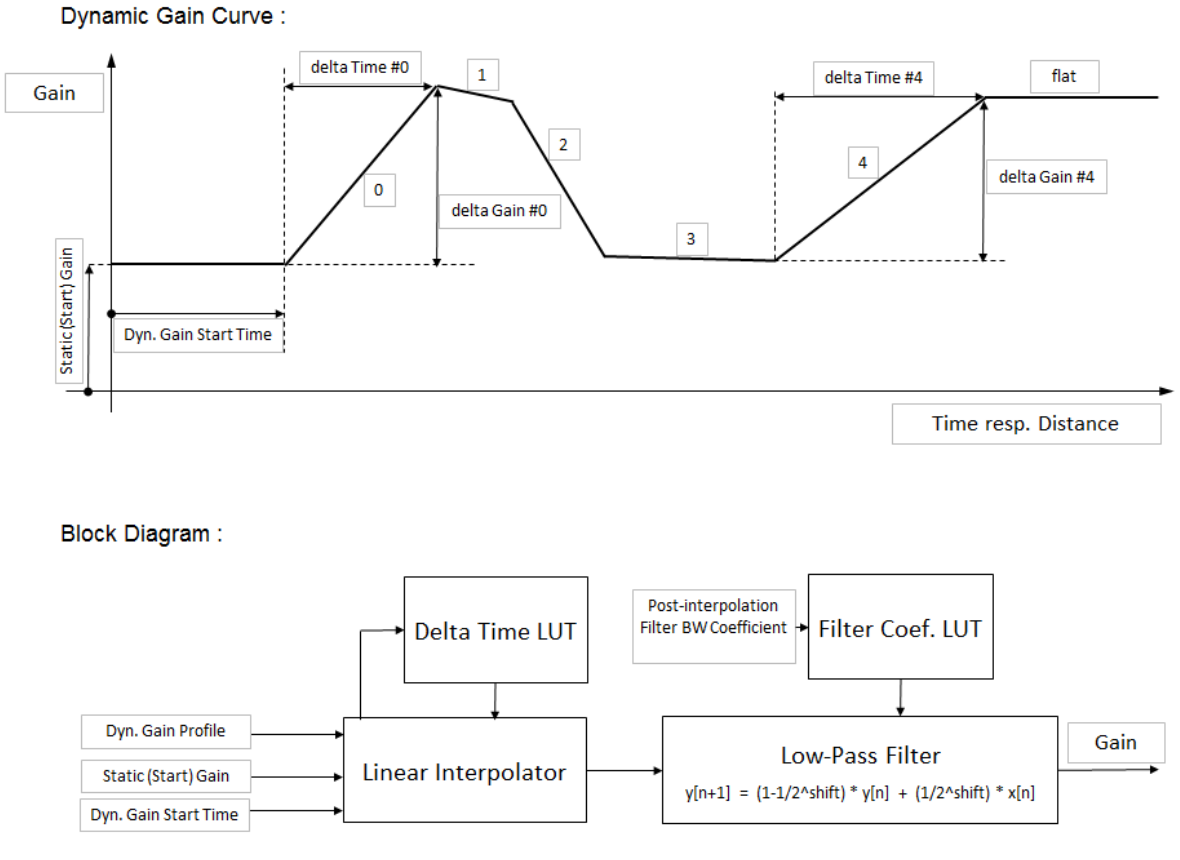


Figure 10. Dynamic Gain Principle

Table 23. DYNAMIC GAIN DELTA TIME DELTA_GAIN_DTz[3:0] CODE LUT (LOOK-UP TABLE)

DELTA_GAIN_DTz[3:0] Code	Delta Time [µs]	DELTA_GAIN_DTz[3:0] Code	Delta Time [µs]
0	102.4	8	3276.8
1	204.8	9	4505.6
2	409.6	10	5939.2
3	819.2	11	7987.2
4	1228.8	12	10035.2
5	1638.4	13	12697.6
6	2048	14	15974.4
7	2457.6	15	20070.4

14. z stands for index from 0 to 4

Dynamic gain curve is smoothed in low-pass filter which runs at 2.5 MHz. The filter formula is:

$$y_{n+1} = \left(1 - \frac{1}{2^s}\right) \times y_n + \frac{1}{2^s} \times x_n$$

where:

- y = output dynamic gain curve
- x = input signal from dynamic gain interpolator
- s = shift coefficient which defines filter bandwidth

Table 24. DYNAMIC GAIN FILTER COEFFICIENT DYN_GAIN_BW[1:0] CODE LUT (LOOK-UP TABLE):

DYN_GAIN_BW[1:0]	Filter Bandwidth	Coefficient “s”
0	No filter, pass through	0
1	Fast	8
2	Normal	9
3	Slow	10

Dynamic Gain Start Delay

Dynamic gain curve starts at begin of measurement cycle but it is delayed by the time:
“Dyn. Gain Start Time” = DYN_GAIN_START[3:0] * 204.8 μs

The range is from 0 μs to 3072 μs. Equivalent approximate distance is from 0 cm to 52.2 cm.

Table 25. DYNAMIC GAIN IN CONFIGURATION MEMORY (INDEX 8) (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Data Bit
0	0	DELTA_GAIN0 [0]
	…	…
	6	DELTA_GAIN0 [6]
	7	DELTA_GAIN0_SIGN
1	8	DELTA_GAIN1 [0]
	…	…
	14	DELTA_GAIN1 [6]
	15	DELTA_GAIN1_SIGN
…	…	…
4	32	DELTA_GAIN4 [0]
	…	…
	38	DELTA_GAIN4 [6]
	39	DELTA_GAIN4_SIGN
5	40	DELTA_GAIN_DT0 [0]
	…	…
	43	DELTA_GAIN_DT0 [3]
	44	DELTA_GAIN_DT1 [0]
	…	…
	47	DELTA_GAIN_DT1 [3]
6	48	DELTA_GAIN_DT2 [0]
	…	…
	51	DELTA_GAIN_DT2 [3]
	52	DELTA_GAIN_DT3 [0]
	…	…
	55	DELTA_GAIN_DT3 [3]
7	56	DELTA_GAIN_DT4 [0]
	…	…
	59	DELTA_GAIN_DT4 [3]
	60	DYN_GAIN_START [0]
	…	…
	63	DYN_GAIN_START [3]
8	64	DYN_GAIN_BW [0]
	65	DYN_GAIN_BW [1]

15. DELTA_GAINx_SIGN = 0 … positive DELTA_GAINx
16. DELTA_GAINx_SIGN = 1 … negative DELTA_GAINx

SUPER READ, SUPER WRITE

Super read data transfer is very useful at ultrasonic system startup. It enables to read all configuration memory items in one transaction which are initialized from EEPROM memory at power-on reset.

Then, the communication master (ECU) can use super write data transfer to initialize most of configuration memory items.

Table 26. INDEX 11 READ DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	CARRIER_PER [0]
	…	…
	7	CARRIER_PER [7]
1	8	CARRIER_PER [8]
	9	CARRIER_PER [9]
	10	CARRIER_PER [10]
	11	RX_GAIN_CODE [0]
	…	…
	15	RX_GAIN_CODE [4]
2	16	RX_GAIN_CODE [5]
	17	RX_GAIN_CODE [6]
	18	DYN_GAIN_ENA
	19	REVERB_MON_DUR [0]
	…	…
	23	REVERB_MON_DUR [4]
3	24	REVERB_MON_DUR [5]
	25	REVERB_MON_DUR [6]
	26	REVERB_MON_DUR [7]
	27	TX_CURR [0]
	…	…
	31	TX_CURR [4]
4	32	TX_CURR [5]
	33	REVERB_PER_VAR_LIMIT [0]
	34	REVERB_PER_VAR_LIMIT [1]
	35	CARRIER_PER_AUTO_ENA
	36	NOISE_SUPP_ENA
	37	TOF_CALIB [0]
	38	TOF_CALIB [1]
	39	TOF_CALIB [2]
5	40	TOF_CALIB [3]
	41	TOF_CALIB [4]
	42	TOF_CALIB [5]
	43	IO_PUP_ENA
	44	IO_SLP_FAST

Index 11 write data structure. Data are transferred LSBit first.

It is a sequential write to the following indexes in the following order: 2a, 3, 4, 7 and 10.

COMMAND BYTE

The chip is commanded to requested action by writing the particular *Command Code* to the command byte item in configuration memory at index 15. The Command Byte cannot be read back, it is write only access. Commands are protected by 8-bits coding, Hamming distance, checksum and number of message bits. Unwanted execution is practically impossible.

Table 27. COMAND BYTE

Command Code	Action
hex: 29 bin: 0010 1001	*Unlock EEPROM* – unlocks EEPROM for next I/O Line command. EEPROM has to be unlocked first to successfully execute Program EEPROM and Refresh Configuration RAM. EEPROM is automatically locked after the finishing of any following command.
hex: D6 bin: 1101 0110	*Program EEPROM* − store data in configuration memory marked “Yes” in EEPROM column in Table 1 into EEPROM
hex: 73 bin: 0111 0011	*Refresh Configuration RAM* from EEPROM (items stored in EEPROM only)
hex: Ax bin: 1010 xxxx	*Write TP_ENA bits* − TP_ENA[3:0] <= CommandByte[3:0]
hex: E7 bin: 1110 0111	*Unlock reading from Conf. RAM index <5…12>* – enables reading from Conf. RAM indexes <5…12>, otherwise there will be no response to I/O Line read command for Conf. RAM indexes <5…12>
hex: 18 bin: 0001 1000	*Lock reading from Conf. RAM index <5…12>* – disables reading from Conf. RAM indexes <5…12>
hex: 92 bin: 1001 0010	*Activate low power mode* − The chip enters low consumption mode and it only accepts IO Line command bytes “De-activate low power mode” and “SW reset”. Normal operation is not possible.
hex: 5 bin: 0000 0101	*De-activate low power mode* − Normal mode is re-entered from low power mode and normal operation is restored. See Electrical Characteristic section for required wake time (t_{wake}) to re-enter normal mode.
hex: 5A bin: 0101 1010	*SW reset* – Software activation of power-on reset (POR). This command effect is equal to POR.
others	no reaction

17. Reading from Conf. RAM indexes <5…12> is enabled after POR.

Store Data to EEPROM:
1st command *Unlock EEPROM*
2nd command *Program EEPROM*

Refresh Data from EEPROM:
1st command *Unlock EEPROM*
2nd command *Refresh Configuration RAM*

CHIP ID

The chip ID can be read from index 15. It is read only access.

Table 28. INDEX 15 DATA READ STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	IC_ID_MT [0]
	…	…
	3	IC_ID_MT [3]
	4	IC_ID_FM [0]
	…	…
	7	IC_ID_FM [3]

18. IC_ID_FM: Full mask silicon version. Completely modified silicon version.
19. IC_ID_MT: Metal tune silicon subversion. Small bugs can be fixed by different active components interconnection. Metal layers are modified but active silicon components remain the same.
20. The first silicon version is: IC_ID_FM = 1, IC_ID_MT = 1
21. The second silicon version is: IC_ID_FM = 2, IC_ID_MT = 1

CUSTOMER TEST OUTPUTS, TP_ENA

Custom diagnostic test (debugging) output/input (TST1...4) signals are selected by TP_ENA bits. TP_ENA bits are set via appropriate Command byte. DSP internal "analog" signals are PDM modulated. External low-pass filters are required. See table below for valid test signal combinations.

Table 29. CUSTOMER TEST OUTPUTS, TP_ENA

TP_ENA[3:0]	TST0	TST1	TST2	TST3
0000 (Default)	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ
0001	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	THRESHOLD[9:0] PDM2	ECHO_MAG[9:0] PDM1
0010	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	ECHO_ENVELOPE PDM2	ECHO_MAG[9:0] PDM1
0011	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	Not Defined	Not Defined
0100	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	ECHO_DET	ECHO_MAG[9:0] PDM1
0101	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	Not Defined	Not Defined
0110	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	GAIN[7:0] PDM2	ECHO_MAG[9:0] PDM1
0111	Hi−Z / 4 kΩ	Hi−Z / 4 kΩ	IO_RXD	IO_DRV (input)
1000	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	Hi−Z / 4kΩ	Hi−Z / 4kΩ
1001	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	THRESHOLD[9:0] PDM2	ECHO_MAG[9:0] PDM1
1010	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	ECHO_ENVELOPE PDM2	ECHO_MAG[9:0] PDM1
1011	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	Not Defined	Not Defined
1100	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	ECHO_DET	ECHO_MAG[9:0] PDM1
1101	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	Not Defined	Not Defined
1110	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	GAIN[7:0] PDM2	ECHO_MAG[9:0] PDM1
1111	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	IO_RXD	IO_DRV (Input)

22. Hi−Z / 4 kΩ = IO is not driven but pull down active
23. VGA_Gain = (analog(PDM2) / 20 mV) * (30 / 63) dB
24. Initial/POR value shall be 0 decimal ("0000" binary) – test outputs are disabled
25. GAIN[7:0] is effectively using half of the full-scale of PDM output
26. Threshold[9:0] is effectively using half of the full-scale of PDM output

Recommended External Low-pass Filter

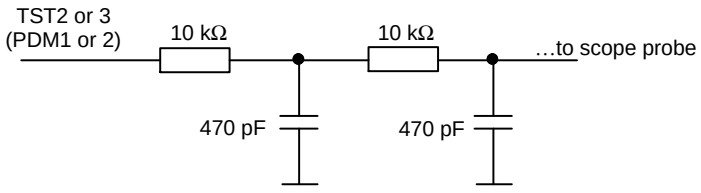


Figure 11. Recommended PDM External Low-pass Filter

EEPROM PROGRAMMING SEQUENCE

EEPROM programming operation is performed in 12 successive steps:

1. Power-on the device.
2. Read Configuration RAM index 1 to clear SENSOR_STATUS (SENSOR_STATUS[7] = HW ERROR).
3. Write data into Configuration RAM (EEPROM shadow registers).
4. Verify EEPRPOM shadow registers content by reading back Configuration RAM index 11 (super read) and index 9. If mismatch detected, go-to step 2.
5. Unlock EEPROM – Write Command Code 0x29hex into Configuration RAM index 15.
6. Program EEPROM − Write Command Code 0xD6hex into Configuration RAM index 15.
7. Wait 25 ms. It is needed to complete programming of the EEPROM memory.
8. Unlock EEPROM – Write Command Code 0x29hex into Configuration RAM index 15.
9. Refresh Configuration RAM − Write Command Code 0x73hex into Configuration RAM index 15.
10. Read Configuration RAM index 1 to get SENSOR_STATUS. SENSOR_STATUS[7] (EEPROM ERROR or HW_ERROR) should be 0. If SENSOR_STATUS[7] is 1, EEPROM failure occurred, then, go-to step 3.
11. Verify EEPRPOM shadow registers content by reading back Configuration RAM index 11 (super read) and index 9. If mismatch detected, go-to step 3.
12. Power-off the device.

EEPROM ERROR CORRECTION BLOCK

The error correction block utilizes SECDED coding for one bit error correction and 2 bits error detection. As data are split in words 16 bits long each, 5 extra bits are required for encoding ECC (Hamming code) and one extra bit for parity check (two bits error detection). The encoding bits are spread into the bit matrix accordingly to the Tab.2.

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Data	P0	P1	D0	P2	D1	D2	D3	P3	D4	D5	D6	D7	D8	D9	D10	P4	D11	D12	D13	D14	D15
P0	X		X		X		X		X		X		X		X		X		X		X
P1		X	X			X	X			X	X			X	X			X	X		
P2				X	X	X	X					X	X	X	X					X	X
P3								X	X	X	X	X	X	X	X						
P4																X	X	X	X	X	X

Figure 12. 16-bits Word SECDED Encoding

Error correction is based on the calculation of the parity bits. The parity bits are spread in such a way, that if the parity fails, the position of the error bit is defined directly by the position of the failing bits.

Example 1:

If the failure appears on bit 9 (D4), the parity of P0 and P3 will be wrong (column for bit 9, X's are for P0 and P3). Putting one on the wrong positions of the parity when writing parity word would be:

P4, P3, P2, P1, P0 = 01001 binary = 9 decimal.

Example 2:

Error is on parity bit P4 – the word is 10000 = bit 16 decimal (that is directly the parity bit P4).

If two bits error is detected, invalid data of the impacted address in the shadow registers will not be updated.

IO_LINE_CTRL (COMMAND PULSE, MEASUREMENT CONTROL, DATA COMMUNICATION)

I/O Line is a master-slave point-to-point communication link. If more than one chip is connected to master (ECU) unit, it creates **star topology**.

Every I/O Line communication starts with particular command pulse. Its length and meaning is in table below:

Table 30. IO_LINE COMMAND PULSE

Command Pulse	Min. Pulse Length [μs]*	Typ. Pulse Length [μs]	Max. Pulse Length [μs]*	Addressing	Description
T_{SND1}	328	400	472	−	TX+RX (direct measurement with THR1 table)
T_{REC2}	503	580	657	−	RX only (indirect measurement with THR2 table)
T_{REC1}	697	780	863	−	RX only (indirect measurement with THR1 table)
T_{SND2}	920	1010	1100	−	TX+RX (direct measurement with THR2 table)
T_{DATA}	1172	1270	1368	R/nW, xxxx	Data communication

*I/O Line command pulse, which is generated by ECU master, has to be always in range from minimal pulse length to maximal pulse length under any applicable condition (especially EMC disturbance, which may shift I/O Line edges by tens of microseconds). It is strongly recommended to generate command pulses as close as possible to typical pulse length to keep maximal command recognition margin.

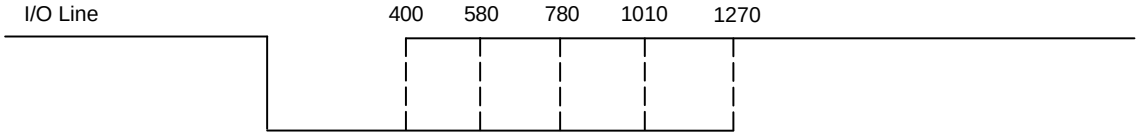


Figure 13. I/O Line Command Pulses

IO LINE SHORT TO VBAT/GND DETECTION

If the chip detects that I/O Line logical value (dominant or recessive level) differs from the value driven by the chip for time ≥ 350 μs then I/O Line short circuit condition is detected. In this case, the chip immediately stops driving the I/O Line.

On-going measurement respective I/O Line data communication is immediately interrupted. I/O Line has to be in recessive level for at least T_{DEB} time to accept the next I/O Line command.

MEASUREMENT CONTROL

The measurement can be started by T_{SND1}, T_{REC2}, T_{REC1} or T_{SND2} command pulse. Measured ultrasonic echoes can be reported on I/O Line in 3 different modes. Modes are selected in Configuration Memory. The figure below depicts these modes.

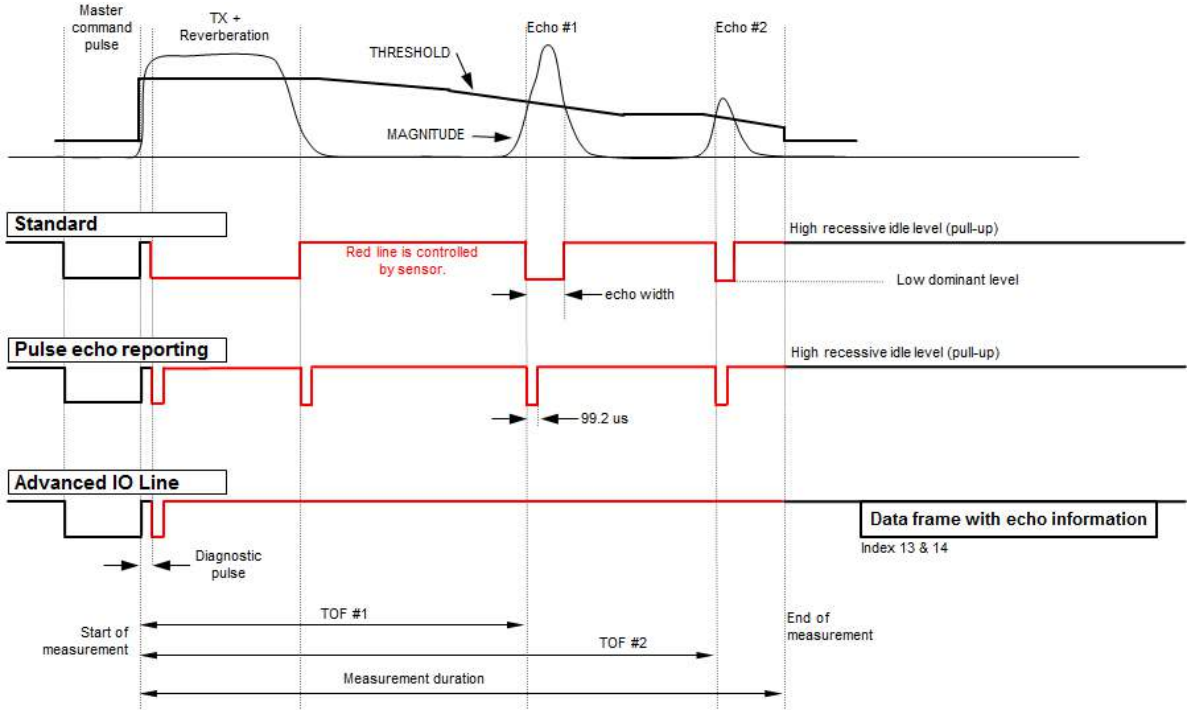
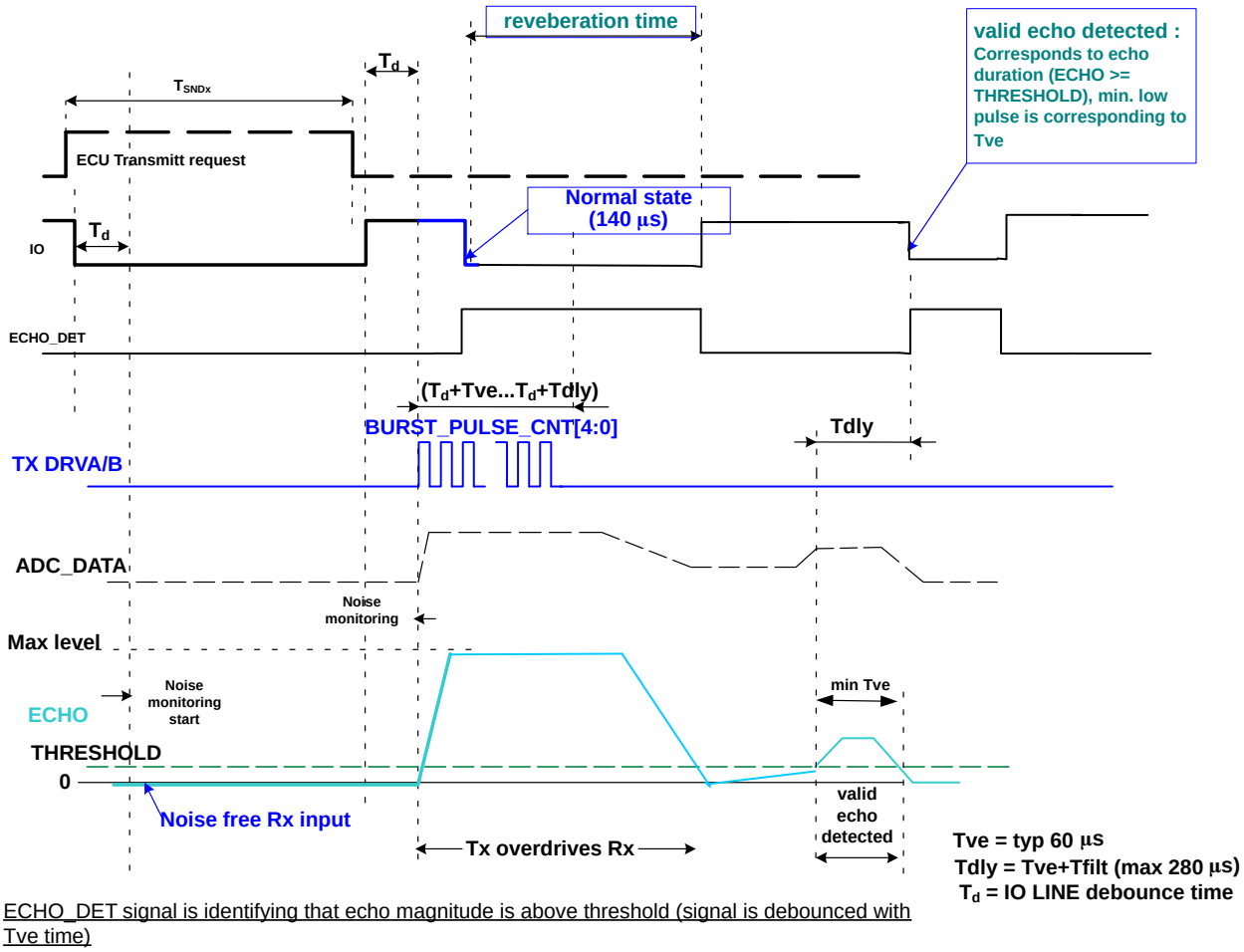


Figure 14. I/O Line Measurement Modes Comparison

Table 31. I/O LINE MEASUREMENT MODES COMPARISON

Measurement IO Line Mode	Diagnostic Pulse IO_TRANS_DIAG_ENA	Echo IO Line Reporting	Echo Width Information	Measurement Can be Stopped
Standard IO_ECHO_PULSE_ENA = 0 ADV_IO_ENA = 0	Yes (optional)	Dominant pulse	Yes	No
Pulse Echo Reporting IO_ECHO_PULSE_ENA = 1 ADV_IO_ENA = 0	Yes (optional)	Dominant pulse of 99,2 μs	No	Yes …by at least 350 μs dominant pulse which is generated by the I/O Line master.
Advanced IO Line IO_ECHO_PULSE_ENA = 0 ADV_IO_ENA = 1	Yes (always, it is used for acknowledge)	IO Line is idle during measurement => **No Disturbance** Echoes times are reported in configuration memory index 13 and 14.	No	Yes …by 100 μs dominant pulse or any command pulse which is generated by the I/O Line master.

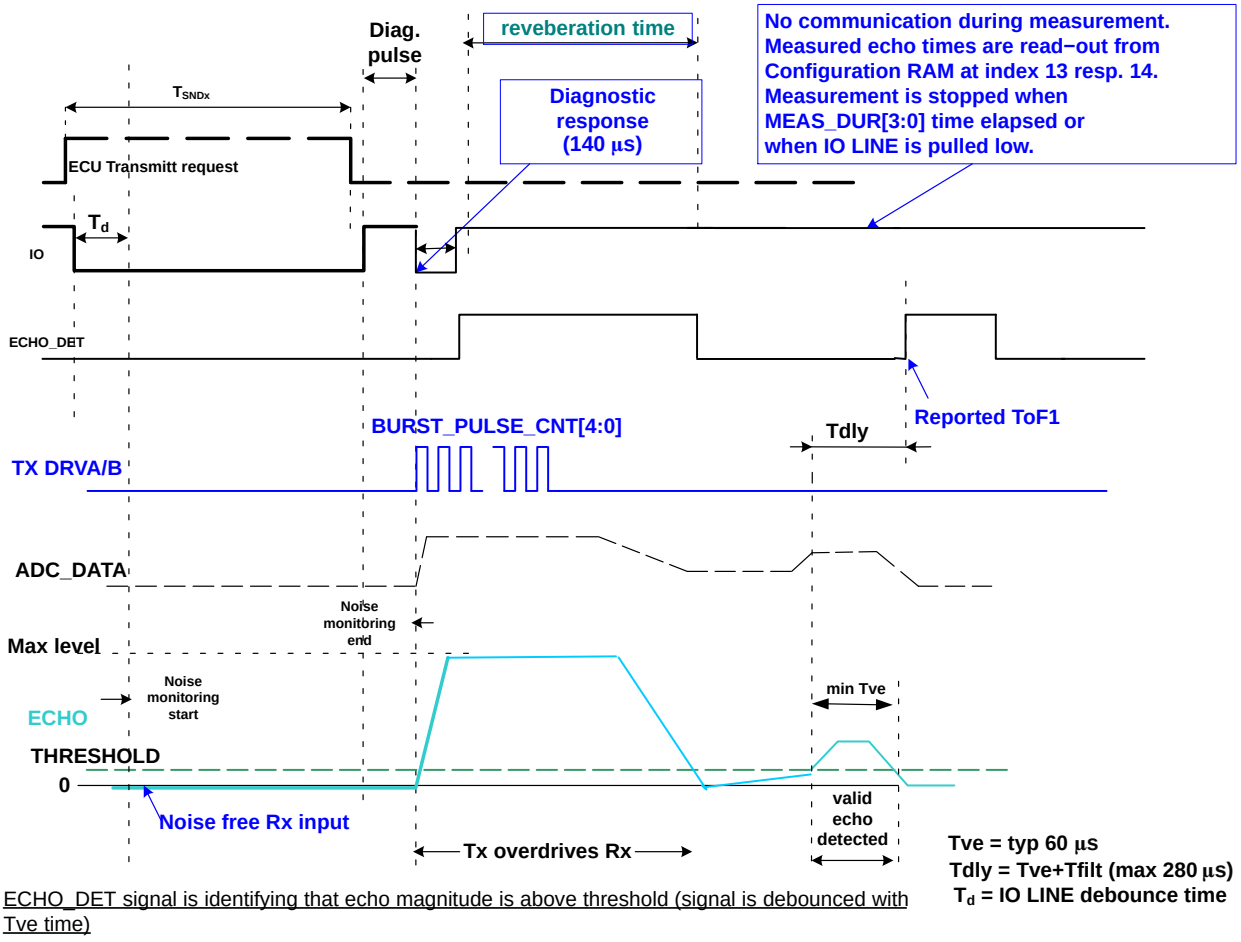
T_{SND1}/T_{SND2} Command (Direct Measurement); ADV_IO_ENA = 0



ECHO_DET signal is identifying that echo magnitude is above threshold (signal is debounced with Tve time)

Figure 15. Send Command Sequence with Threshold Table 1 (T_{SND1}) and Threshold Table 2 (T_{SND2}) Noise Free and Defect Free Case

T_{SND1}/T_{SND2} Command (Direct Measurement); ADV_IO_ENA = 1



ECHO_DET signal is identifying that echo magnitude is above threshold (signal is debounced with Tve time)

Figure 16. Send Command Sequence with Threshold Table 1 (T_{SND1}) and Threshold Table 2 (T_{SND2}) Noise Free and Defect Free Case

T_{REC1}/T_{REC2} Command (Indirect Measurement); ADV_IO_ENA = 0

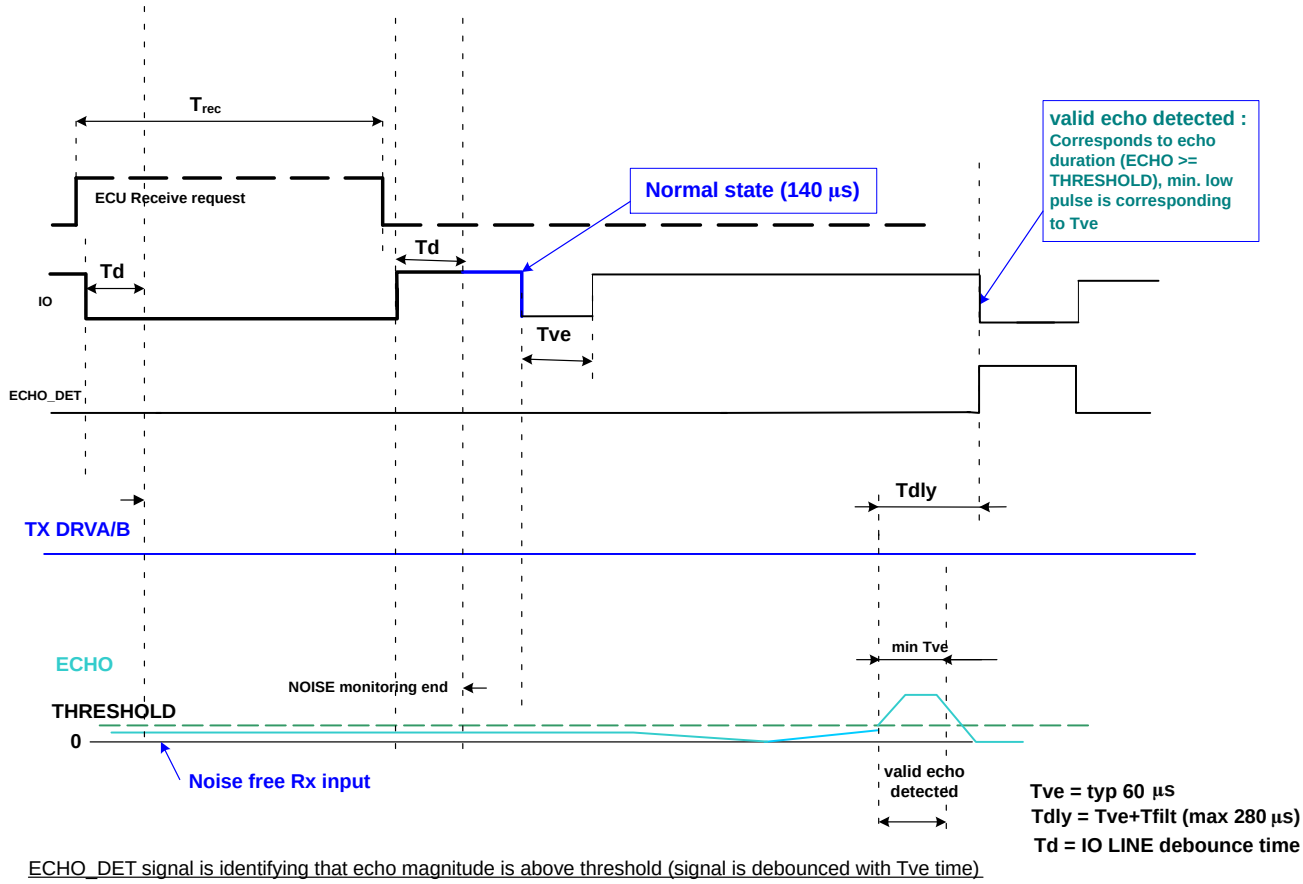


Figure 17. Receive Command Sequence
Noise Free and Defect Free Case

T_{REC1}/T_{REC2} Command (Indirect Measurement); ADV_IO_ENA = 1

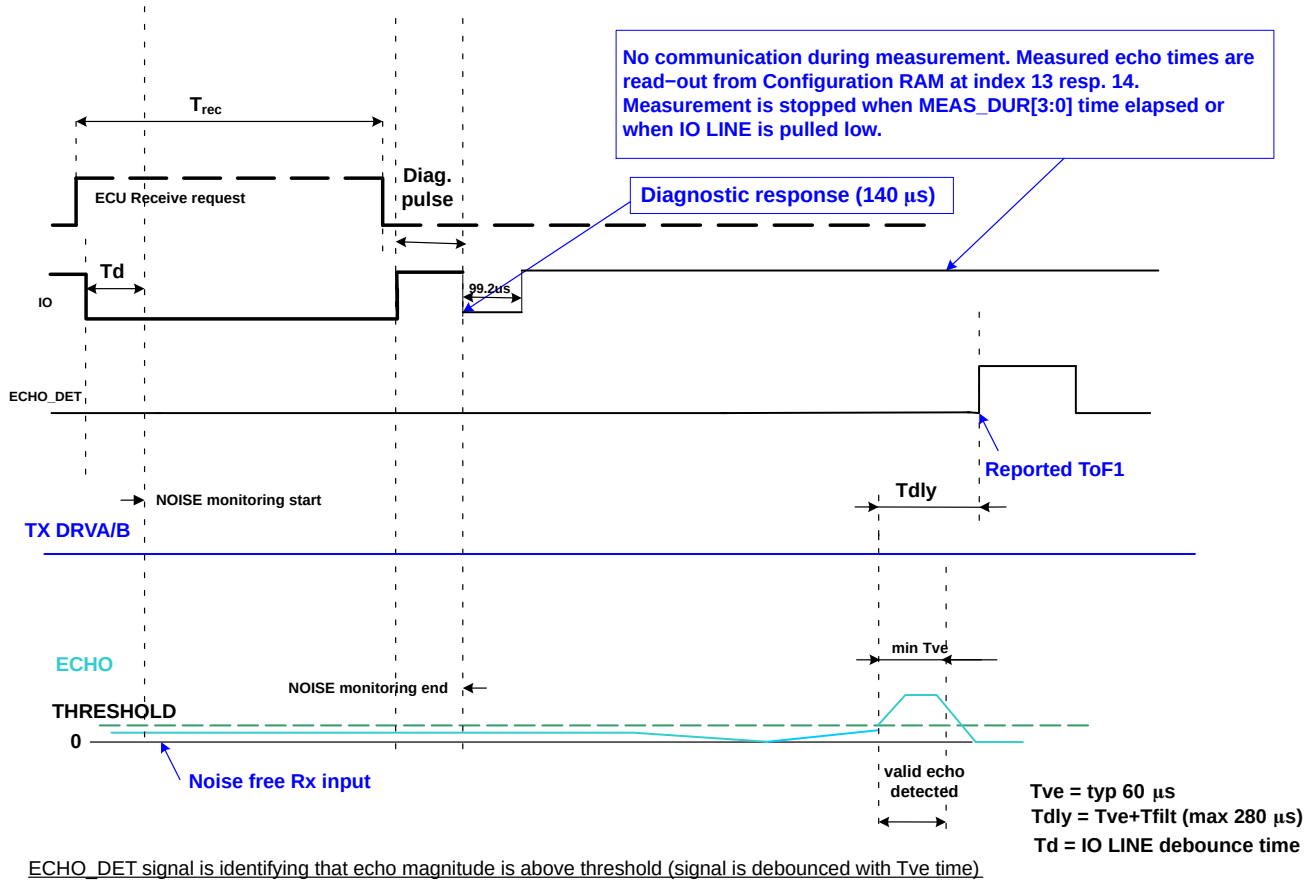
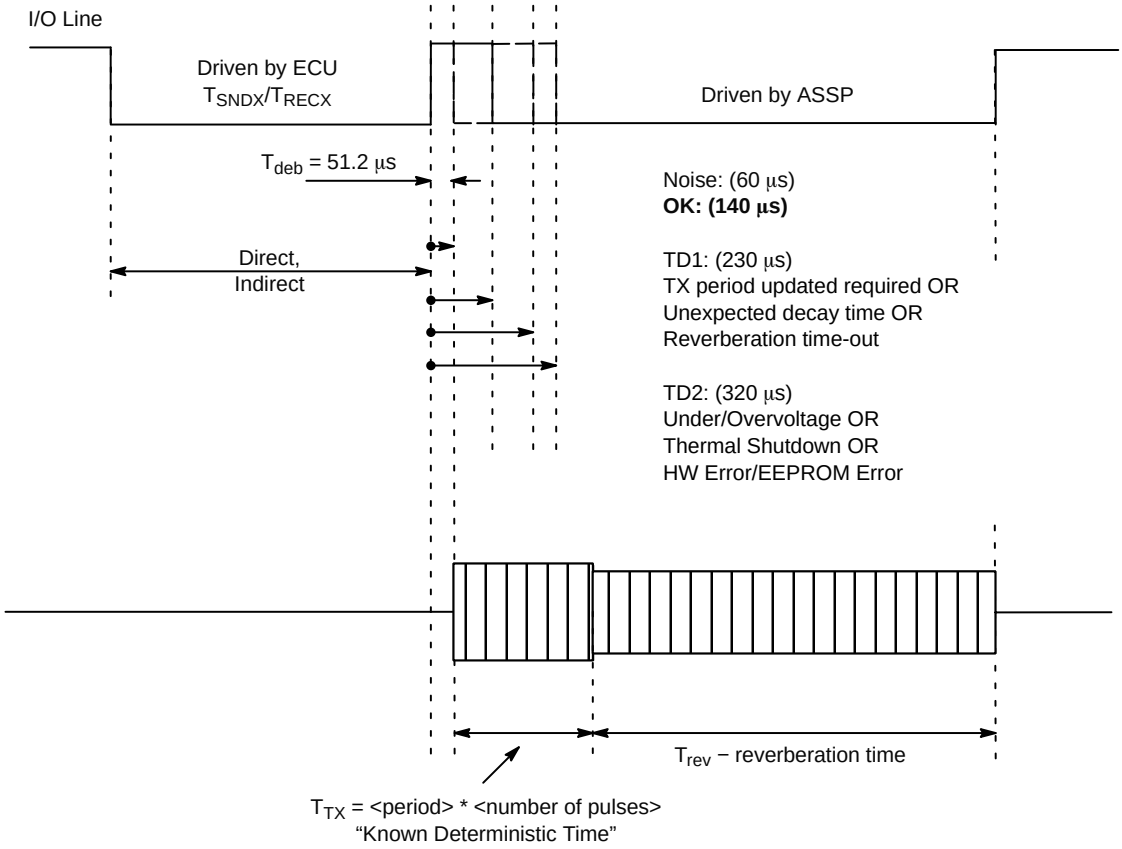


Figure 18. Receive Command Sequence
Noise Free and Defect Free Case



Note: All NCV75215 generated timing has accuracy of 3%.

Figure 19. I/O Line Noise Reporting and Sensor Defect Reporting (Diagnostic Pulse) for T_{SNDx} and T_{RECx} Commands

DATA COMMUNICATION

Every I/O Line data communication starts by T_{DATA} command pulse. The chip supports index data read and write transfers.

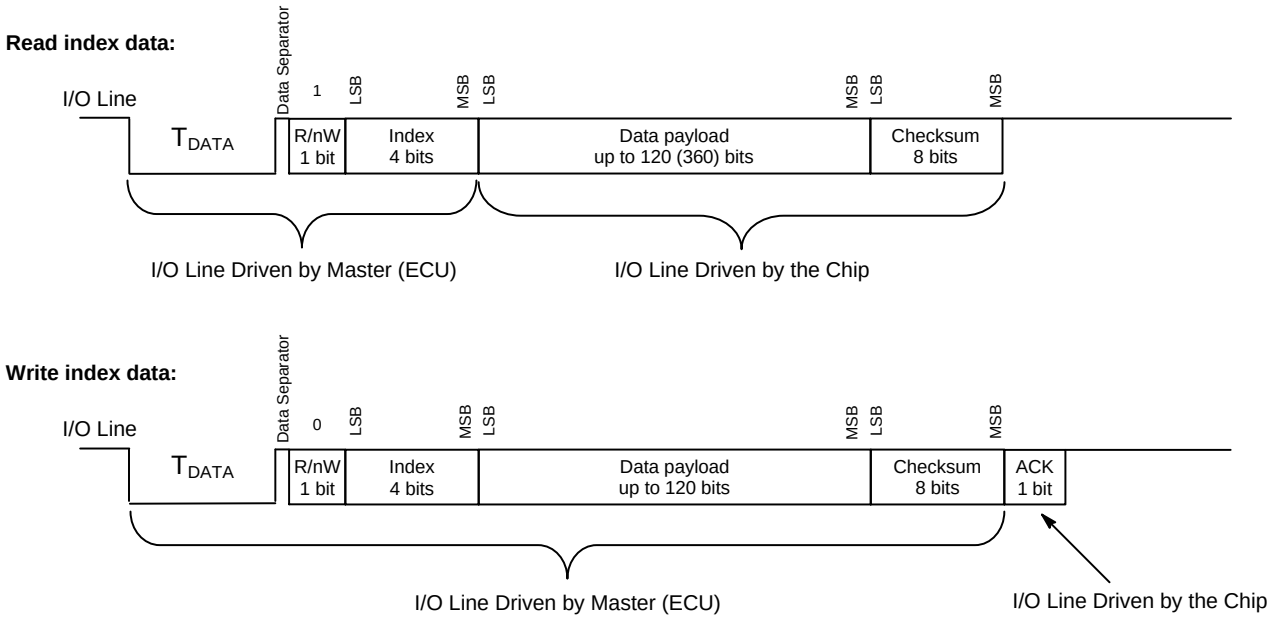


Figure 20. Read and Write Index Data

Table 32. I/O LINE DATA COMMUNICATIONS COMMAND

Command Part	No. of Bits	Typical Time [μs]	Note
Command pulse T_{DATA}	–	1270	I/O Line low
Data separator*	–	100	I/O Line high (idle)
R/nW bit	1	300	0 … write operation, 1 … read
Configuration memory index	4	1200	4 address bits
Data payload	x	300 * x	x … number of bits
Enhanced check sum	8	2400	
Acknowledge bit	(1)	(300)	Write operation only
Command separator	–	> 100	I/O Line high (idle)

*When reception of data separator is finished (identified by I/O Line falling edge of R/nW bit) temperature measurement is executed. Typical duration of temperature measurement is 10 μs.

Total data write command time in [μs] :

T_{DATA}(DATA_WRITE) = 5670 + 300 * <number of data payload bits>

Every data bit is modulated as I/O Line PWM pulse according to the Figure 21.

The ECU should drive I/O Line low for t_{typ} [μs] (T_{BIT_LOW} = 1/3 * T_{BIT}, T_{BIT_HIGH} = 2/3 * T_{BIT}, where T_{BIT} = 300 μs).

Data rate is accepted from 2.7 kbit/s to 4.4 kbit/s (typically 3.3 kbit/s).

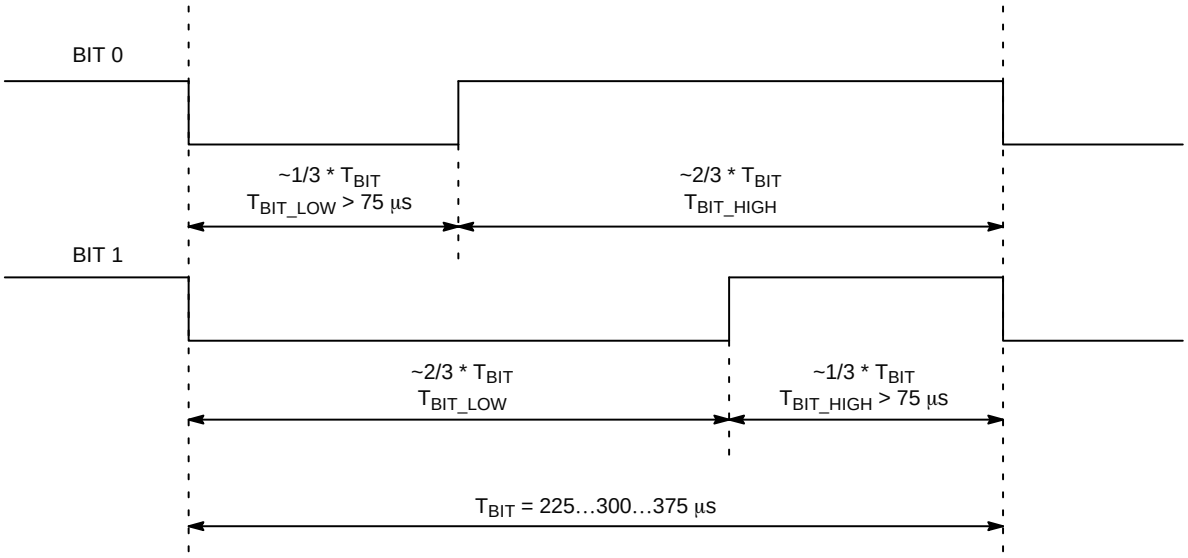


Figure 21. BIT0/BIT1 Coding

Meaning of R/nW + Address bits and overview of Configuration Memory indexes is in table below:

Table 33.

Addressing: R/nW + 4 Index Address Bits	Config Memory Index	Configuration Memory Index Description
R 0000	0	Temperature
R 0001	1	Status byte + Reverberation period
R/nW 0010	2	Carrier Period
R/nW 0011	3	TX burst pulse count
R/nW 0100	4	Measurement duration
R/nW 0101	5	Threshold table #1
R/nW 0110	6	Threshold table #2
R/nW 0111	7	Gain + Noise measurement setting
R/nW 1000	8	Dynamic gain
R/nW 1001	9	User data
R/nW 1010	10	Reverberation + TX current + other setting
R/nW 1011	11	Super read / write
R 1100	12	Measurement echo magnitude data (sampled echo magnitude)
R 1101	13	Measurement results − short
R 1110	14	Measurement results − long
R/nW 1111	15	Command Byte/Chip ID

CHECKSUM

Validity of data transferred over I/O Line is ensured by Enhanced 8-bit Checksum. The checksum calculation is explained in example below.

Example:
R/nW = 1 (read operation)
Index = 2 = 0010 bin
CARRIER_PER [10:0] = 3EA hex
11 data payload bits => 2 bytes for checksum calculation

1. 8-bit Checksum Initial Value

Bit	7	6	5	4	3	2	1	0
Data	R/nW	Index bit 3	Index bit 2	Index bit 1	Index bit 0	0	0	0
Example = 0x90	1	0	0	1	0	0	0	0

2. Data

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 Example = 0xEA	CP7 (Note 28)	CP6	CP5	CP4	CP3	CP2	CP1	CP0
	1	1	1	0	1	0	1	0
1 Example = 0x03	0 (Note 27)	0 (Note 27)	0 (Note 27)	0 (Note 27)	0 (Note 27)	CP10	CP9	CP8
	0	0	0	0	0	0	1	1

27. Incomplete byte is padded by 0 s.
28. “CP” stands for CARRIER_PER.

3. Checksum Calculation

Algorithm:

```
unsigned int check_sum =
             (RnW << 7) | (index << 3);
for (i=0; i<byte_count; i++)
    { check_sum = check_sum + data_byte[i];
      if (check_sum > 255)
          check_sum = check_sum – 255;
    }
check_sum = check_sum ^ 0xFF;
```

Example:

check_sum = 0x90 (initial value in this example)

byte #0:
check_sum = 0x90 + 0xEA = 0x17A
check_sum = 0x17A – 0xFF = 0x7B

byte #1:
check_sum = 0x7B + 0x03 = 0x7E

4. Checksum Inversion

check_sum = 0x7E xor 0xFF = 0x81

Checksum to transmit is inversion of final checksum accumulator (not 0x7E => 0x81 to transmit/check as checksum).

ACKNOWLEDGE BIT

Meaning of Acknowledge bit is explained in Figure 22.

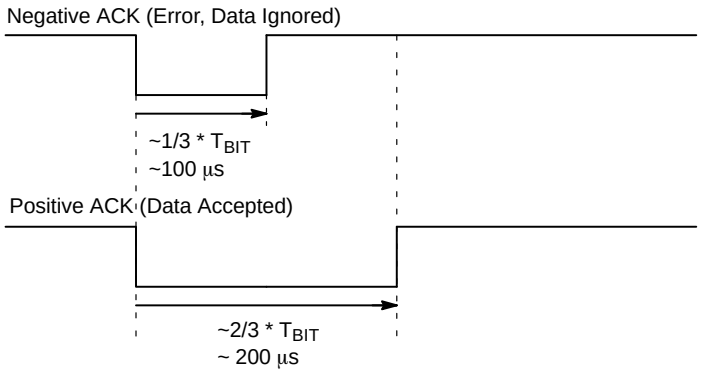
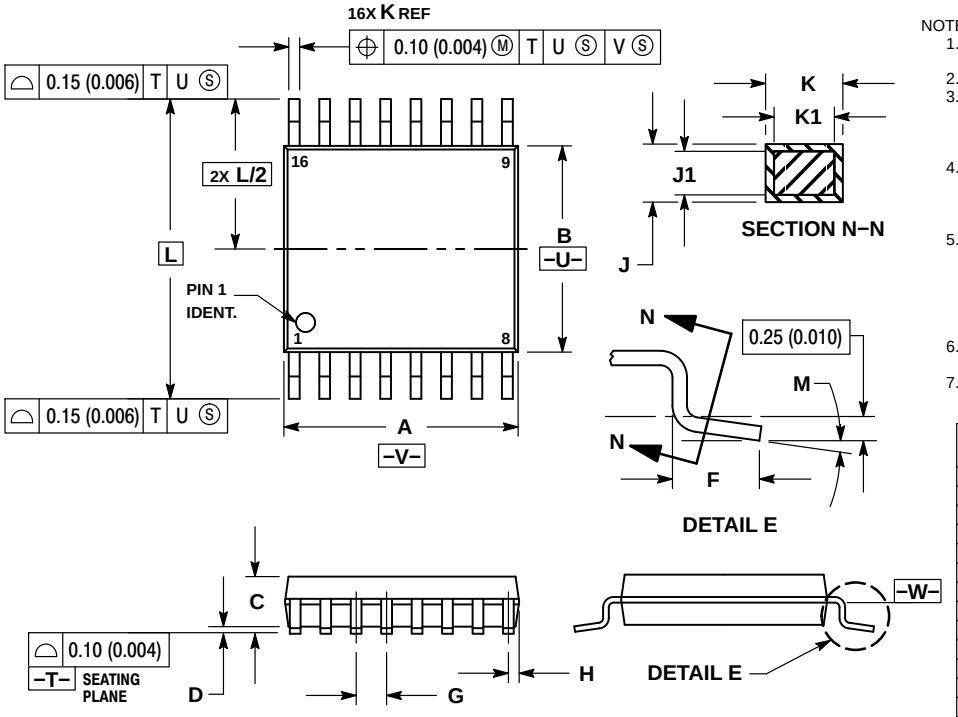


Figure 22. I/O Data Communication − Meaning of Acknowledge Bit

The chip transmits acknowledge bit after reception of the last checksum bit. Acknowledge bit is transmitted after data write transfer only.

PACKAGE DIMENSIONS

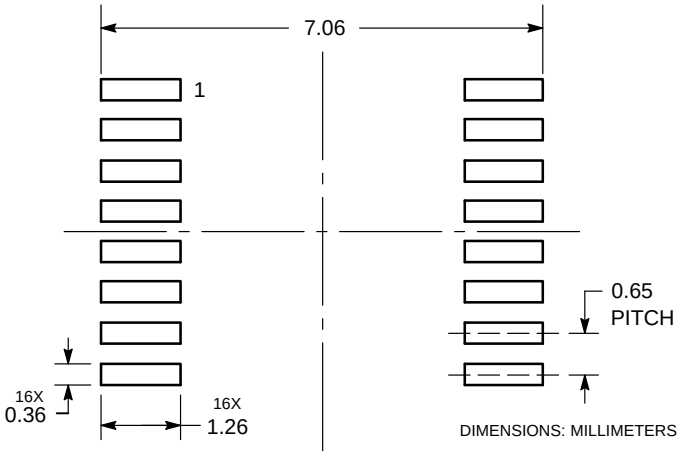
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



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