

DESCRIPTION

The MP2141N is a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs. It can achieve 1A of continuous output current from a 2.3V-to-5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time control scheme provides a fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2141N is available in an ultra-small SOT563 package and requires a minimal number of readily available, standard, external components.

The MP2141N is ideal for a wide range of applications, including high-performance DSPs, wireless power, portable and mobile devices, and other low-power systems.

FEATURES

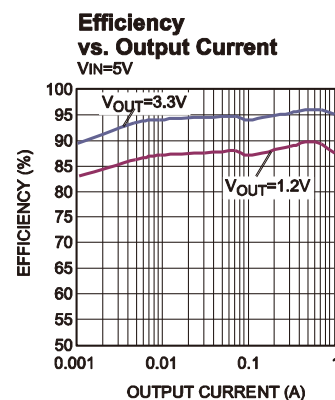
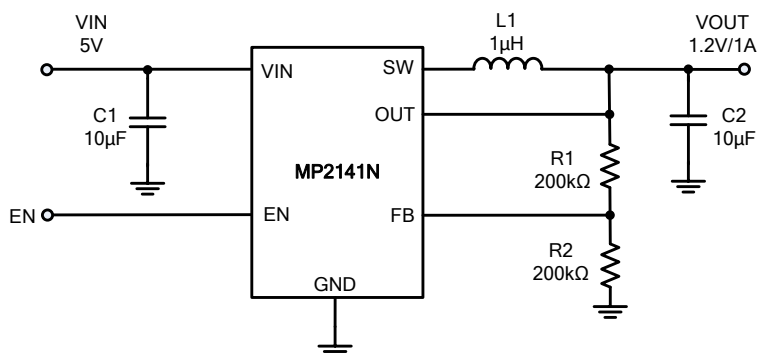
- Low Quiescent Current: 11µA
- 2.2MHz Switching Frequency
- EN for Power Sequencing
- Wide 2.3V-to-5.5V Operating Input Range
- Output Adjustable from 0.6V
- Up to 1A Output Current
- 120mΩ and 80mΩ Internal Power MOSFET Switches
- Output Discharge
- Short-Circuit Protection (SCP) with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- 100% Duty Cycle
- Power Good Only for Fixed Output Version
- Available in a SOT563 Package

APPLICATIONS

- Wireless/Networking Cards
- Portable and Mobile Devices
- Battery-Powered Devices
- Low-Voltage I/O System Power

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	V _{OUT} Range
MP2141NGTF*	SOT563	See Below	Adjustable
MP2141NGTF-15**		See Below	Fixed 1.5V
MP2141NGTF-18**		See Below	Fixed 1.8V

* For Tape & Reel, add suffix -Z (e.g. MP2141NGTF-Z)

** Contact factory for fixed output options

TOP MARKING (MP2141NGTF)**AUDY****LLL**

AUD: Product code of MP2141NGTF
Y: Year code
LLL: Lot number

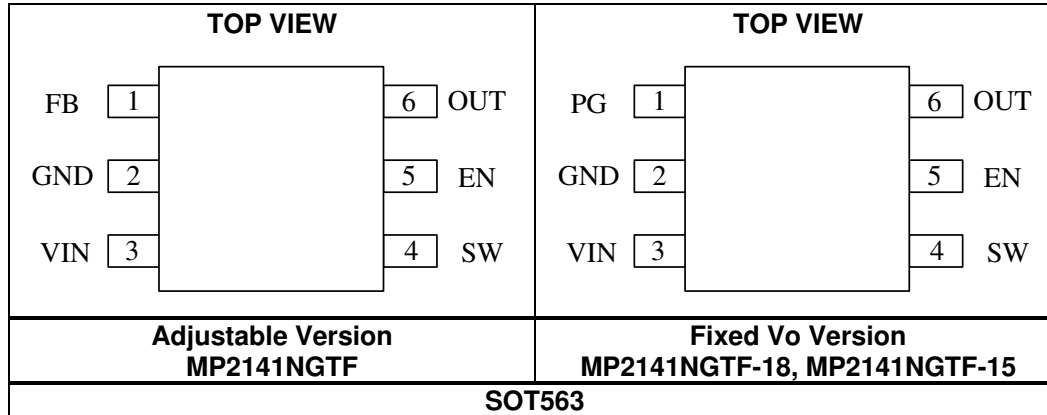
TOP MARKING (MP2141NGTF-15)**AUNY****LLL**

AUN: Product code of MP2141NGTF-15
Y: Year code
LLL: Lot number

TOP MARKING (MP2141NGTF-18)**AUPY****LLL**

AUP: Product code of MP2141NGTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V _{IN})	6V
V _{SW}	-0.3V (-5V for <10ns) to 6V (8V for <10ns or 10V for <3ns)
All other pins	-0.3V to 6V
Junction temperature	150°C
Lead temperature	260°C
Continuous power dissipation (T _A = +25°C) ⁽²⁾ ⁽⁴⁾	1.5W
Storage temperature.....	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V _{IN})	2.3V to 5.5V
Operating junction temp. (T _J)...	-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}
EV2141N-TF-00A ⁽⁴⁾	80	50 °C/W
SOT563 ⁽⁵⁾	130	60 °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on EV2141N-TF-00A, 2-layer PCB.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁷⁾. Typical value is tested at $T_J = +25^{\circ}C$. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	$2.3V \leq V_{IN} \leq 5.5V$, $T_J = 25^{\circ}C$	594	600	606	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	588		612	
Fixed Output Voltage ⁽⁸⁾		Only for MP2141NGTF-18, $I_{OUT} = 10mA$, $T_J = 25^{\circ}C$	1.782	1.8	1.818	V
		Only for MP2141NGTF-18, $I_{OUT} = 10mA$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$	1.764	1.8	1.836	V
		Only for MP2141NGTF-15, $I_{OUT} = 10mA$, $T_J = 25^{\circ}C$	1.485	1.5	1.515	V
		Only for MP2141NGTF-15, $I_{OUT} = 10mA$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$	1.470	1.5	1.530	V
Feedback current	I_{FB}	$V_{FB} = 0.63V$		50	100	nA
P-FET switch on resistance	R_{DSON_P}			120		m Ω
N-FET switch on resistance	R_{DSON_N}			80		m Ω
Switch leakage current		$V_{EN} = 0V$, $V_{IN} = 6V$, $V_{SW} = 0V$ and $6V$, $T_J = 25^{\circ}C$		0	1	μ A
P-FET peak current limit		Sourcing	1.8	2.4		A
N-FET valley current limit		Sourcing, valley current limit		1.5		A
ZCD				0		mA
On time	T_{ON}	$V_{IN} = 5V$, $V_{OUT} = 1.2V$		110		ns
		$V_{IN} = 3.6V$, $V_{OUT} = 1.2V$		150		
Switching frequency	f_s	$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{OUT} = 500mA$, $T_J = 25^{\circ}C$ ⁽⁵⁾	1760	2200	2640	kHz
		$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{OUT} = 500mA$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁵⁾	1650	2200	2750	
Minimum off time	$T_{MIN-OFF}$			60		ns
Minimum on time ⁽⁶⁾	T_{MIN-ON}			60		ns
Soft-start time	T_{SS-ON}	V_{OUT} rise from 10% to 90%		0.5		ms
Under-voltage lockout threshold rising				2	2.25	V
Under-voltage lockout threshold hysteresis				150		mV
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	R_{DIS}	$V_{EN} = 0V$, $V_{OUT} = 1.2V$		1		k Ω
EN input current		$V_{EN} = 2V$		1.2		μ A
		$V_{EN} = 0V$		0		μ A
Supply current (shutdown)		$V_{EN} = 0V$, $T_J = 25^{\circ}C$		0	1	μ A

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C⁽⁷⁾. Typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (quiescent)		V _{EN} = 2V, V _{FB} = 0.63V, V _{IN} = 3.6V, 5V, T _J = 25°C		11	13	μ A
Thermal shutdown ⁽⁶⁾				160		°C
Thermal hysteresis ⁽⁶⁾				30		°C
Power Good Leakage Current (Fixed V _o version only)	I _{PG}			50	100	nA
Power Good Upper Trip Threshold (Fixed V _o version only)		V _o with Respect to the Regulation		90		%
Power Good Lower Trip Threshold (Fixed V _o version only)				85		%
Power Good Delay (Fixed V _o version only)				70		μ s
Power Good Sink Current Capability (Fixed V _o version only)		Sink 1mA			400	mV

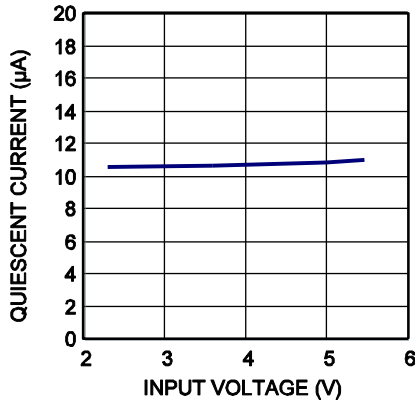
NOTES:

- 6) Guaranteed by engineer sample characterization, no production test.
- 7) Guaranteed by characterization test, no production test.
- 8) Without sleep mode.

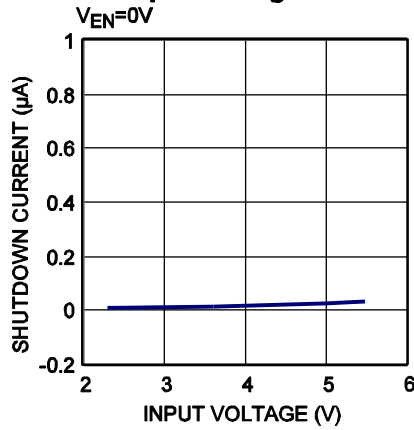
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0 μ H, T_A = +25°C, unless otherwise noted.

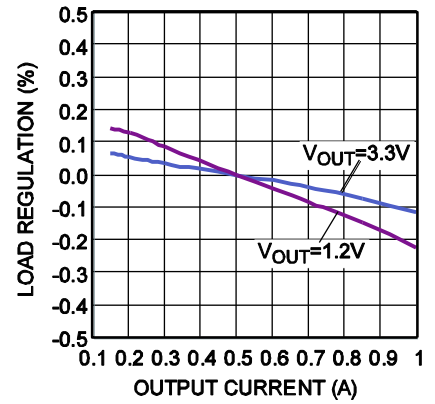
Quiescent Current vs. Input Voltage



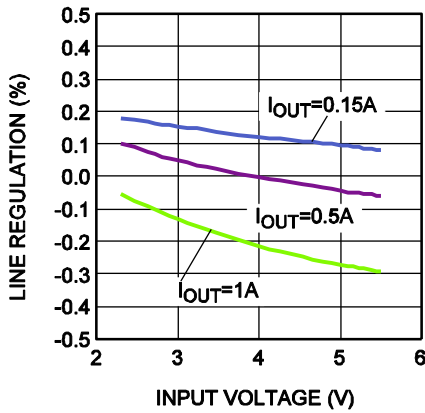
Shutdown Current vs. Input Voltage



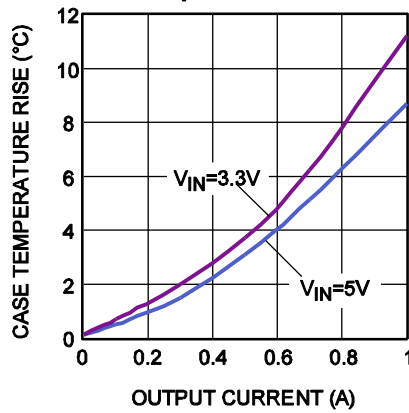
Load Regulation vs. Output Current



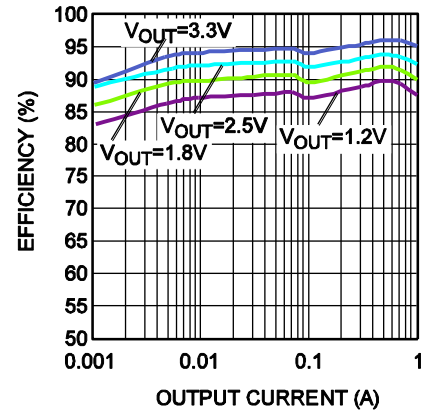
Line Regulation vs. Input Voltage



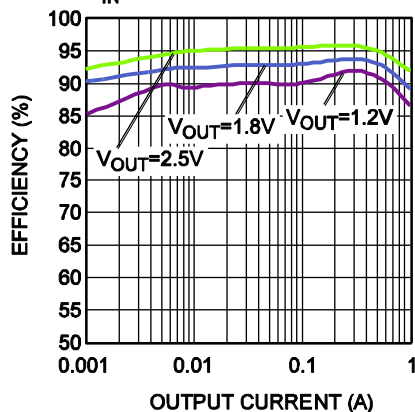
Case Temperature Rise vs. Output Current



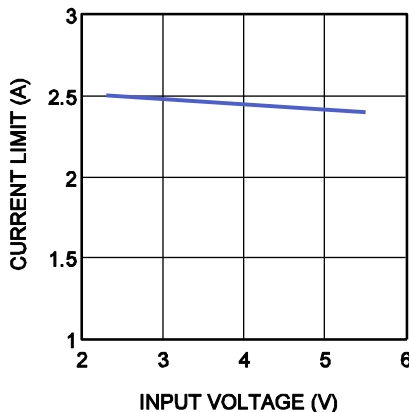
Efficiency vs. Output Current



Efficiency vs. Output Current

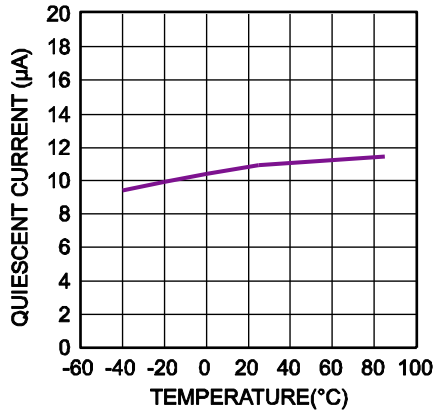
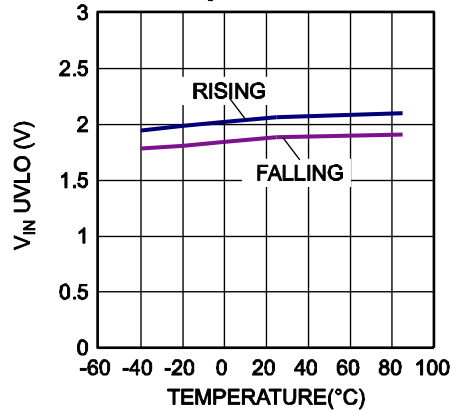
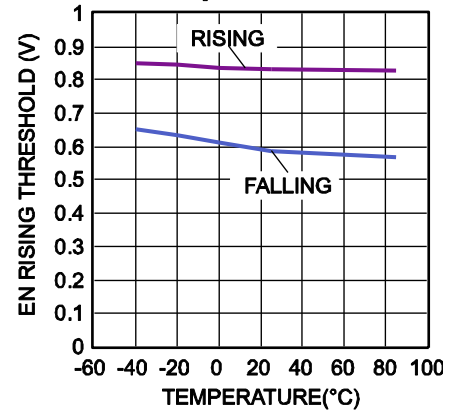
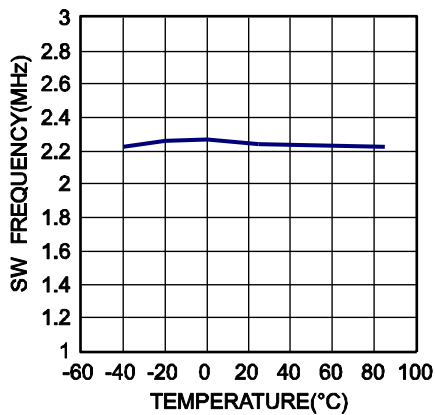


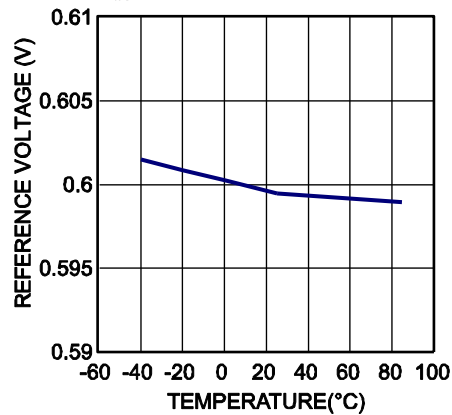
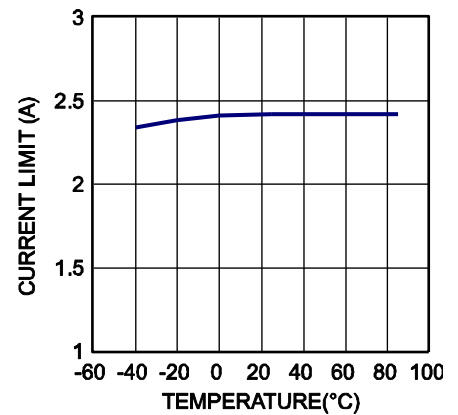
Current Limit vs. V_{IN}



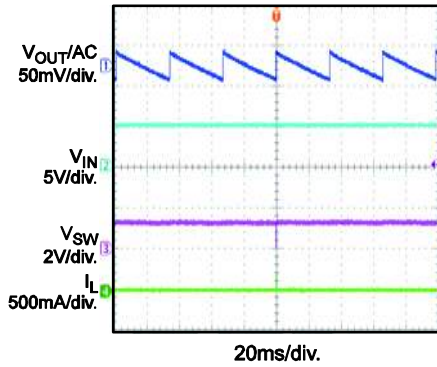
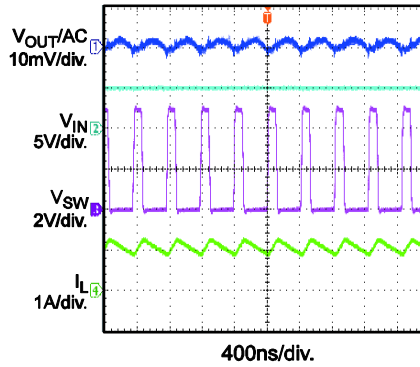
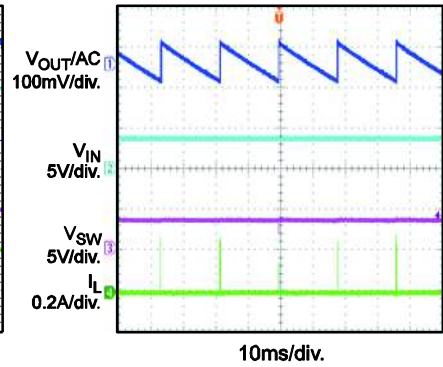
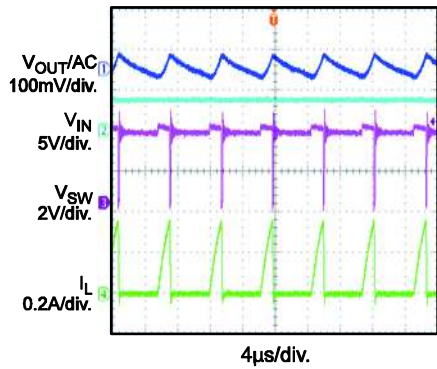
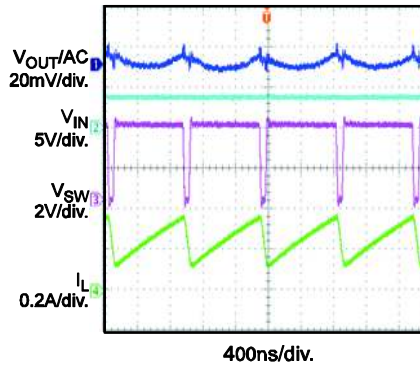
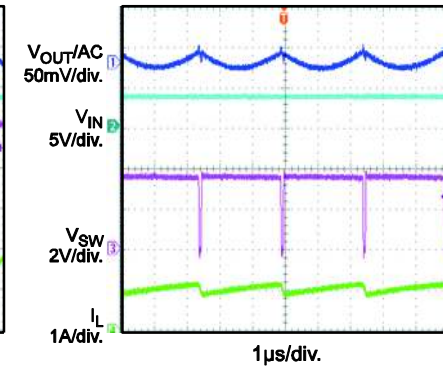
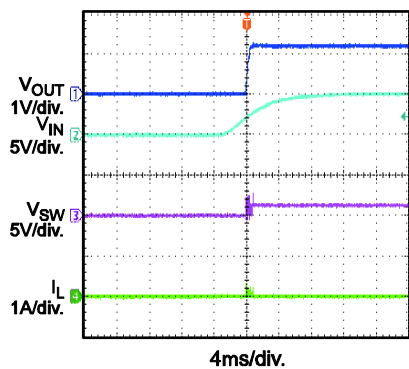
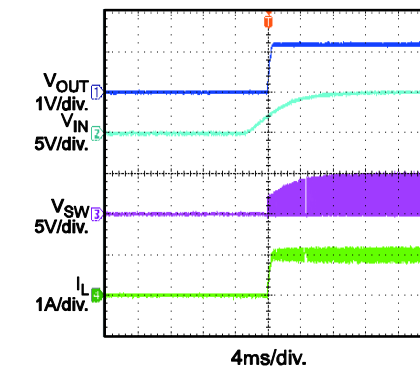
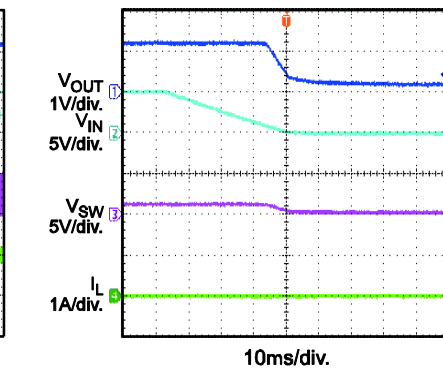
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

 V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0 μ H, T_A = +25°C, unless otherwise noted.

Quiescent Current vs. Temperature

V_{IN} UVLO Rising and Falling Threshold vs. Temperature

EN Rising and Falling Threshold vs. Temperature

Switch Frequency vs. Temperature

Reference Voltage vs. Temperature

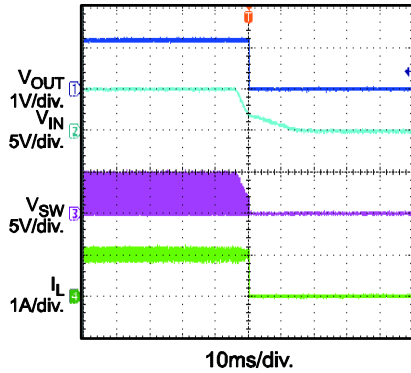
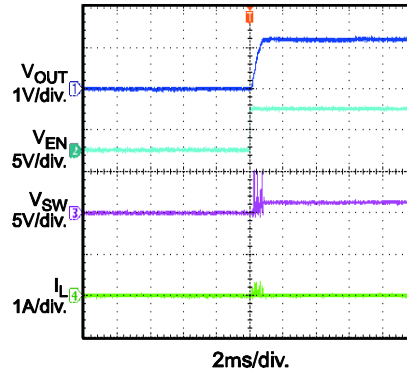
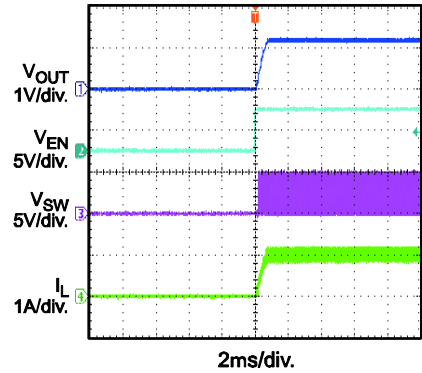
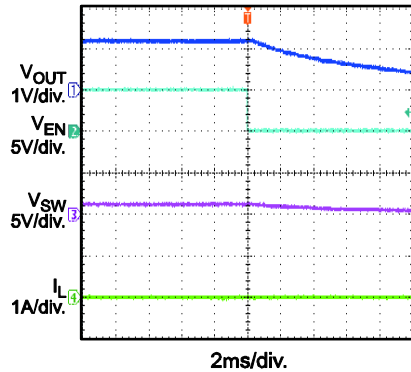
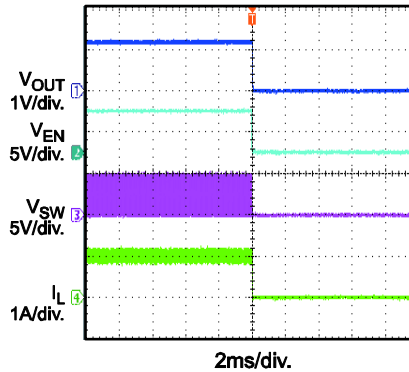
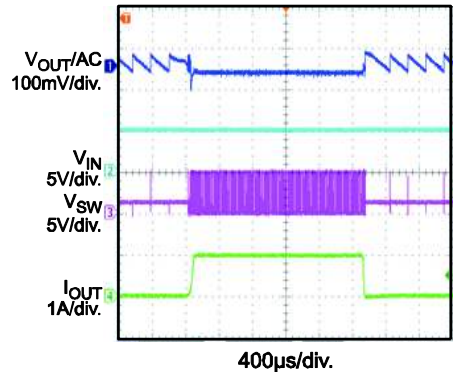
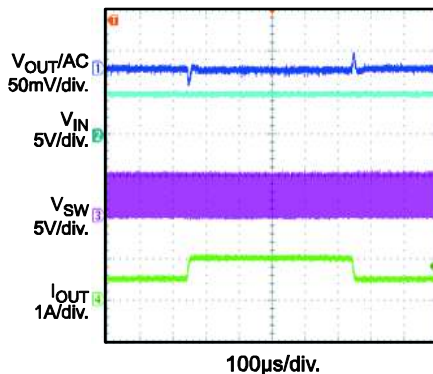
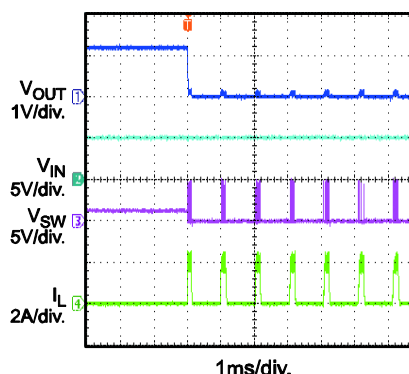
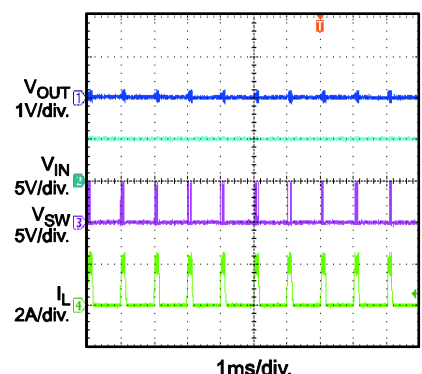
 V_{IN} = 3.6V

Current Limit vs. Temperature


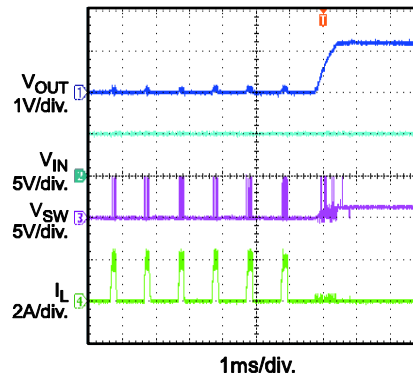
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 1.0\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

Steady State
without Load

Steady State
with 1A Load

Steady State
 $V_{IN}=3.6V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$

Steady State
 $V_{IN}=3.6V$, $V_{OUT}=3.3V$, $I_{OUT}=0.05A$, AAM

Steady State
 $V_{IN}=3.6V$, $V_{OUT}=3.3V$, $I_{OUT}=0.25A$, AAM

Steady State
 $V_{IN}=3.6V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, AAM

V_{IN} Power Up
without Load

V_{IN} Power Up
with 1A Load

V_{IN} Shut Down
without Load


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

 V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0 μ H, T_A = +25°C, unless otherwise noted.

V_{IN} Shut Down
with 1A Load

EN Start Up
without Load

EN Start Up
with 1A Load

EN Shut Down
without Load

EN Shut Down
with 1A Load

Load Transient Response
I_{OUT} = 0A to 1A

Load Transient Response
I_{OUT} = 0.5A to 1A

Short Circuit Entry

Short Circuit


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 1.0\mu H$, $T_A = +25^\circ C$, unless otherwise noted.**Short Circuit Recovery**

PIN FUNCTIONS

Pin #	Name	Description
1	FB/PG	MP2141NGTF: Feedback. An external resistor divider from the output to GND tapped to FB sets the output voltage. MP2141NGTF-18: Power Good Indicator. The output of this pin is an open drain with external pull up resistor to Vin.
2	GND	Power ground.
3	VIN	Supply voltage. The MP2141N operates from a +2.3V to +5.5V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at input.
4	SW	Output switching node. SW is the drain of the internal high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.
5	EN	On/off control.
6	OUT	Output voltage power rail and input sense. Connect the load to OUT. An output capacitor is needed to decrease the output voltage ripple.

BLOCK DIAGRAM

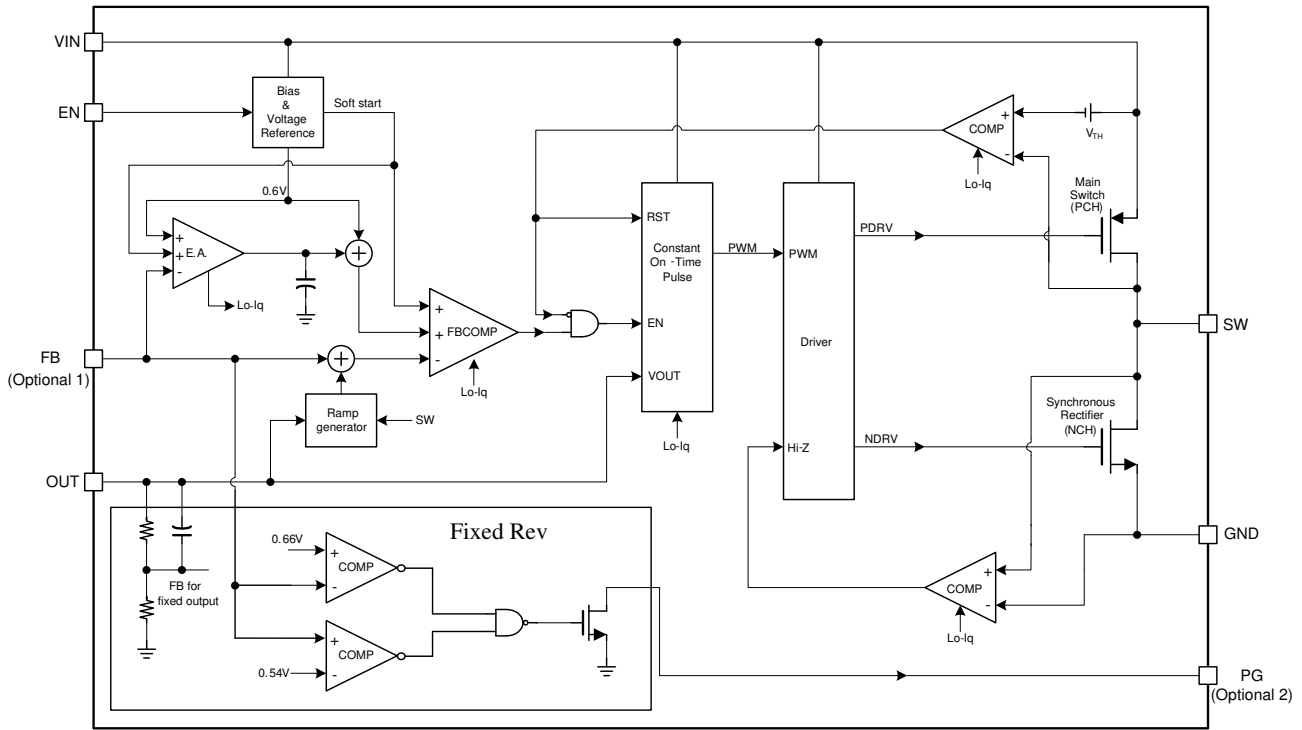


Figure 1: Functional Block Diagram

Note: Option 1- FB pin is only for MP2141NGTF

Option 2- PG pin is only for MP2141NGTF-18

OPERATION

The MP2141N uses constant-on-time control with an input voltage feed-forward to stabilize the switching frequency over the full input range. It achieves 1A of continuous output current from a 2.3V-to-5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-on-Time Control

Compared to fixed-frequency PWM control, constant-on-time control offers a simpler control loop and a faster transient response. By using an input voltage feed-forward, the MP2141N maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.454\mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the MP2141N uses a fixed minimum off time of 60ns.

Sleep Mode Operation

The MP2141N features sleep mode to achieve high efficiency at extremely light loads. In sleep mode, most of the circuit blocks are turned off except the error amplifier and the PWM comparator. Therefore, the operation current is reduced to a minimal value (see Figure 2).

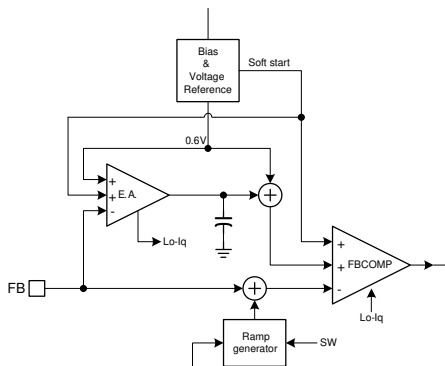


Figure 2: Operation Blocks at Sleep Mode

When the load becomes lighter, the output voltage ripple is bigger and drives the error amplifier output (EAO) lower. When the EAO hits an internal low threshold, it clamps at that level, and the MP2141N enters sleep mode.

During sleep mode, the valley of the FB voltage is regulated to the internal reference voltage, making the average output voltage slightly higher than the output voltage at DCM or CCM. The on-time pulse at sleep mode is around 40% larger than that in DCM or CCM. Figure 3 shows the average FB voltage relationship with the internal reference at sleep mode.

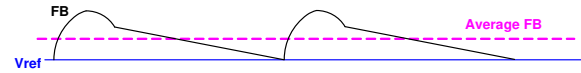


Figure 3: FB Average Voltage at Sleep Mode

When the MP2141N is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated, and the output voltage ripple decreases as well. Once the EAO is higher than the internal low threshold, the MP2141N exits sleep mode and enters DCM or CCM depending on the load. In DCM or CCM, the EAO regulates the average output voltage to the internal reference (see Figure 4).

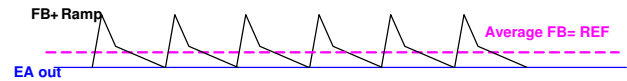


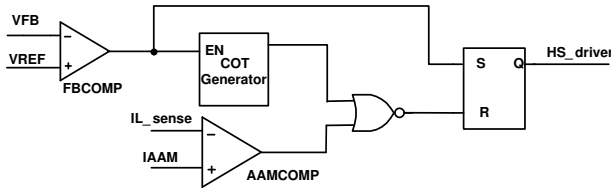
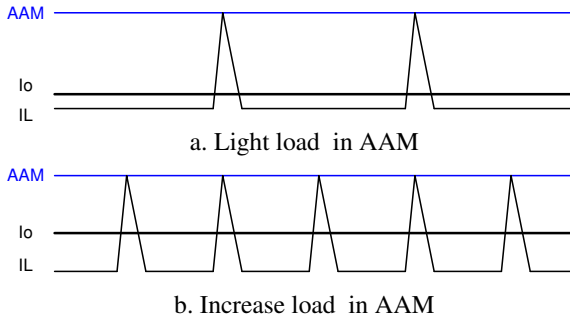
Figure 4: DCM Control

There is always a loading hysteresis when entering sleep mode and exiting sleep mode due to the error amplifier clamping response time.

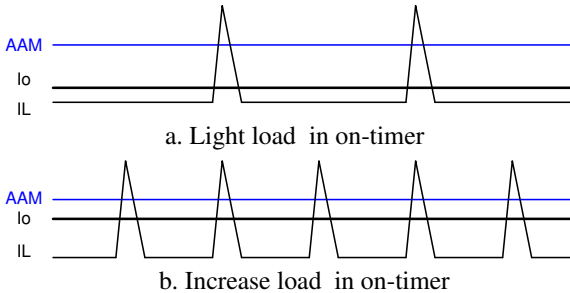
AAM Operation at Light-Load Operation

The MP2141N uses an advanced asynchronous modulation (AAM) power-save mode with a zero-current cross detection (ZCD) circuit for light loads.

The MP2141N uses AAM power-save mode in light loads (see Figure 5). The AAM current (I_{AAM}) is set internally. The SW on pulse time is decided by an on-time generator and AAM comparator. At light-load condition, SW on pulse time is stretched. The AAM comparator pulse is longer than the on-time generator. The mode of operation is shown below in Figure 6.


Figure 5: Simplified AAM Control Logic

Figure 6: AAM Comparator Control T_{ON}

The AAM comparator pulse is shorter than the on-time generator. The mode of operation is shown below in Figure 7. This usually occurs when using a very small inductance.


Figure 7: On-Time Control (T_{ON})

Besides the upper on time method, the AAM circuit has another 150ns AAM blank time in sleep mode. If the on-time is less than 150ns, the high-side MOSFET may turn off after the on-time generator pulse without AAM control. The on-time pulse at sleep mode is around 40% larger than that at DCM or CCM. In this condition, I_L may not reach the AAM threshold (see Figure 8).

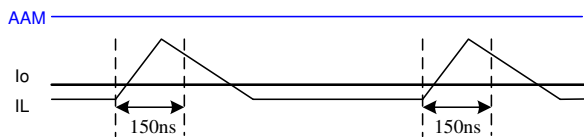
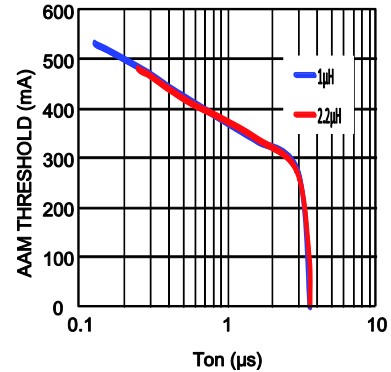

Figure 8: AAM Blank Time in Sleep Mode

Figure 9 shows the AAM threshold decreasing with T_{ON} increasing gradually. For CCM state, I_{OUT} requires at least more than half of the AAM threshold.

AAM Threshold vs. Ton

Figure 9: AAM Threshold Decreasing with T_{ON} Increasing

The MP2141N uses ZCD to detect if the inductor current begins reversing. When the inductor current reaches the ZCD threshold, the low-side switch is turned off.

AAM and the ZCD circuit together cause the MP2141N to work in DCM mode in light load continuously, even if V_{OUT} is close to V_{IN}.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2V), the MP2141N can be enabled by pulling EN higher than 1.2V. Floating EN or pulling it down to ground disables the MP2141N. There is an internal 1M Ω resistor from EN to ground.

When the device is disabled, the MP2141N goes into output discharge mode automatically. Its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MP2141N has a built-in soft start that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The soft start time is about 0.5ms, typically.

Current Limit

The MP2141N has a 2.4A high-side switch current limit, typically. When the high-side switch reaches its current limit, the MP2141N remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

Short Circuit and Recovery

The MP2141N enters short-circuit protection mode when it reaches the current limit and attempts to recover with hiccup mode. The MP2141N disables the output power stage, discharges the soft-start capacitor, and then attempts to soft start again automatically. If the short-circuit condition remains after the soft start ends, the MP2141N repeats this cycle until the short circuit disappears and the output rises back to regulation level.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application Circuit on page 17). Select the feedback resistor (R1), typically between 40kΩ to 200kΩ, to reduce the V_{OUT} leakage current. There is no strict requirement on the feedback resistor. R1 > 10kΩ is reasonable for most applications. Calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

Figure 10 shows the feedback circuit.

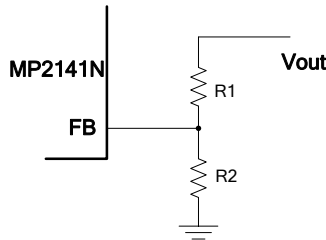


Figure 10: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 0.47μH-to-2.2μH inductor. Select an inductor with a DC resistance below 15mΩ to optimize efficiency.

A high-frequency switch mode power supply with a magnetic device has strong, electronic, magnetic inference for the system. Any unshielded power inductor should be avoided. Metal alloy or multi-layer chip power inductors are ideal shielded inductors for the application of the EMI, as they can decrease the influence effectively. Table 2 lists some recommended inductors.

Table 2: Suggested Inductor List

Manufacturer P/N	Inductance (μH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO. LTD.
1239AS-H-1R0M	1.0	Tokyo
74438322010	1.0	Würth

For most designs, the inductance value can be calculated with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. Higher output voltages may require a 22μF capacitor to increase system stability.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst case occurs at V_{IN} = 2V_{OUT}, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality 0.1μF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended. For best results, use low ESR capacitors to limit the output voltage ripple. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (8)$$

Where L₁ is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 11 and follow the guidelines below.

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to IN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short and away from the feedback network.
5. Keep the V_{OUT} sense line as short as possible or keep it away from the power inductor.

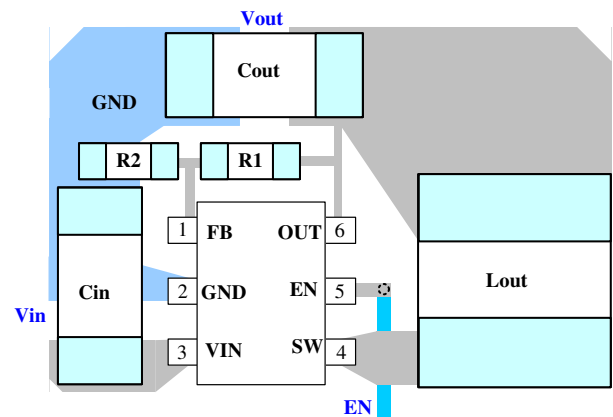


Figure 11: Two Ends of the Input Decoupling Capacitor Close to Pin 2 and Pin 3

TYPICAL APPLICATION CIRCUITS

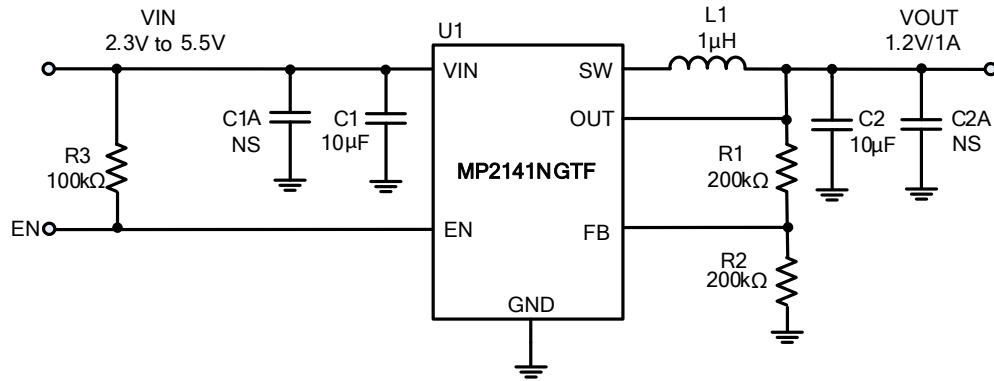


Figure 12: Typical Application Circuit for MP2141NGTF

NOTE: $V_{IN} < 3.3V$ may require more input capacitors

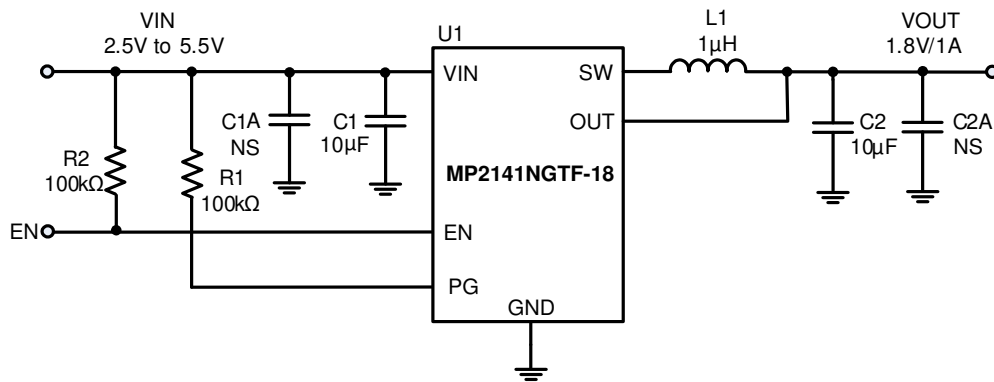
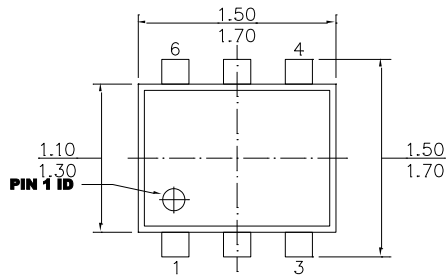


Figure 13: Typical Application Circuit for MP2141NGTF-18

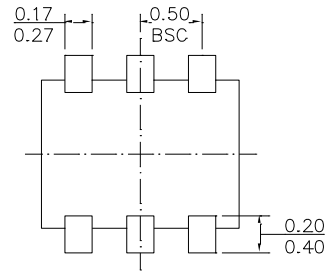
Note: $V_{IN} < 3.3V$ may need more input capacitor.

PACKAGE INFORMATION

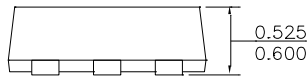
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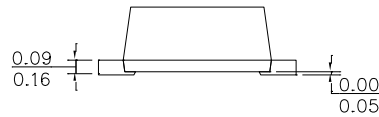
TOP VIEW



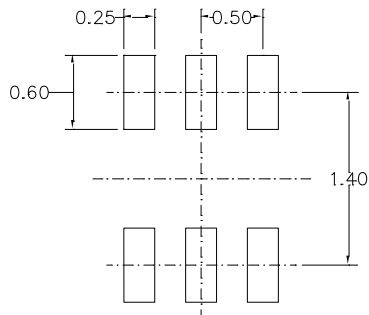
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING IS NOT TO SCALE.

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