

MOSFET – N-Channel, POWERTRENCH®

80 V, 100 A, 3.9 mΩ

FDMS039N08B

General Description

This N-Channel MOSFET is produced using onsemi's advance POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

- Max $R_{DS(on)}$ = 3.2 mΩ (Typ.) @ $V_{GS} = 10\text{ V}$, $I_D = 50\text{ A}$
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse Recovery Charge, $Q_{rr} = 80\text{ nC}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

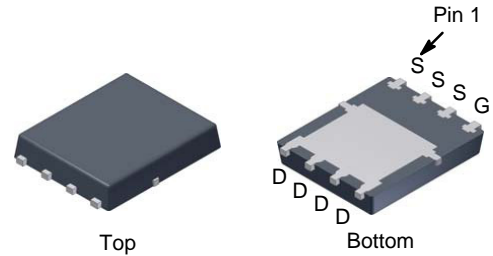
Symbol	Parameter	FDMS039N08B	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_A = 25^\circ\text{C}$) (Note 1a)	100	A
		19.4	
I_{DM}	Drain Current – Pulsed (Note 2)	400	mJ
E_{AS}	Single Pulse Avalanche Energy (Note 3)	240	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) ($T_A = 25^\circ\text{C}$) (Note 1a)	104	W
		2.5	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

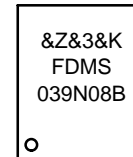
Symbol	Parameter	FDMS039N08B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
80 V	3.9 mΩ @ 10 V	100 A



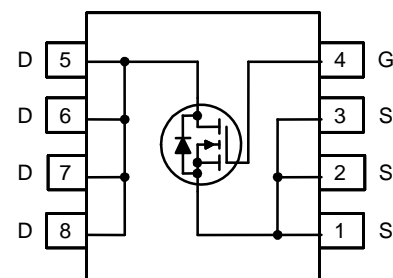
PQFN8 5X6, 1.27P
(Power 56)
CASE 483AE

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Code
FDMS039N08B = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDMS039N08B

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.04	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 50 A	–	3.2	3.9	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 50 A	–	100	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V f = 1 MHz	–	5715	7600	pF
C _{oss}	Output Capacitance		–	881	1170	pF
C _{rss}	Reverse Transfer Capacitance		–	15	–	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 40 V, V _{GS} = 0 V	–	1646	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 40 V, I _D = 50 A, V _{GS} = 0 V to 10 V (Note 4)	–	77	100	nC
Q _{gs}	Gate to Source Gate Charge		–	34	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	13	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	16	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.2	–	Ω

SWITCHING CHARACTERISTICS

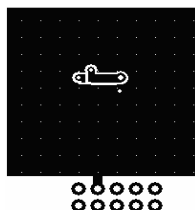
t _{d(on)}	Turn-On Delay Time	V _{DD} = 40 V, I _D = 50 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	42	94	ns
t _r	Turn-On Rise Time		–	25	60	ns
t _{d(off)}	Turn-Off Delay Time		–	48	106	ns
t _f	Turn-Off Fall Time		–	17	44	ns

DRAIN-SOURCE CHARACTERISTICS

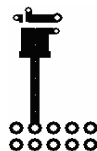
I _S	Maximum Continuous Drain to Source Diode Forward Current	–	–	100	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	400	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 50 A	–	–	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 50 A, V _{DD} = 40 V di/dt = 100 A/μs	–	68	–	ns
Q _{rr}	Reverse Recovery Charge		–	80	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- Repetitive rating; pulse-width limited by maximum junction temperature.
- L = 0.3 mH, I_{AS} = 40 A, starting T_J = 25°C.
- Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

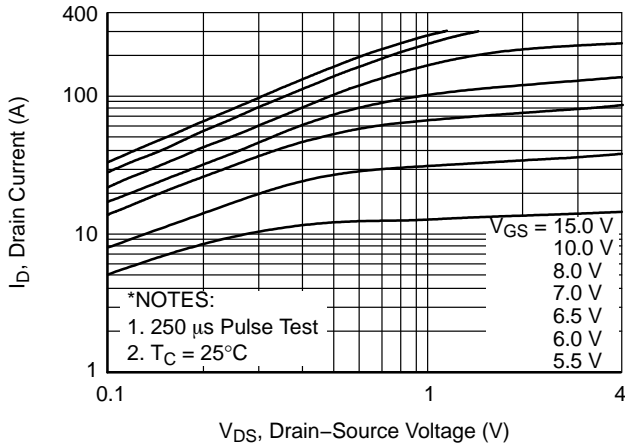


Figure 1. On-Region Characteristics

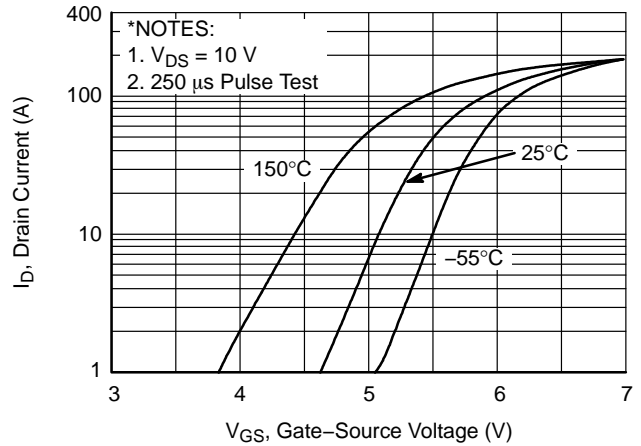


Figure 2. Transfer Characteristics

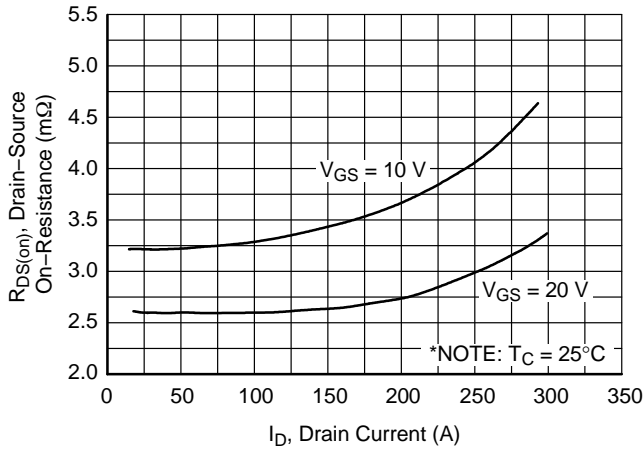


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

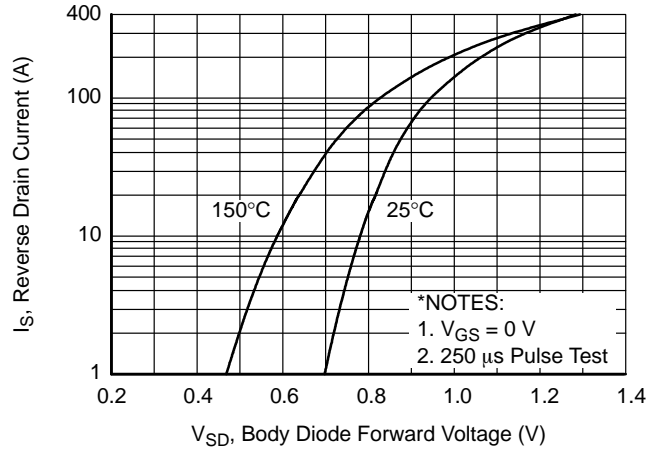


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

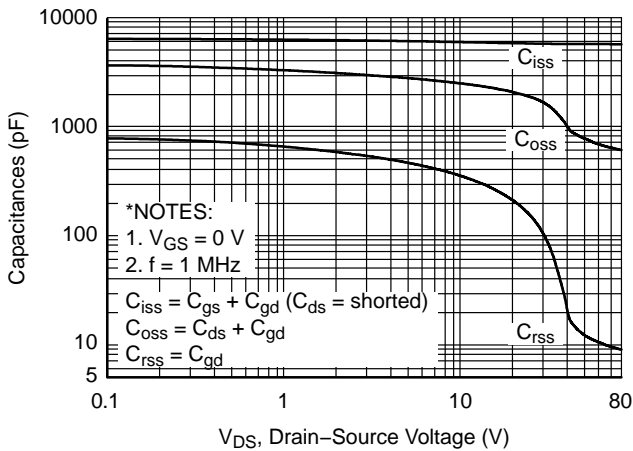


Figure 5. Capacitance Characteristics

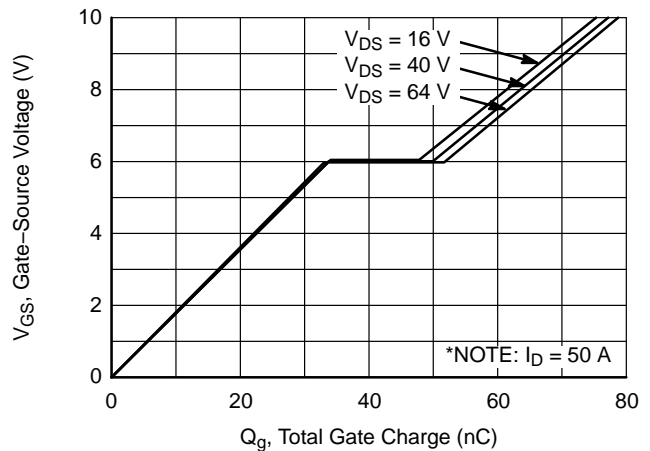


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

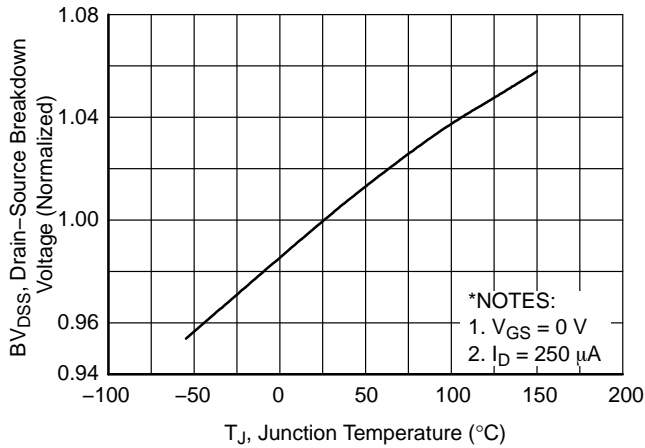


Figure 7. Breakdown Voltage Variation vs. Temperature

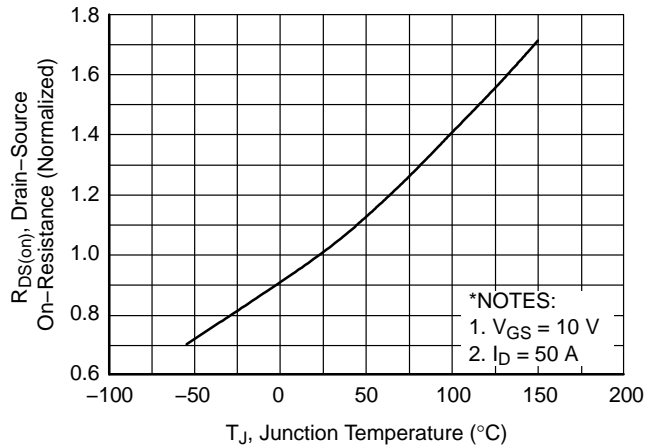


Figure 8. On-Resistance Variation vs. Temperature

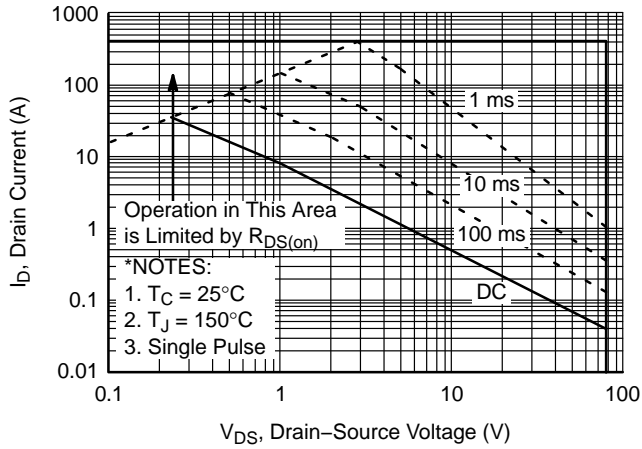


Figure 9. Maximum Safe Operating Area

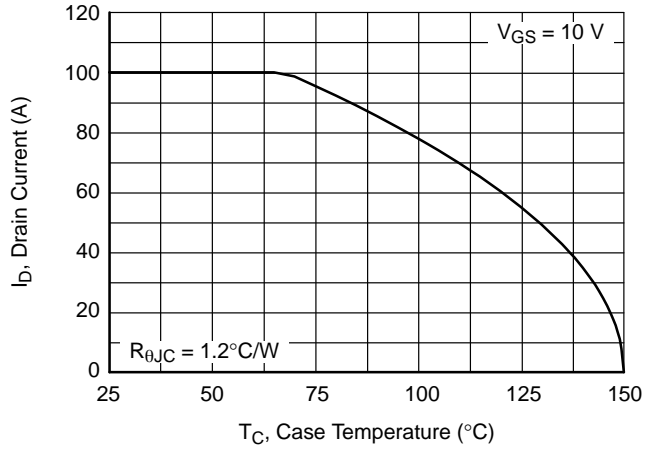


Figure 10. Maximum Drain Current vs. Case Temperature

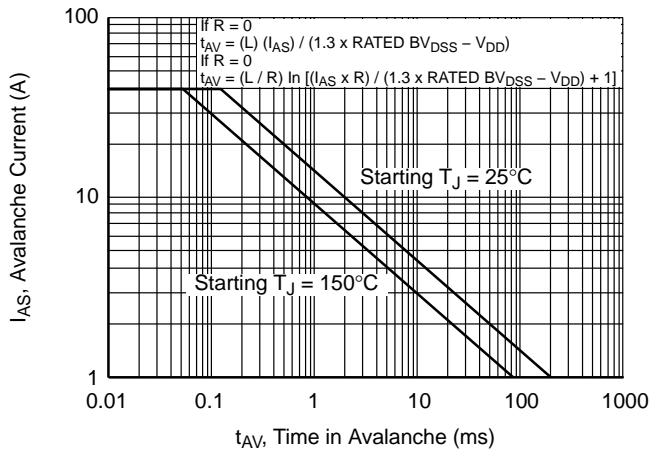


Figure 11. Unclamped Inductive Switching Capability

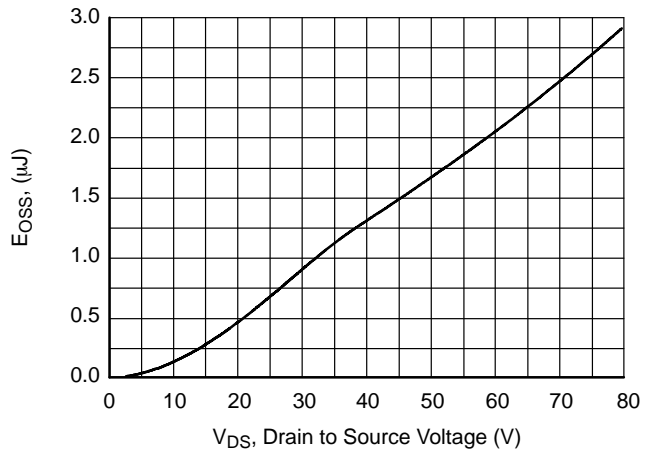


Figure 12. E_{oss} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

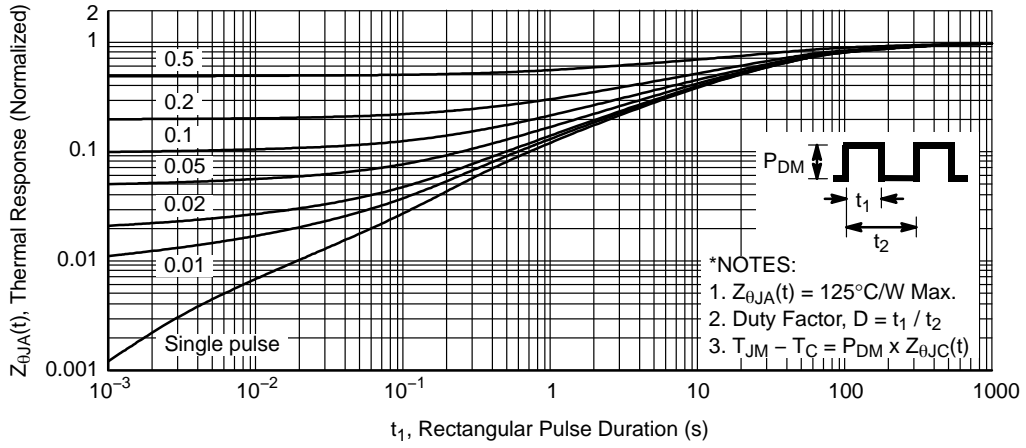


Figure 13. Transient Thermal Response Curve

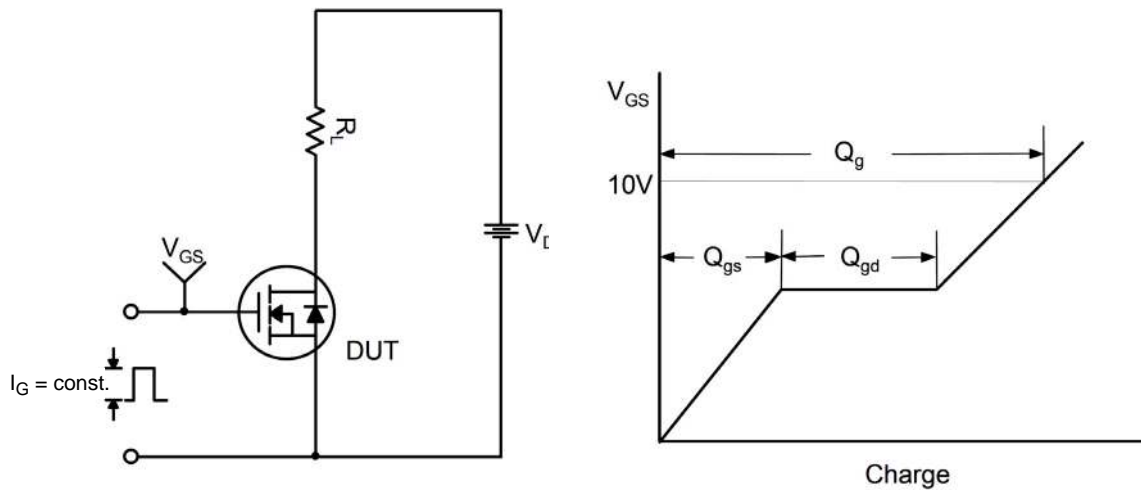


Figure 14. Gate Charge Test Circuit & Waveform

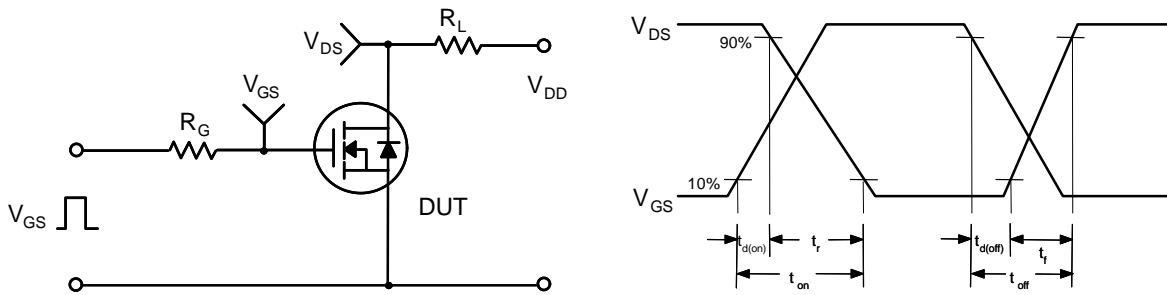


Figure 15. Resistive Switching Test Circuit & Waveforms

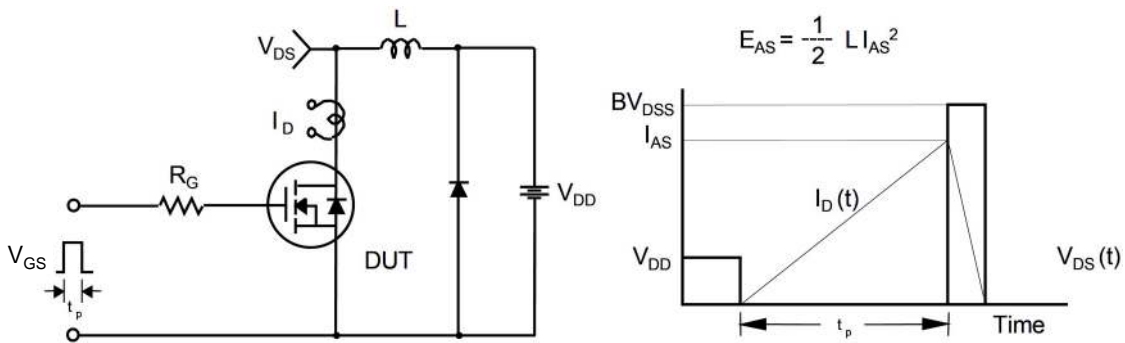


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

FDMS039N08B

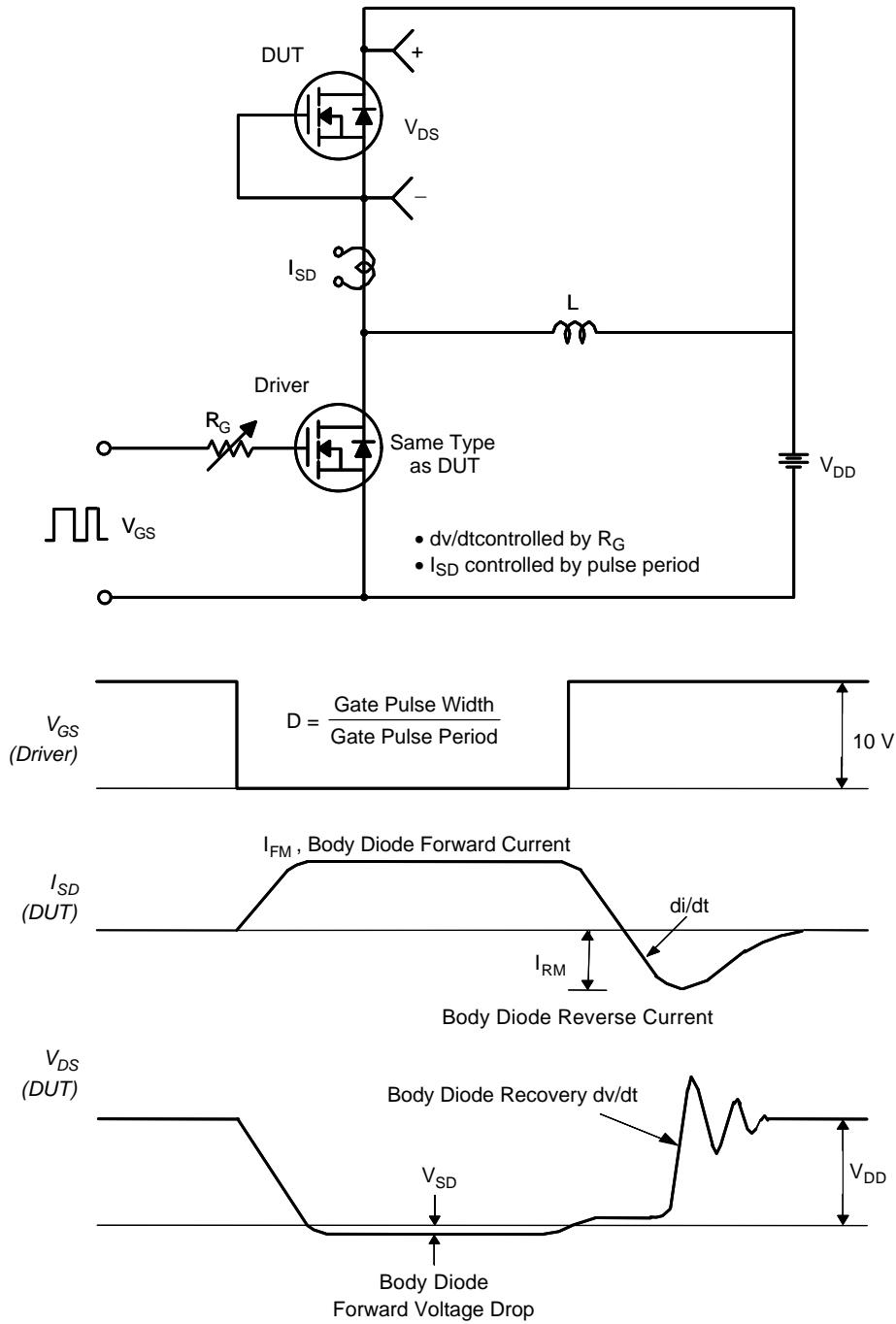


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

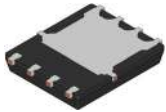
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMS039N08B	FDMS039N08B	PQFN8 5X6, 1.27P (Power 56) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

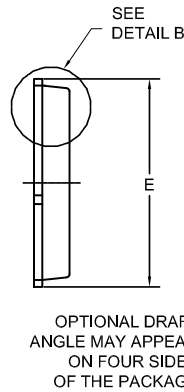
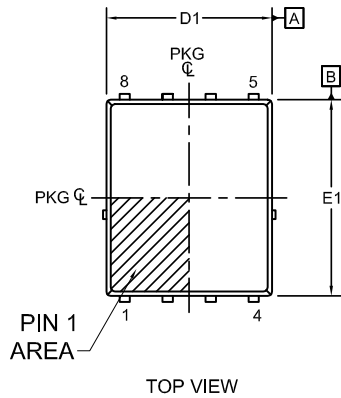
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



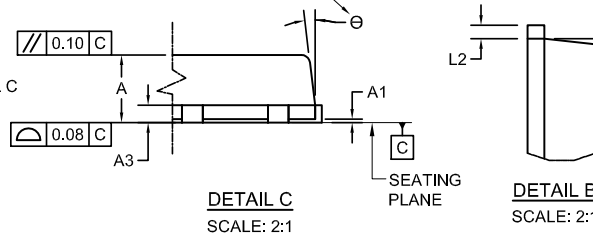
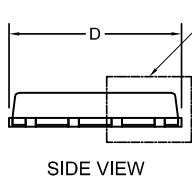
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

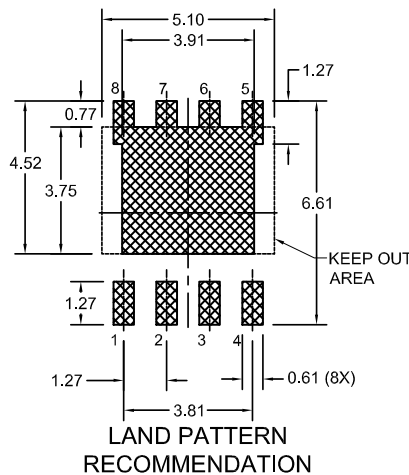
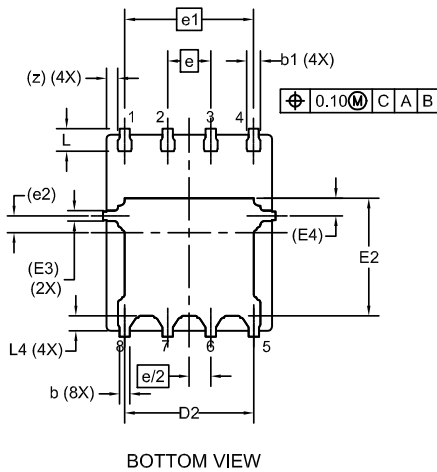


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 1

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