MP6539B

100V, Three-Phase BLDC Motor Pre-Driver

DESCRIPTION

The MP6539B is a gate driver IC designed for three-phase, brushless DC motor driver applications. The MP6539B is capable of driving three half-bridges consisting of six N-channel power MOSFETs up to 100V.

The MP6539B uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. An internal charge pump maintains the high-side gate drive if the output is held high for an extended period of time.

Internal safety features include shoot-through protection, adjustable dead-time control, under-voltage lockout (UVLO), and thermal shutdown.

The MP6539B is similar to the MP6539. It does not implement auto bootstrap charging, does not include over-current protection, and is powered only from the VDD pin (VIN and LDO have been removed).

The MP6539B is available in TSSOP-28 (9.7mmx6.4mm) and QFN-28 (4mmx5mm) packages with an exposed thermal pad.

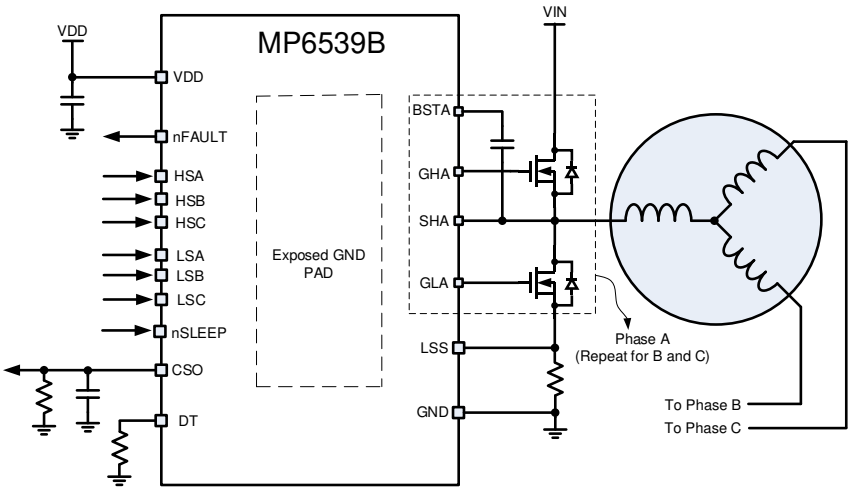
FEATURES

- Supports 100V Operation
- 120V V_{BST} Maximum Voltage
- Integrated Current-Sense Amplifier
- Low-Power Sleep Mode for Battery-Powered Applications
- Adjustable Dead-Time Control to Prevent Shoot-Through
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in Thermally Enhanced, Surface-Mounted TSSOP and QFN Packages

APPLICATIONS

- Three-Phase, Brushless DC Motors and Permanent Magnet Synchronous Motors
- Power Drills
- E-Bike

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MP6539BGV*	QFN-28 (4mmx5mm)	*See Below*
MP6539BGF**	TSSOP-28 EP (9.7mmx6.4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6539BGV–Z).
** For Tape & Reel, add suffix –Z (e.g. MP6539BGF–Z).

TOP MARKING (MP6539BGV)

MPSYWW
M6539B
LLLLLL

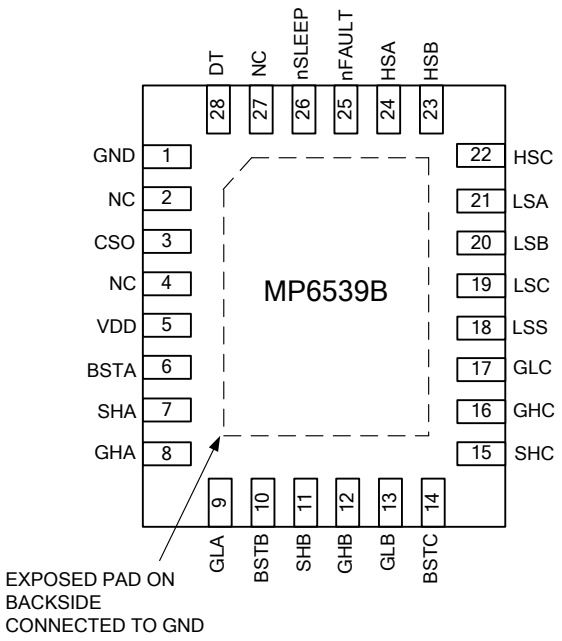
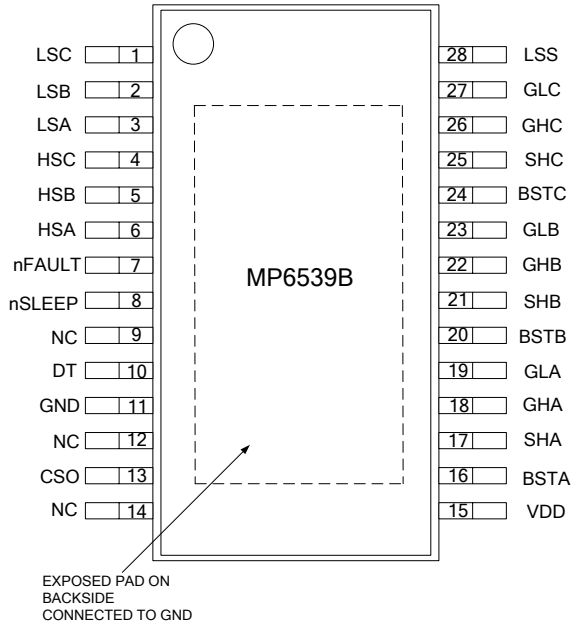
MPS: MPS prefix
Y: Year code
WW: Week code
M6539B: Part number
LLLLLL: Lot number

TOP MARKING (MP6539BGF)

MPSYYWW
MP6539B
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6539B: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-28 (4mmx5mm)	**TSSOP-28 EP (9.7mmx6.4mm)**

PIN FUNCTIONS

QFN28 Pin #	TSSOP Pin #	Name	Description
1	11	GND	**Ground.**
2	12	NC	**No connection.**
3	13	CSO	**Current sense output.** See text.
4	14	NC	**No connection.**
5	15	VDD	**Gate driver supply voltage.**
6	16	BSTA	**Bootstrap output phase A.**
7	17	SHA	**High-side source connection phase A.**
8	18	GHA	**High-side gate drive phase A.**
9	19	GLA	**Low-side gate drive phase A.**
10	20	BSTB	**Bootstrap output phase B.**
11	21	SHB	**High-side source connection phase B.**
12	22	GHB	**High-side gate drive phase B.**
13	23	GLB	**Low-side gate drive phase B.**
14	24	BSTC	**Bootstrap output phase C.**
15	25	SHC	**High-side source connection phase C.**
16	26	GHC	**High-side gate drive phase C.**
17	27	GLC	**Low-side gate drive phase C.**
18	28	LSS	**Low-side source connection.**
19	1	LSC	**Phase C low-side input pin.**
20	2	LSB	**Phase B low-side input pin.**
21	3	LSA	**Phase A low-side input pin.**
22	4	HSC	**Phase C high-side input pin.**
23	5	HSB	**Phase B high-side input pin.**
24	6	HSA	**Phase A high-side input pin.**
25	7	nFAULT	**Fault indication.** Open-drain output. Logic low when in a fault condition.
26	8	nSLEEP	**Sleep mode input.** Logic low to enter low-power sleep mode, high to enable. Internal pull down.
27	9	NC	**No connection.**
28	10	DT	**Dead-time setting.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (VDD) GLA/B/C .....-0.3V to 14.5V
BSTA/B/C .....-0.3V to 120V
GHA/B/C .....-0.3V to (BST - SH) + 0.3V
GHA/B/C (transient, 2µs) .....
…….....-8V to (BST - SH) + 0.3V
LSS .....-0.3V to 4V
LSS (transient, 2µs) .....-1V to 4V
SHA/B/C .....-5V to 110V
SHA/B/C (transient, 2µs) .....-8V to 110V
All other pins to GND .....-0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
QFN-28 (4mmx5mm)……3.1W
TSSOP-28 EP (9.7mmx6.4mm)……3.9W
Storage temperature..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

Recommended Operating Conditions (3)

Motor voltage (V_{IN}).....+8V to 100V
Input voltage (V_{DD}).....+8.5V to 14V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-28 (4mmx5mm)……	40	9....	°C/W
TSSOP-28 EP……	...32.....	6....	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Gate driver supply voltage	V_{DD}		8.5		14	V
Quiescent current	I_Q	nSLEEP = 1, not switching		1.1		mA
	I_{SLEEP}	nSLEEP = 0		2		µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 0.8V	-2.4		2.4	µA
	$I_{IN(L)}$	V_{IL} = 5V	-14		14	µA
nSLEEP pull-down resistance	$R_{SLEEP-PD}$			500		kΩ
Internal pull-down resistance	R_{PD}			500		kΩ
Fault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_O = 5mA			0.15	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuits						
VDD UVLO rising threshold	V_{DD_RUVLO}		6.5	7.5	8.5	V
VDD UVLO falling threshold	V_{DD_FUVLO}		6	6.8	7.6	V
VDD UVLO hysteresis	V_{DD_HYS}			500		mV
VBST UVLO threshold	V_{BST_UVLO}	Voltage between SHx and BSTx		6.2		V
SLEEP wake-up time	t_{SLEEP}			70		µs
Thermal shutdown	T_{TSD}			150		°C
Gate Drive						
Bootstrap diode forward voltage	V_{FBOOT}	I_D = 10mA			1.2	V
		I_D = 50mA			2.3	V
Maximum source current	I_{SOURCE}(5)			0.8		A
Maximum sink current	I_{SINK}(5)			1		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		7		Ω
HS gate drive pull-down resistance	R_{HS-DN}	V_{DS} = 1V	0.5		5.5	Ω
LS gate drive pull-down resistance	R_{LS-DN}	V_{DS} = 1V	0.5		5.5	Ω

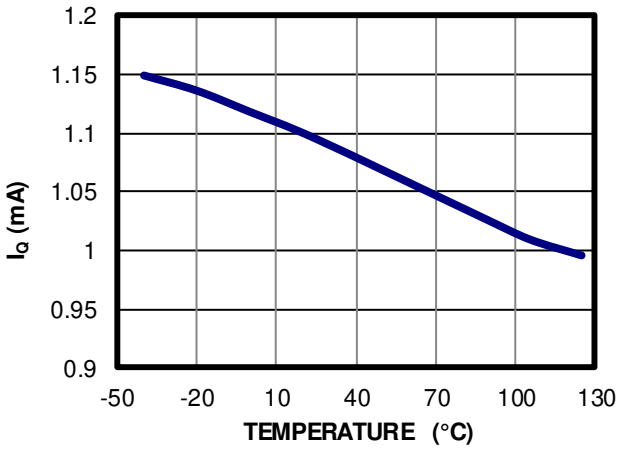
Note:

5) Guaranteed by design.

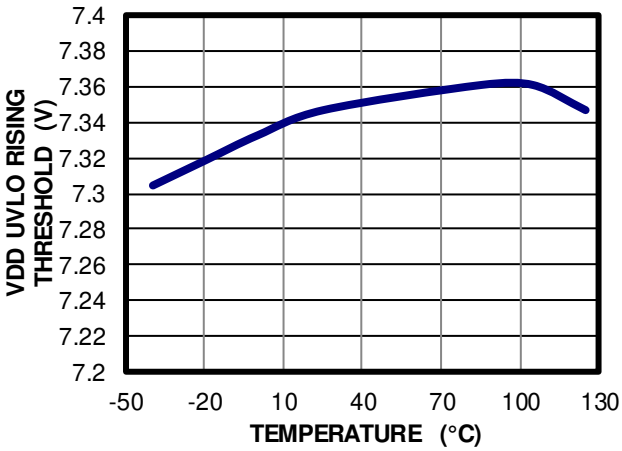
TYPICAL CHARACTERISTICS

Quiescent Current vs. Temperature

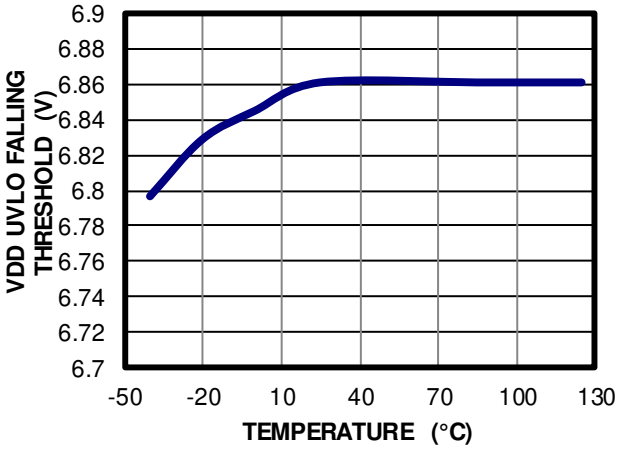
VDD = 12V



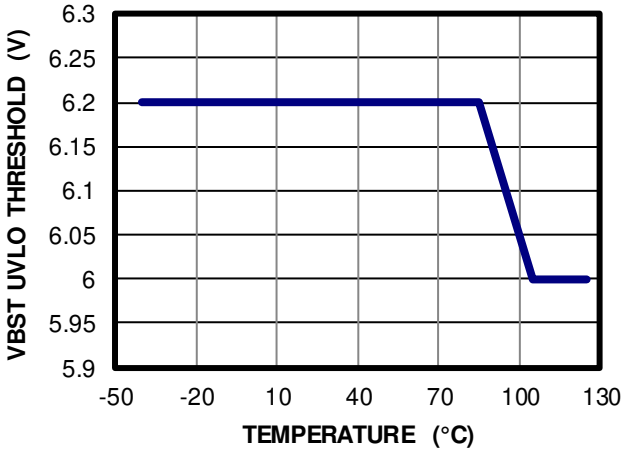
VDD UVLO Rising Threshold vs. Temperature



VDD UVLO Falling Threshold vs. Temperature



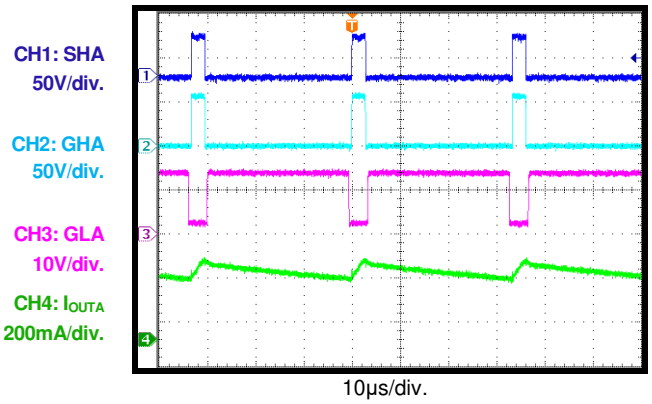
VBST UVLO Threshold vs. Temperature



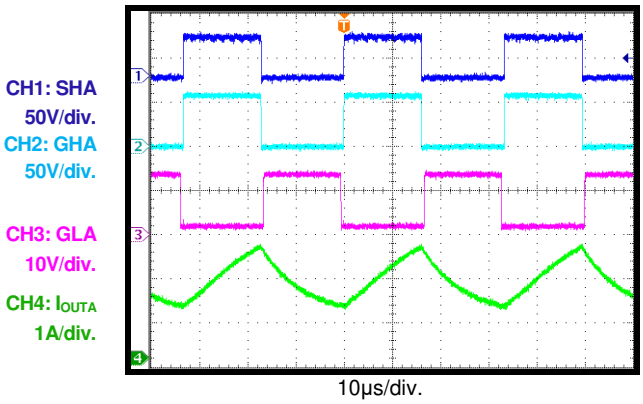
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{DD} = 12V, A-phase switching, B-phase LS on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

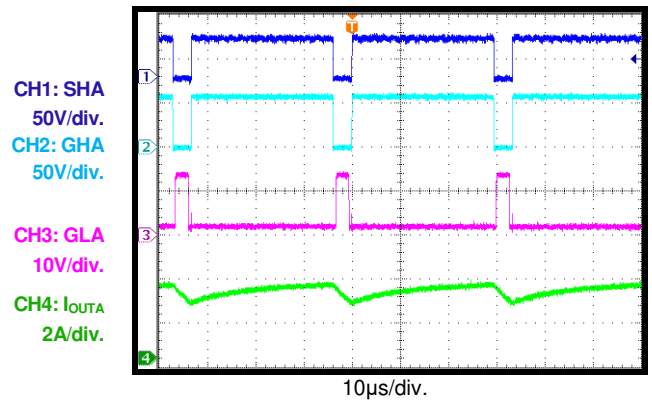
Steady State
Duty = 10%



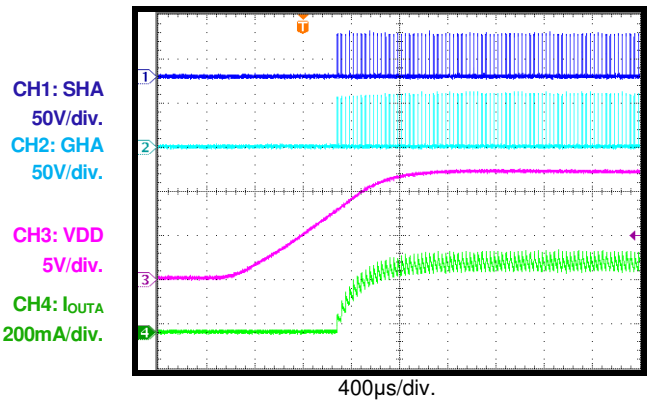
Steady State
Duty = 50%



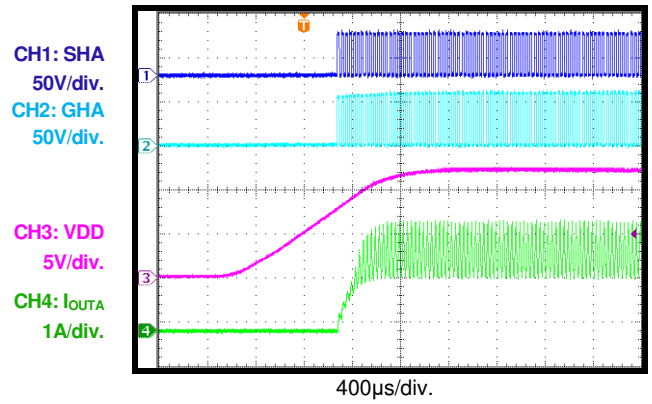
Steady State
Duty = 90%



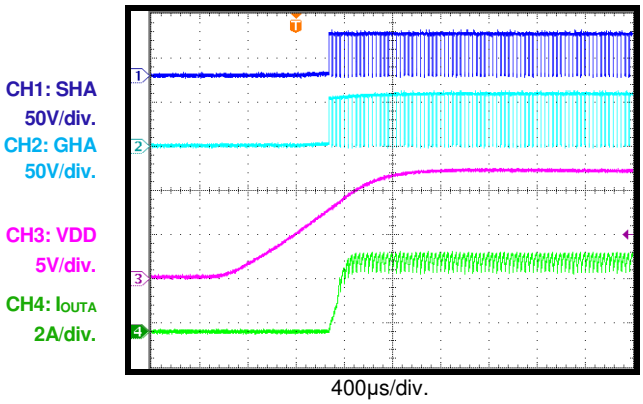
Power Ramp Up
Duty = 10%



Power Ramp Up
Duty = 50%



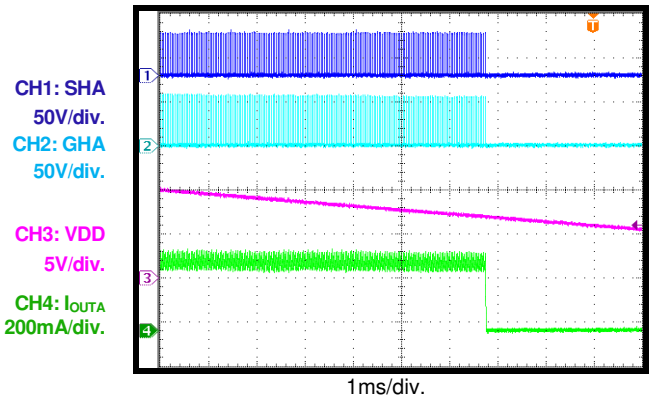
Power Ramp Up
Duty = 90%



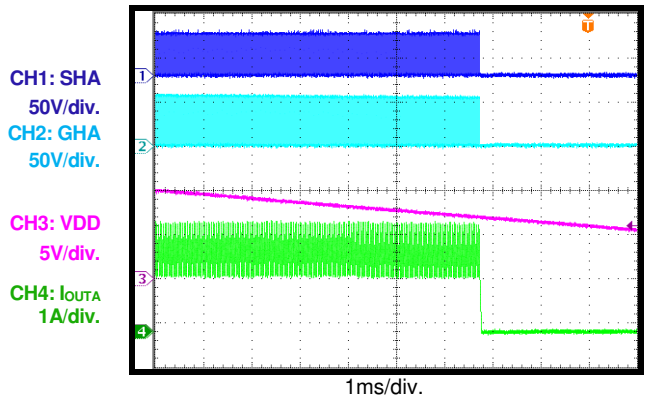
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{DD} = 12V, A-phase switching, B-phase LS on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

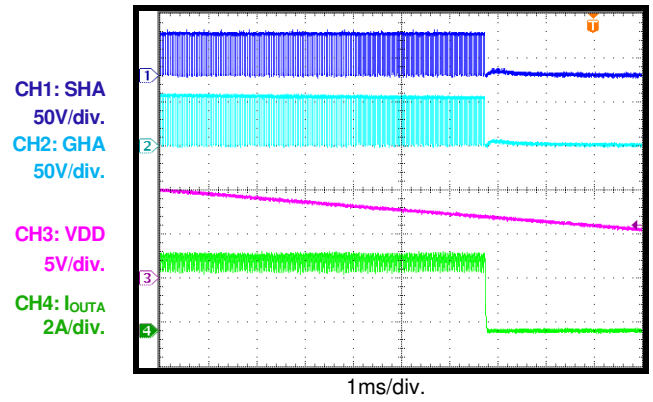
Power Ramp Down
Duty = 10%



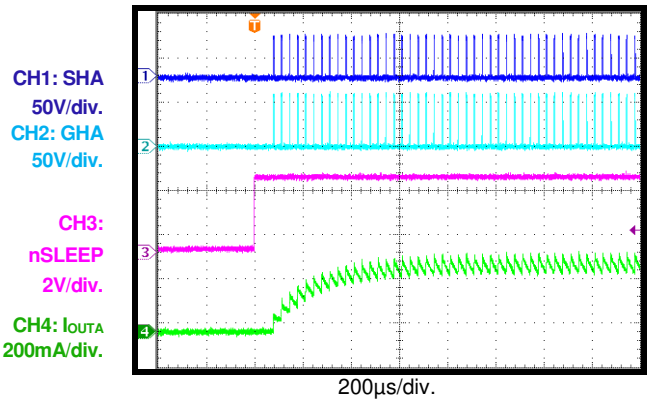
Power Ramp Down
Duty = 50%



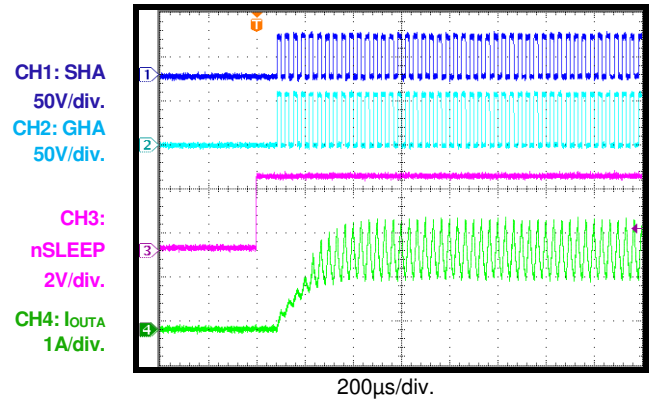
Power Ramp Down
Duty = 90%



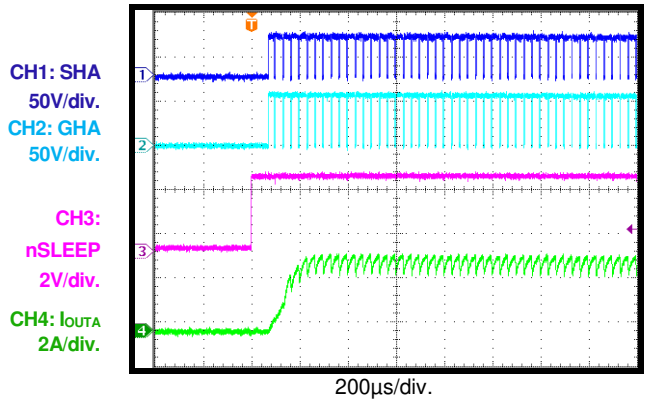
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



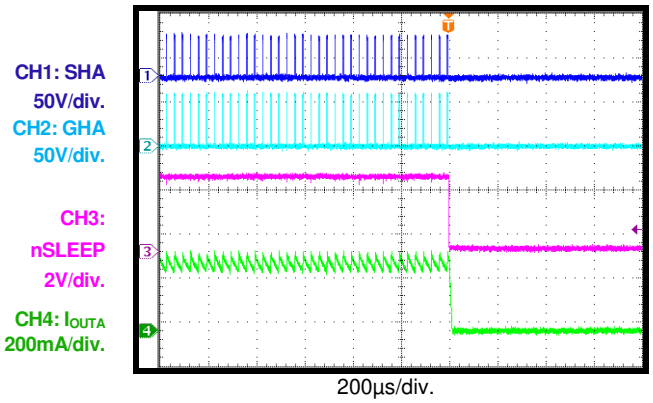
Sleep Recovery
Duty = 90%



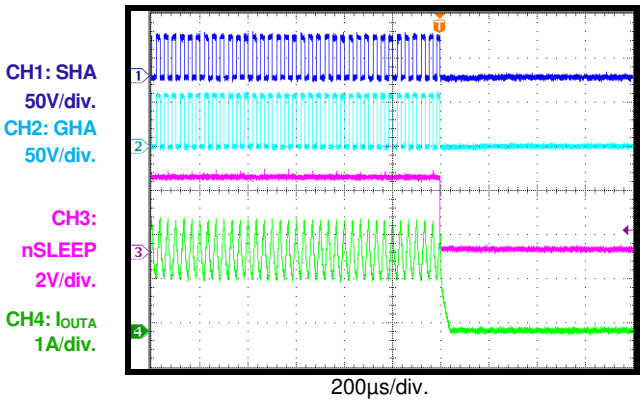
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{DD} = 12V, A-phase switching, B-phase LS on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

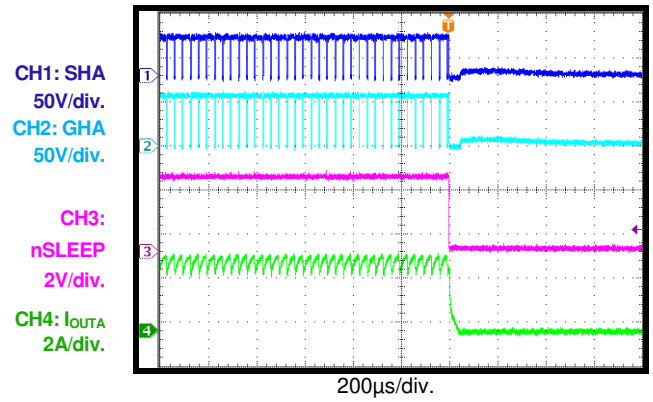
Sleep Entry
Duty = 10%



Sleep Entry
Duty = 50%



Sleep Entry
Duty = 90%



FUNCTIONAL BLOCK DIAGRAM

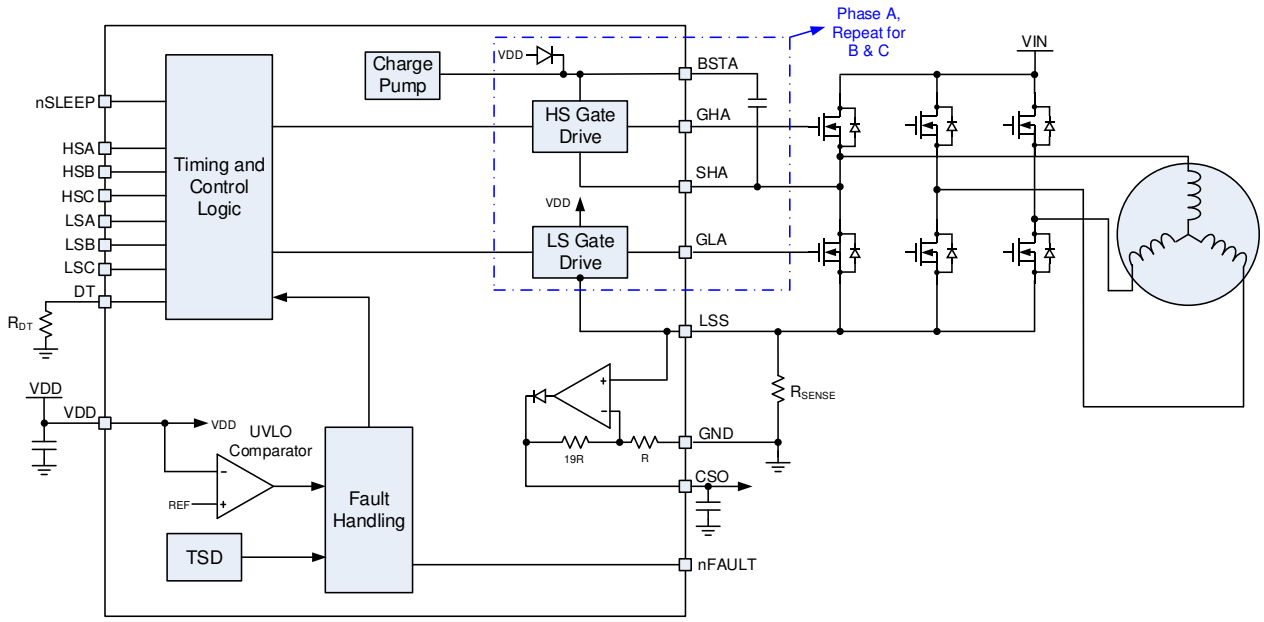


Figure 1: Functional Block Diagram

OPERATION

The MP6539B is a three-phase, BLDC motor pre-driver that can drive three half-bridges with a 0.8A source and 1A sink current capability. The MP6539B supports operation on motor supply voltage up to 100V. It also features a low-power sleep mode, which disables the device and draws very low supply current.

Power-Up

The power-up sequence is initiated by the application of voltage to VDD. To initiate power-up, VDD must be above the 7.5V VDD UVLO threshold.

It is recommended that each output be driven low to provide an initial charge of the bootstrap capacitors before driving an output high. The MP6539B does not perform this bootstrap charge automatically.

The power-up process takes approximately 70µs, after which the MP6539B responds to logic inputs and drives the outputs.

Input Logic

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 70µs must pass before issuing a pulse-width modulation (PWM) command to allow the internal circuitry time to stabilize.

HSx is used to control the gate driver for the high-side MOSFET (HS-FET) of each phase. LSx is used to control the gate driver for the low-side MOSFET (LS-FET). A positive dead time is enforced by the device to prevent shoot-through. If both HSx and LSx are driven high or low, neither MOSFET is driven (see Table 1).

Table 1: Input Logic Truth Table

LSx	HSx	SHx
H	H	High impedance
H	L	GND
L	H	VIN
L	L	High impedance

nFAULT

nFAULT reports to the system when a fault condition occurs, such as over-temperature protection (OTP). nFAULT is an open-drain output, and is driven low when a fault condition occurs. If the fault condition is released, nFAULT is pulled high by an external pull-up resistor.

Current-Sense Amplifier

An integrated current-sense amplifier amplifies the voltage on LSS (relative to GND) by a factor of 20. This voltage is the output to CSO.

The current-sense amplifier only sources current. A minimum 1nF external capacitor must be connected from CSO to ground for stability.

During the PWM on time, current flowing through the output MOSFETs also flows through the shared low-side current sense resistor, generating a voltage that is amplified by the current sense amplifier, which charges the external capacitor on CSO. During the PWM off time, current recirculates through the LS-FETs and does not pass through the sense resistor, so there is zero voltage across it. During this time, the capacitor discharges through the internal feedback resistor (approximately 450kΩ) as well as through any external resistor to ground. Select an external resistor and capacitor to provide a filter to hold the value of the current through the PWM off time. Any external resistor used should be 1kΩ or greater.

If the current sense amplifier is not used, connect LSS directly to ground.

Charge Pump and Bootstrap

Normally, the high-side gate-drive voltage is generated from bootstrap capacitors connected between SHx and BSTx. The bootstrap capacitor is charged whenever the LS-FET is turned on.

If the output is held high for a long period of time, the bootstrap capacitor discharges slowly. This eventually results in gate driver loss for the HS-FET. To prevent this, an internal charge pump generates a voltage to maintain the bootstrap capacitor charge.

The bootstrap voltage is monitored by an under-voltage detection circuit. If any bootstrap voltage falls below the VBST UVLO voltage, its associated high-side output is disabled. The VBST UVLO does not cause the nFAULT signal to be driven low.

Dead-Time Adjustment

To prevent shoot-through in any phase of the bridge, it is necessary to insert a dead time (t_{DEAD}) between a high-side or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead-time resistor (R_{DT}) between DT and ground using Equation (1):

$$t_{DEAD}(\mu s) = 0.044 * R_{DT}(k\Omega) + 0.1 \quad (1)$$

If DT is tied directly to GND, a 77ns internal minimum dead time is applied. Leave DT open to generate a 6µs dead time.

VDD UVLO Protection and Power-Off

If the voltage on VDD falls below the VDD UVLO threshold voltage, the outputs are disabled and the nFAULT signal is asserted. Operation resumes when VDD rises above the UVLO threshold.

When VDD passes below the UVLO threshold, the HS and LS outputs are driven low to turn off the MOSFETs. As VDD drops further, eventually the outputs become high-impedance. If it is possible for VDD to be turned off while the MOSFETs are still powered, it is recommended to add external pull-down resistors from the gate to source of the MOSFETs.

Thermal Shutdown

If the die temperature exceeds safe limits, the MP6539B disables all gate drive outputs, and nFAULT is driven active low. Operation resumes automatically once the die temperature falls to a safe level.

APPLICATION INFORMATION

Comparing the MP6539 and MP6539B

The MP6539B is similar to the MP6539, with the following changes:

1. The VIN pin and associated circuitry have been removed. Power is provided only through the VDD pin, which was previously the VREG pin.
2. The bootstrap auto-charge function at power-up has been removed, which reduces the power-up time to about 70µs.
3. Over-current protection and VDS sensing have been removed. The only protection circuits implemented are VDD UVLO, OTP, and VBST UVLO.
4. Since there is no VIN pin, when VDD drops to zero, the gate drive outputs become high-impedance.

Bootstrap Components

The primary source of charge to enable the HS-FETs is provided by the bootstrap capacitors. There are several considerations to be made when selecting the size of these capacitors.

When the output is driven low, the bootstrap capacitor is charged from VDD through an internal diode. To turn on the HS-FET, the charge in the bootstrap capacitor is transferred to the gate of the HS-FET to turn it on. If the bootstrap capacitor is too small, it will not contain enough charge to fully enhance the MOSFET.

The minimum acceptable bootstrap capacitor value depends on the total gate charge of the HS-FET Q_T, the internal boot diode voltage drop (V_{FBOOT}), and how much voltage drop can be tolerated from the VDD supply voltage (ΔV_{BOOT}) and still adequately enhance the MOSFET. This can be calculated with Equation (2):

$$C_{BOOT} \geq Q_T / (\Delta V_{BOOT} - V_{FBOOT}) \quad (2)$$

It is recommended to use a capacitor of between 2x and 4x this minimum value. It is also important to take into consideration the capacitance change under bias for ceramic capacitors.

For example, a MOSFET with a total gate charge Q_T of 50nC, a VDD voltage of 12V, and a minimum desired gate drive voltage of 10V would be calculated as:

$C_{BOOT} \geq 50nC / (12V - 10V - 1.2V)$, or 62nF. Therefore, a 100nF or 220nF capacitor would be a reasonable choice.

At the other extreme, if the bootstrap capacitor is too large, it will take a very long time to charge when the output is low, due to the limited current sourcing capability through the bootstrap diode. The total power dissipated in the boot diode can also be a concern.

Bootstrap Pre-Charge

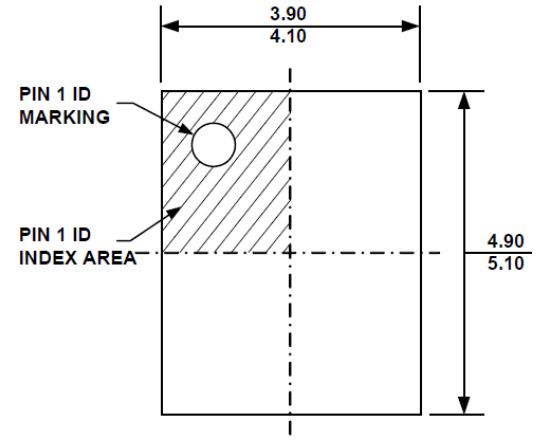
At power-up, and whenever the device has been disabled for some time, the bootstrap capacitors are discharged. Before attempting to drive an output high, the bootstrap capacitors should be pre-charged. This function is not performed automatically by the MP6539B.

Pre-charge is accomplished by turning on each LS-FET, one at a time. This allows current to flow from VDD through the internal bootstrap diode and the capacitor, and through the LS-FET.

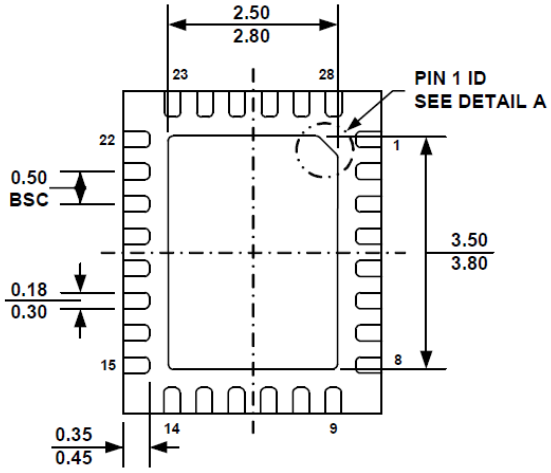
If large bootstrap capacitors (over 220nF) are used, the pre-charge should be done with multiple pulses at a 20% duty cycle to limit the amount of power dissipated in the bootstrap diodes.

PACKAGE INFORMATION

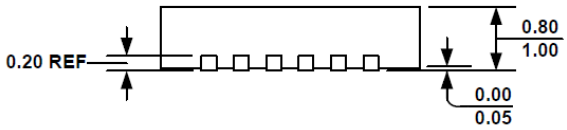
QFN-28 (4mmx5mm)



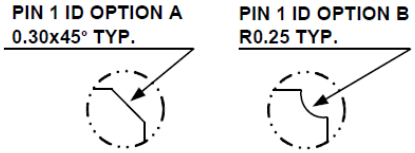
TOP VIEW



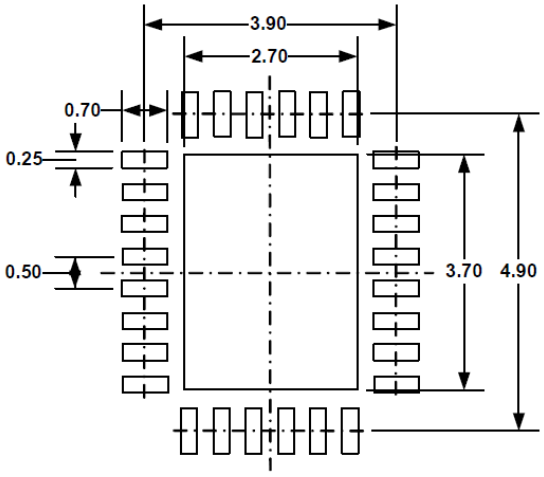
BOTTOM VIEW



SIDE VIEW



DETAIL A



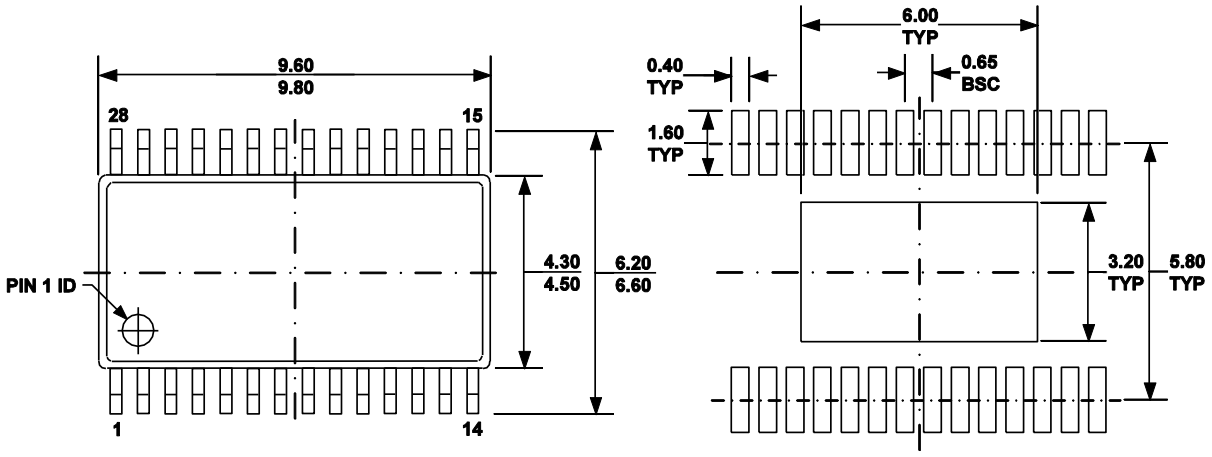
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

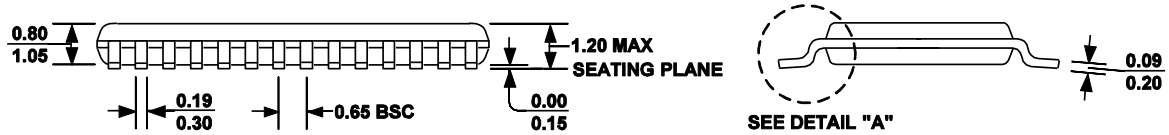
PACKAGE INFORMATION *(continued)*

TSSOP-28 EP



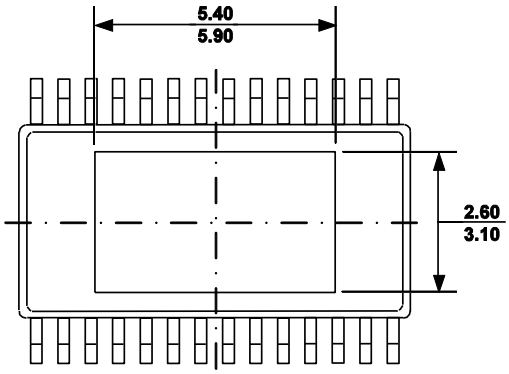
TOP VIEW

RECOMMENDED LAND PATTERN

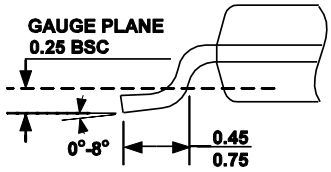


FRONT VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.