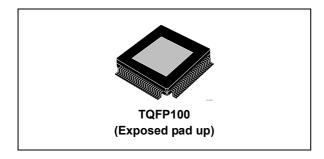


4 x 50 W PWM digital input power amplifier with built-in diagnostics features and low voltage operation

Data brief - production data



Features

- Integrated 108 dB D/A conversion
- I²S and TDM digital input (3.3/1.8 V)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- MOSFET power outputs
- EMI control for FM/AM compatibility
- EMI compliance at the CEI EN 55025 (2009-10)
- · Dithering possibility
- Very low external component count filter
- · Output lowpass filter included in the feedback
- Low radiation function (LRF)
- Max. output power
 - 4 x 50 W/4 Ω @ 15.2 V, 1 kHz
- · High output power capability
 - 28 W/4 Ω 10 % THD, Vd = 14.4 V
- Full I²C bus driving (3.3/1.8 V):
 - Independent front/rear soft play/ mute
 - I²C bus diagnostics (including DC and AC load detection, test signal internally generated)
- Very flexible fault detection though integrated diagnostic
- Offset detector (play or mute mode)
- Four independent short circuit protection
- Clipping detector

- C-MOS compatible enable pin (3.3/5 V)
- ESD protection
- 6 V operation ("Start Stop")

Description

The FDA450LV is a new BCD- SOI (silicon on insulation) technology QUAD BRIDGE class D amplifier, specially intended for car radio applications.

Thanks to the technology used, it is possible to integrate a high performance D/A converter together with powerful MOSFET outputs in class D, to get an outstanding efficiency compared with the standard class AB.

The integrated D/A converter allows to reach outstanding performances (110 dB S/N ratio with 108 dB of dynamic range). The feedback loop includes the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion independently of the inductor and capacitor quality.

FDA450LV is fully configurable through I²C bus interface and integrates a full diagnostics array specially intended for automotive applications.

Thanks to the solutions implemented to solve the EMI problems, the device is conceived to be used in the standard single DIN car-radio box together with the tuner.

The possibility to parallelize the outputs allows to drive both 2 Ω and 1 Ω speakers.

Moreover FDA450LV is able to work with power supply as low as 6 V, thus supporting the most recent low voltage ('start-stop') car-makers specification.

Table 1. Device summary

Order code	Package	Packing
FDA450LV	TQFP100 (exp. pad up)	Tray

Contents FDA450LV

Contents

1	Block diagram and pins description	3
2	Package information	6
3	Revision history	7



Block diagram and pins description

Figure 1. Block diagram CD/DIAG Enable 2 Enable 1 PLL Current Scrambler ch1 Transreristance Generators I2S-CLK I2S PWM Generators Transreristance ch2 Array Power Amplifier PWM Current Generators Array Power Amplifier PWM Scrambler Transreristance Generators ch4 Array 1611 1222 67 2711 6977 6577 50.85 55.6 Value of the control of the GAPGPS0049



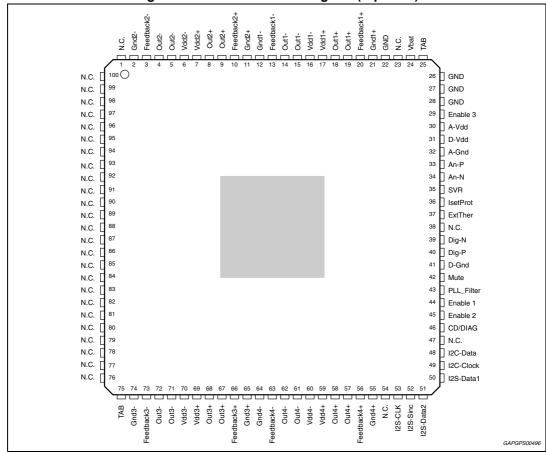




Table 2. Pins list description

N#	Pin	Function	
1	N.C.	Not connected	
2	Gnd2-	Channel 2, half bridge a Power Ground	
3	Feedback2-	Channel 2 half bridge a Feedback	
4	Out2-	Channel 2 half bridge a Output	
5	Out2-	Channel 2 half bridge a Output	
6	Vdd2-	Channel 2 half bridge a Power Supply	
7	Vdd2+	Channel 2 half bridge b Power Supply	
8	Out2+	Channel 2 half bridge b Output	
9	Out2+	Channel 2 half bridge b Output	
10	Feedback2+	Channel 2 half bridge b Feedback	
11	Gnd2+	Channel 2, half bridge b Power Ground	
12	Gnd1-	Channel 1, half bridge a Power Ground	
13	Feedback1-	Channel 1 half bridge a Feedback	
14	Out1-	Channel 1 half bridge a Output	
15	Out1-	Channel 1 half bridge a Output	
16	Vdd1-	Channel 1 half bridge a Power Supply	
17	Vdd1+	Channel 1 half bridge b Power Supply	
18	Out1+	Channel 1 half bridge b Output	
19	Out1+	Channel 1 half bridge b Output	
20	Feedback1+	Channel 1 half bridge b Feedback	
21	Gnd1+	Channel 1, half bridge b Power Ground	
22	Gnd	Ground	
23	N.C.	Not connected	
24	Vbat	Power supply	
25	TAB	-	
26	GND	Ground	
27	GND	Ground	
28	GND	Ground	
29	Enable 3	Chip Enable 3	
30	A-Vdd	Analog Power Supply	
31	D-Vdd	Digital Power Supply	
32	A-Gnd	Analog Ground	
33	An-P	Positive Analog Supply V(svr)+1.65 (Internally generated)	
34	An-N	Negative Analog Supply V(svr)-1.65 (Internally generated)	
35	SVR	Supply Voltage Ripple Rejection Capacitor	
36	IsetProt	Current Protection Resistor Setting	
37	ExtTher	External Thermal Protection Input	
38	N.C.	Not connected	
39	Dig-N	Negative Digital Supply V(svr)-1.65 (Internally generated)	



Table 2. Pins list description (continued)

	Table 2. Pins list description (continued)				
N#	Pin	Function			
40	Dig-P	Positive Digital Supply V(svr)+1.65 (Internally generated)			
41	D-Gnd	Digital Ground			
42	Mute	Mute Input (10uA source current)			
43	PLL_Filter	PLL Filter Network			
44	Enable 1	Chip Enable 1			
45	Enable 2	Chip Enable 2			
		Clip detector and diagnostic output:			
46	CD/DIAG	Overcurrent protection intervention			
		Thermal warning			
		Offset detection			
47	N.C.	Not connected			
48	I2C-Data	I2C Data Input			
49	I2C-Clock	I2C Data Clock			
50	I2S-Data1	I2S/TDM Data 1 Input			
51	I2S Data 2	I2S/TDM Data 2 Input			
52	I2S-Sinc	I2S/TDM Sinc Input			
53	I2S-CLK	I2S/TDM Clock Input			
54	N.C.	Not connected			
55	Gnd4+	Channel 4, half bridge + Power Ground			
56	Feedback4+	Channel 4 half bridge + Feedback			
57	Out4+	Channel 4 half bridge + Output			
58	Out4+	Channel 4 half bridge + Output			
59	Vdd4+	Channel 4 half bridge + Power Supply			
60	Vdd4-	Channel 4 half bridge - Power Supply			
61	Out4-	Channel 4 half bridge - Output			
62	Out4-	Channel 4 half bridge - Output			
63	Feedback4-	Channel 4 half bridge - Feedback			
64	Gnd4-	Channel 4, half bridge - Power Ground			
65	Gnd3+	Channel 3, half bridge + Power Ground			
66	Feedback3+	Channel 3 half bridge + Feedback			
67	Out3+	Channel 3 half bridge + Output			
68	Out3+	Channel 3 half bridge + Output			
69	Vdd3+	Channel 3 half bridge + Power Supply			
70	Vdd3-	Channel 3 half bridge - Power Supply			
71	Ou3-	Channel 3 half bridge - Output			
72	Out3-	Channel 3 half bridge - Output			
73	Feedback3-	Channel 3 half bridge - Feedback			
74	Gnd3-	Channel 3, half bridge - Power Ground			
75	TAB	-			
76 to 100	N.C.	Not connected			



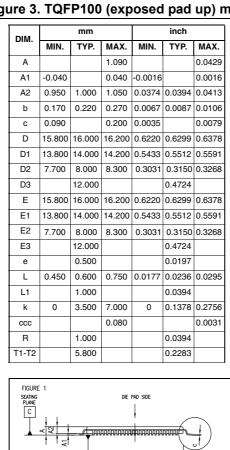
Package information FDA450LV

2 Package information

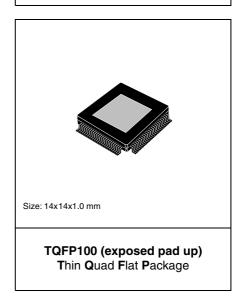
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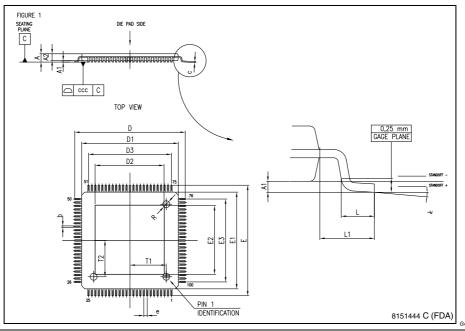
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Figure 3. TQFP100 (exposed pad up) mechanical data and package dimensions



OUTLINE AND MECHANICAL DATA





577

FDA450LV Revision history

3 Revision history

Table 3. Document revision history

Date	Revision	Changes
18-Jul-2013	1	Initial release.
18-Sep-2013	2	Updated Disclaimer.

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