CD4042B Types

CMOS
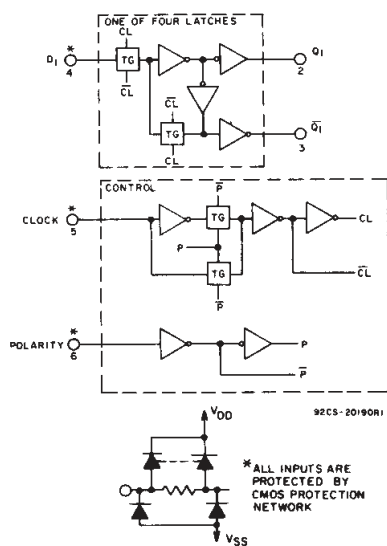## Quad Clocked "D" Latch
High-Voltage Types (20-Volt Rating)

■ CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (D, DR, DT, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).
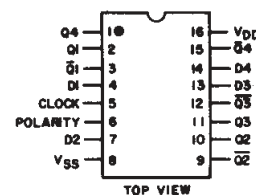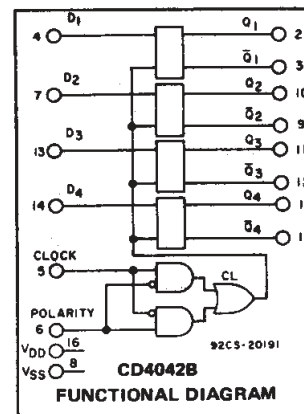
Features:
- Clock polarity control
- Q and $\overline{Q}$ outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:
- Buffer storage
- Holding register
- General digital logic

CD4042B
FUNCTIONAL DIAGRAM

TOP VIEW

TERMINAL ASSIGNMENT

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

CLOCK	POLARITY	Q
0	0	D
⤒	0	LATCH
1	1	D
⤓	1	LATCH

Fig. 1 – Logic block diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	±10^{-5}	±0.1	μA

CD4042B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = -55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

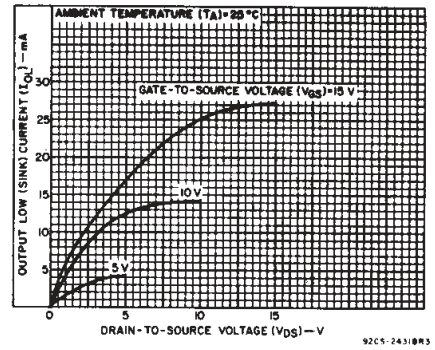| CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A=Full Package Temperature Range)	–	3	18	V
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	60	–	
Setup Time, t_S	5	50	–	ns
	10	30	–	
	15	25	–	
Hold Time, t_H	5	120	–	ns
	10	60	–	
	15	50	–	
Clock Rise or Fall Time: t_r , t_f	5,10 15	Not rise or fall time sensitive.		µS

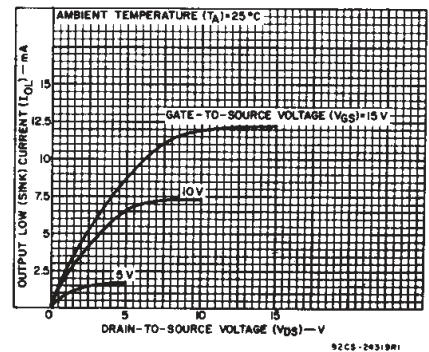Fig. 2 – Typical output low (sink) current characteristics.

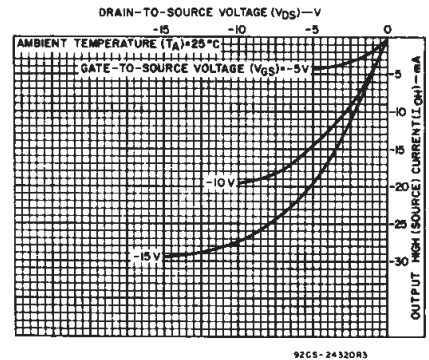Fig. 3 – Minimum output low (sink) current characteristics.

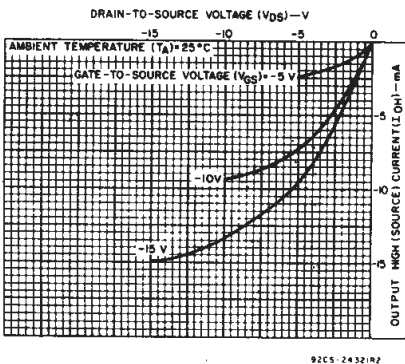Fig. 4 – Typical output high (source) current characteristics.

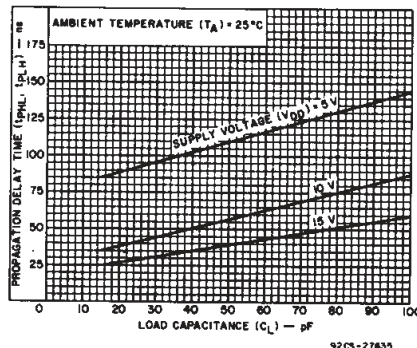Fig. 5 – Minimum output high (source) current characteristics.

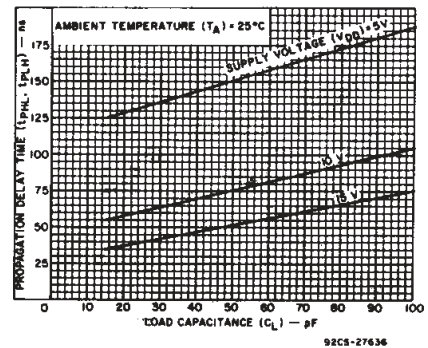Fig. 6 – Typical propagation delay time vs. load capacitance—data to Q.

Fig. 7 – Typical propagation delay time vs. load capacitance—data to $\overline{Q}$.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ

| CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	110	220	ns
	10	55	110	
	15	40	80	
Data In to $\overline{Q}$	5	150	300	ns
	10	75	150	
	15	50	100	
Clock to Q	5	225	450	ns
	10	100	200	
	15	80	160	
Clock to $\overline{Q}$	5	250	500	ns
	10	115	230	
	15	90	180	
Transition Time : t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum Clock Pulse Width, t_W	5	100	200	ns
	10	50	100	
	15	30	60	
Minimum Hold Time, t_H	5	60	120	ns
	10	30	60	
	15	25	50	
Minimum Setup Time, t_S	5	0	50	ns
	10	0	30	
	15	0	25	
Clock Input Rise or Fall Time: t_r, t_f	5,10 15	Not rise or fall time sensitive.		μS
Input Capacitance, C_{IN} Polarity Input	–	5	7.5	pF
All Other Inputs	–	7.5	15	pF
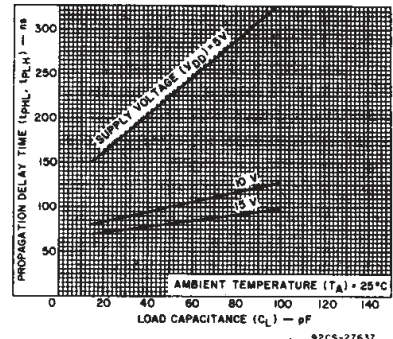
Fig. 8 – Typical propagation delay time vs. load capacitance—clock to Q
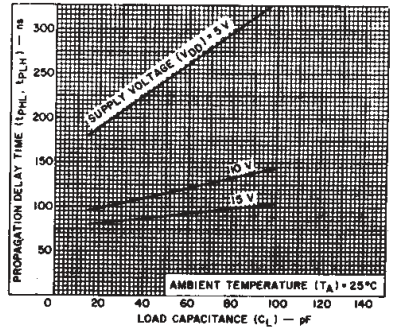
Fig. 9 – Typical propagation delay time vs. load capacitance—clock to $\overline{Q}$.

Fig. 12 – Dynamic test parameters.
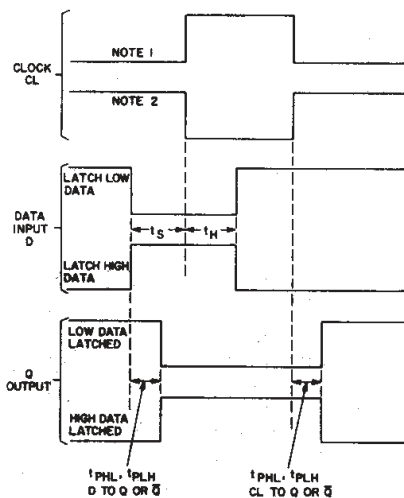
NOTES:
1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.
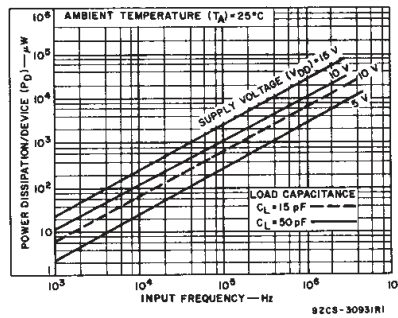
Fig. 10 – Typical power dissipation vs. frequency.
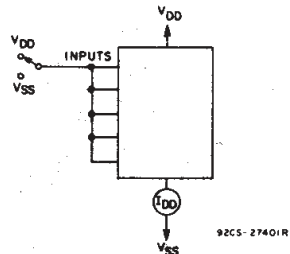
Fig. 13 – Quiescent device current test circuit.
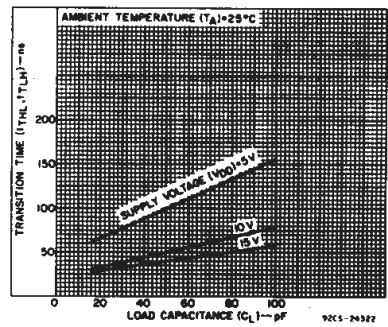
Fig. 11 – Typical transition time vs. load capacitance.

NOTE: TEST ANY COMBINATION OF INPUTS
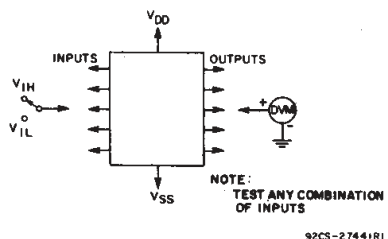
Fig. 14 – Input voltage test circuit.
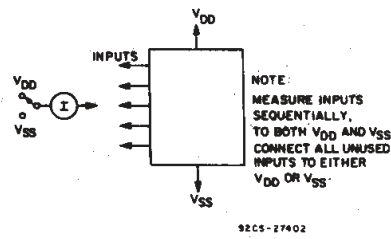
Fig. 15 — Input current test circuit.

92CS-27402

Chip Dimensions and Pad Layout

92CS-35071
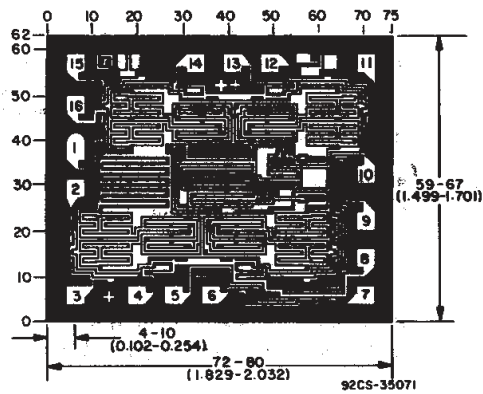
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COMMERCIAL CMOS
HIGH VOLTAGE ICs

3
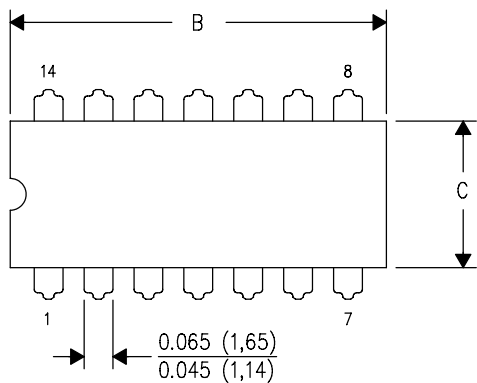
DIM ＼ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. This package is hermetically sealed with a ceramic lid using glass frit.
           D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
           E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002
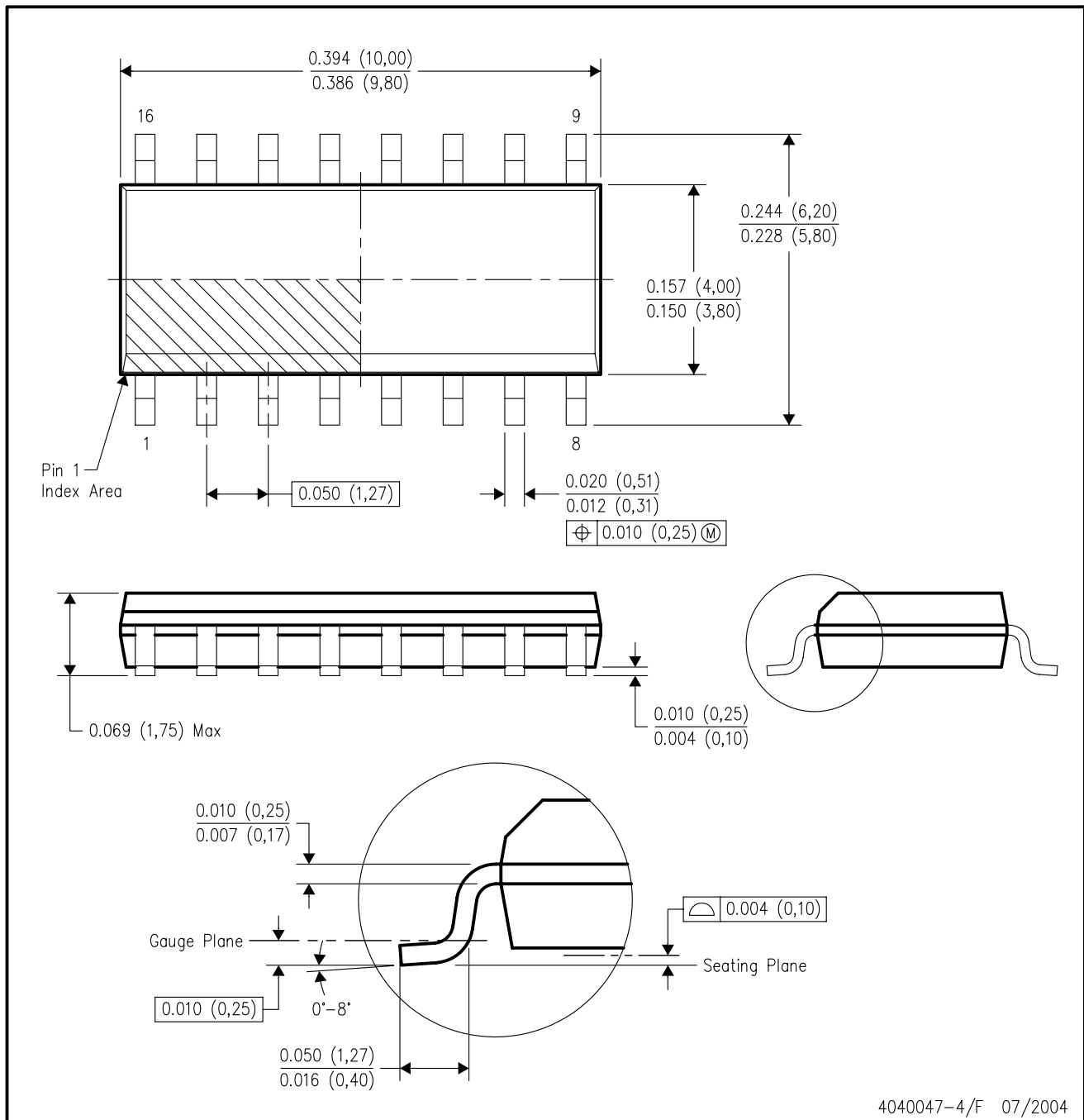
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)   **PLASTIC SMALL−OUTLINE PACKAGE**

0.394 (10,00)
0.386 (9,80)

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F 07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−012 variation AC.

DW (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

Pin 1
Index Area

1   8

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

⌂ | 0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
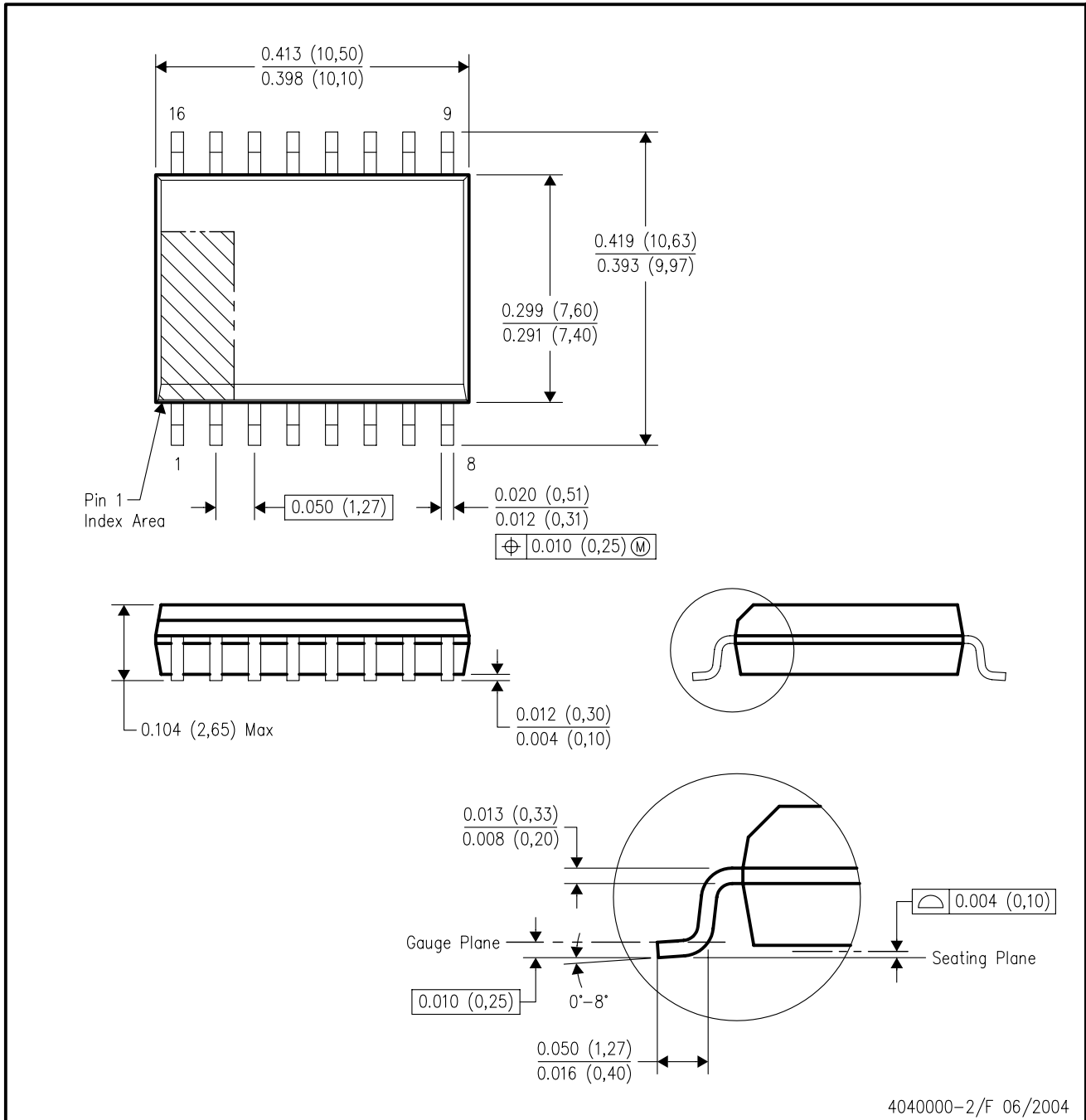
4040000−2/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AA.

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NS (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

1,27

0,51
0,35

⊕ 0,25 Ⓜ

14   8

5,60
5,00

8,20
7,40

1   7

A

0,15 NOM

Gage Plane

0°–10°

0,25

1,05
0,55

0,15
0,05

2,00 MAX

Seating Plane

◻ 0,10

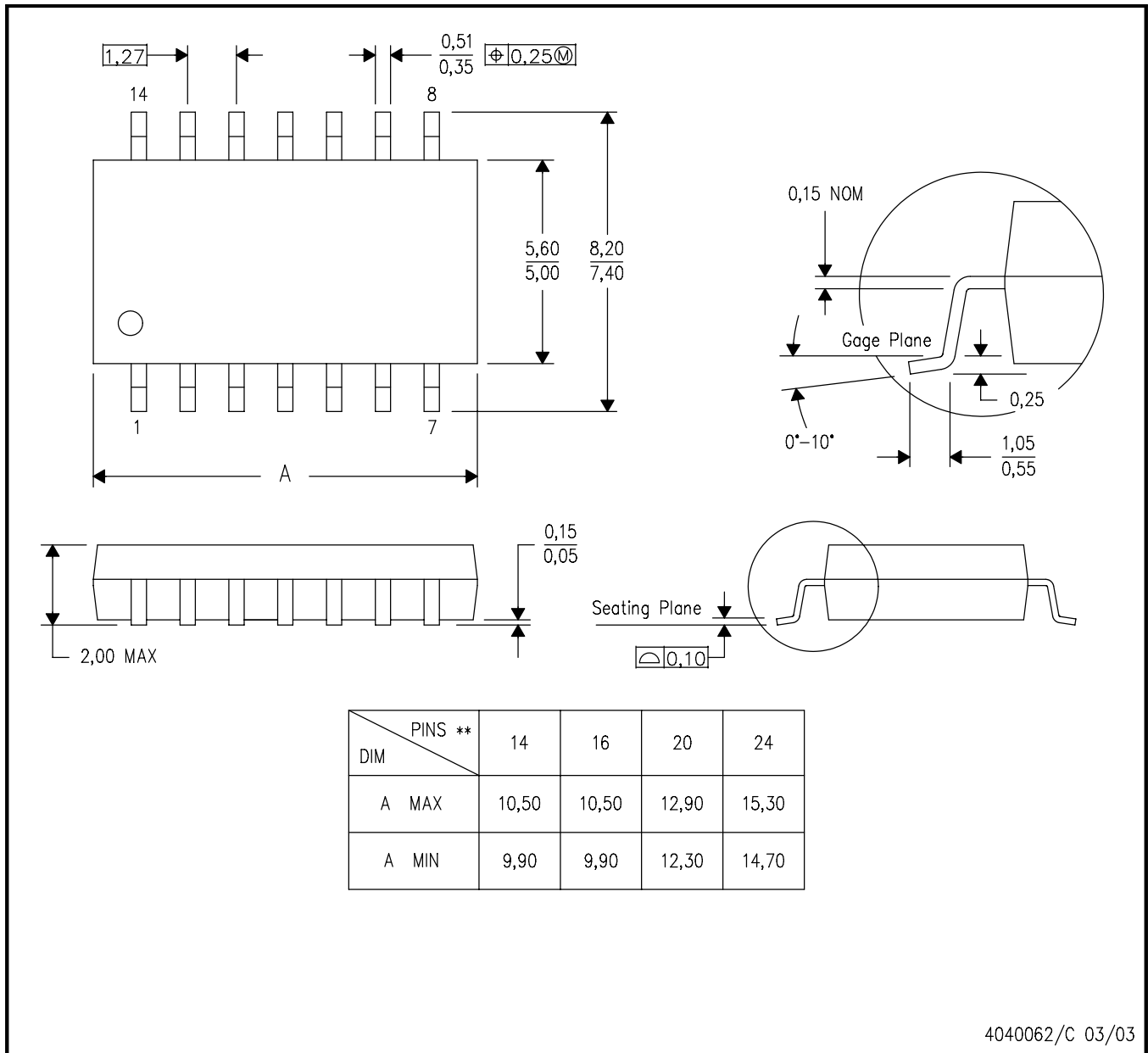| DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

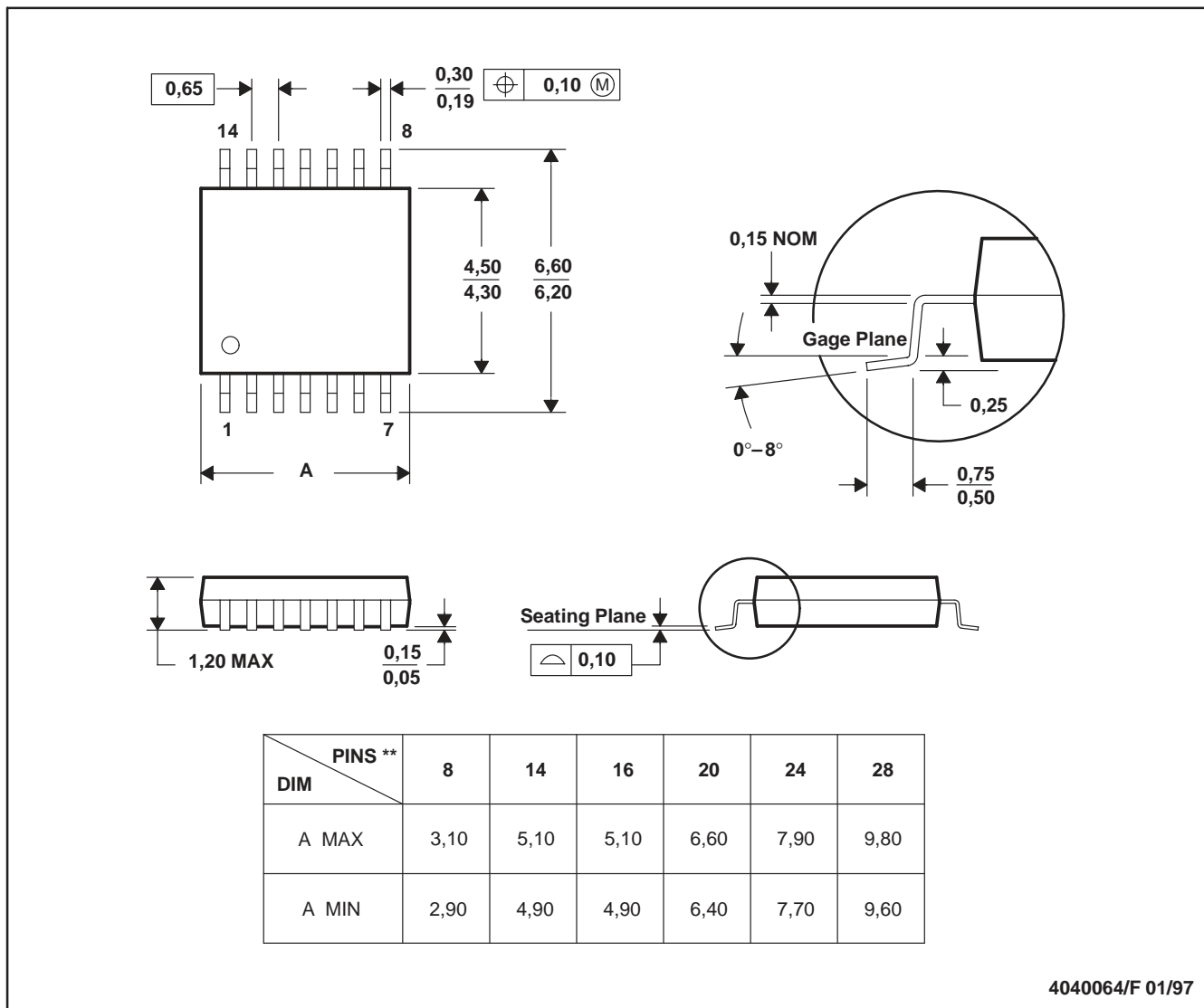|	PINS **	8	14	16	20	24	28
DIM							
A MAX		3,10	5,10	5,10	6,60	7,90	9,80
A MIN		2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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