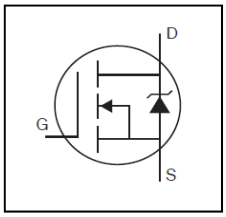
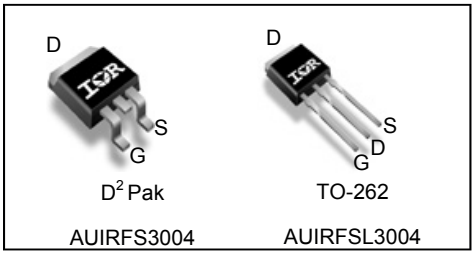
# AUIRFS3004
# AUIRFSL3004

HEXFET® Power MOSFET

### Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *




| | |
|---|---|
| $V_{DSS}$ | 40V |
| $R_{DS(on)}$ typ. | 1.4mΩ |
| max. | 1.75mΩ |
| $I_D$ (Silicon Limited) | 340A① |
| $I_D$ (Package Limited) | 195A |




| G | D | S |
|---|---|---|
| Gate | Drain | Source |

### Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| AUIRFSL3004 | TO-262 | Tube | 50 | AUIRFSL3004 |
| AUIRFS3004 | $D^2$-Pak | Tube | 50 | AUIRFS3004 |
| | | Tape and Reel Left | 800 | AUIRFS3004TRL |

### Absolute Maximum Ratings
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 340① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 240① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited) | 195 | |
| $I_{DM}$ | Pulsed Drain Current ② | 1310 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 380 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| dv/dt | Peak Diode Recovery ④ | 4.4 | V/ns |
| $E_{AS}$ | Single Pulse Avalanche Energy (Thermally Limited) ③ | 300 | mJ |
| $I_{AR}$ | Avalanche Current ② | See Fig.14,15, 22a, 22b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

### Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑨⑩ | — | 0.40 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount), $D^2$ Pak⑧ | — | 40 | |

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*Qualification standards can be found at www.infineon.com

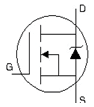
**Static @ $T_J$ = 25°C (unless otherwise specified)**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.037 | — | V/°C | Reference to 25°C, $I_D$ = 5mA ② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 1.4 | 1.75 | mΩ | $V_{GS}$ = 10V, $I_D$ = 195A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| gfs | Forward Trans conductance | 1170 | — | — | S | $V_{DS}$ = 10V, $I_D$ = 195A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 40V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 40V,$V_{GS}$ = 0V,$T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Internal Gate Resistance | — | 2.2 | — | Ω | |

**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| | | | | | | |
|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge | — | 160 | 240 | nC | $I_D$ = 187A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 40 | — | | $V_{DS}$ = 20V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | 68 | — | | $V_{GS}$ = 10V⑤ |
| $Q_{sync}$ | Total Gate Charge Sync. ($Q_g$ - $Q_{gd}$) | — | 92 | — | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | 23 | — | ns | $V_{DD}$ = 26V |
| $t_r$ | Rise Time | — | 220 | — | | $I_D$ = 195A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 90 | — | | $R_G$= 2.7Ω |
| $t_f$ | Fall Time | — | 130 | — | | $V_{GS}$ = 10V⑤ |
| $C_{iss}$ | Input Capacitance | — | 9200 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 2020 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 1340 | — | | $f$ = 1.0MHz, See Fig. 5 |
| $C_{oss\ eff.(ER)}$ | Effective Output Capacitance (Energy Related) | — | 2440 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 32V⑦ |
| $C_{oss\ eff.(TR)}$ | Effective Output Capacitance (Time Related) | — | 2690 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 32V⑥ |

**Diode Characteristics**

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 340① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ② | — | — | 1310 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C,$I_S$ = 195A,$V_{GS}$ = 0V ⑤ |
| $t_{rr}$ | Reverse Recovery Time | — | 27 | — | ns | $T_J$ = 25°C $V_{DD}$ = 34V |
| | | — | 31 | — | | $T_J$ = 125°C $I_F$ = 195A, |
| $Q_{rr}$ | Reverse Recovery Charge | — | 18 | — | nC | $T_J$ = 25°C di/dt = 100A/µs ⑤ |
| | | — | 41 | — | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | — | 1.2 | — | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.016mH, $R_G$ = 25Ω, $I_{AS}$ = 195A, $V_{GS}$ =10V. Part not recommended for use above this value.

④ $I_{SD}$ ≤ 195A, di/dt ≤ 930A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑨ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑩ $R_{\theta JC}$ value shown is at time zero

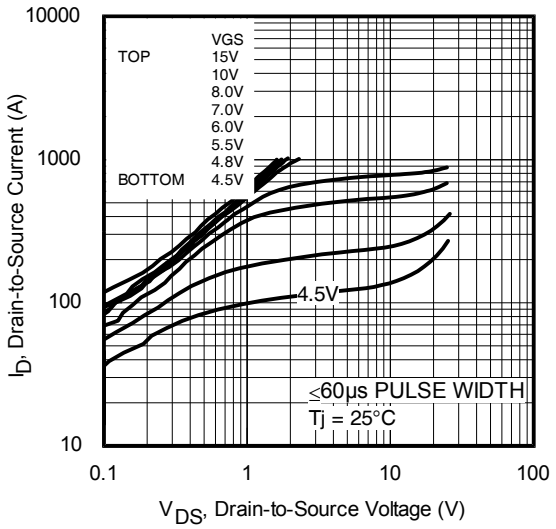



**Fig. 1** Typical Output Characteristics

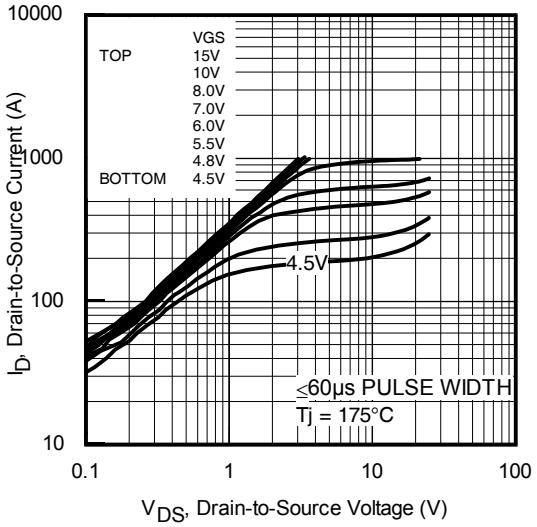



**Fig. 2** Typical Output Characteristics

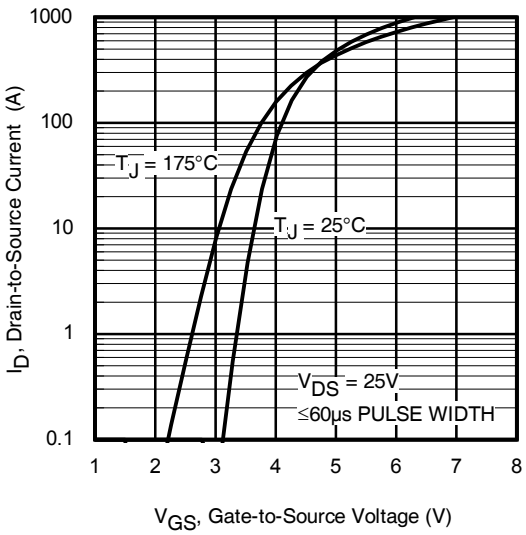



**Fig. 3** Typical Transfer Characteristics

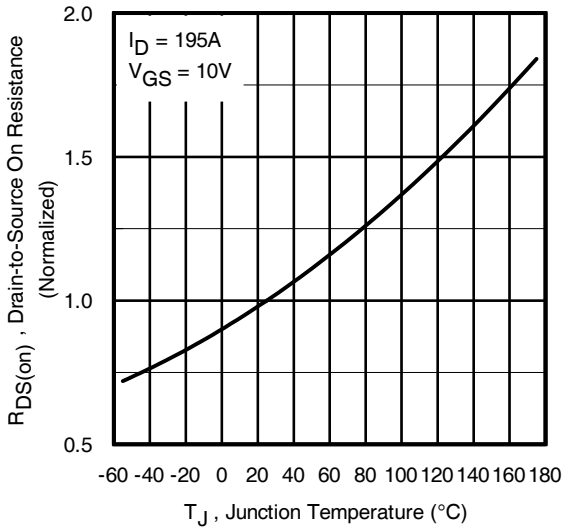



**Fig. 4** Normalized On-Resistance vs. Temperature

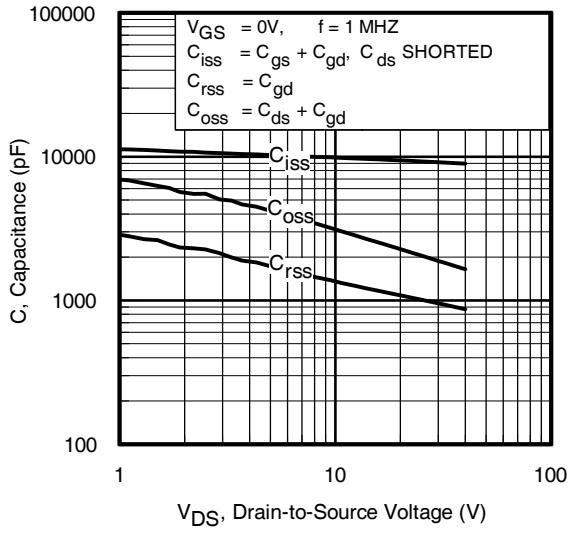



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

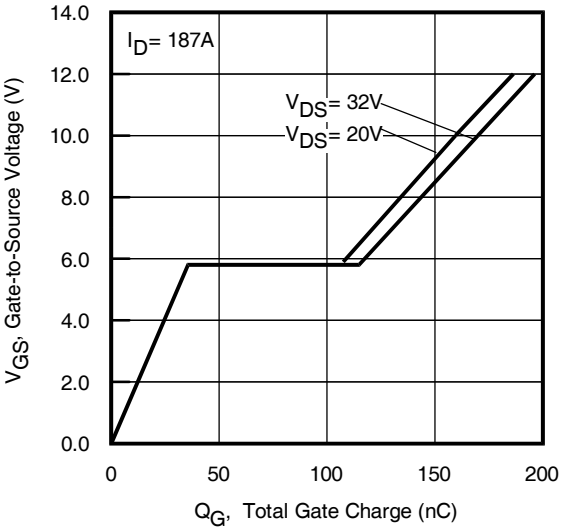



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

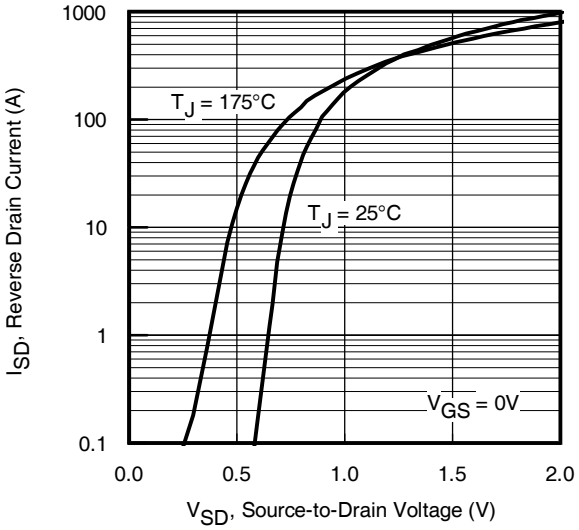



**Fig. 7** Typical Source-to-Drain Diode

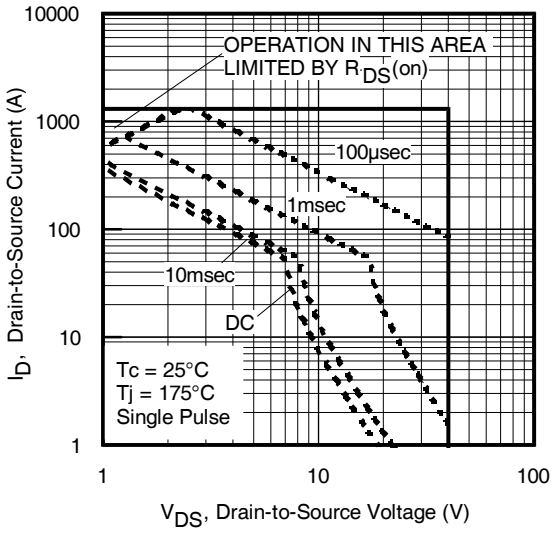



**Fig 8.** Maximum Safe Operating Area

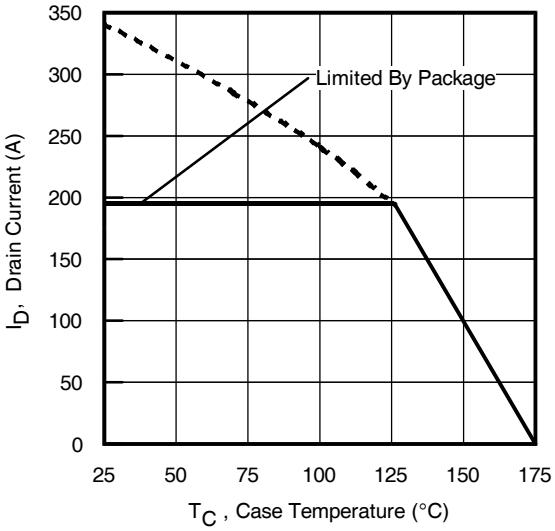



**Fig 9.** Maximum Drain Current vs. Case Temperature

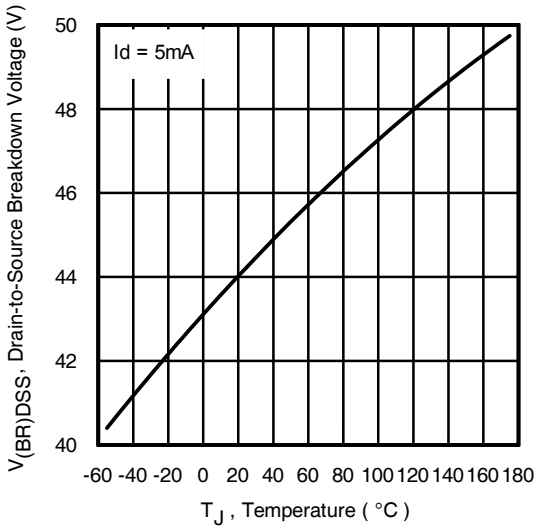



**Fig 10.** Drain-to-Source Breakdown Voltage

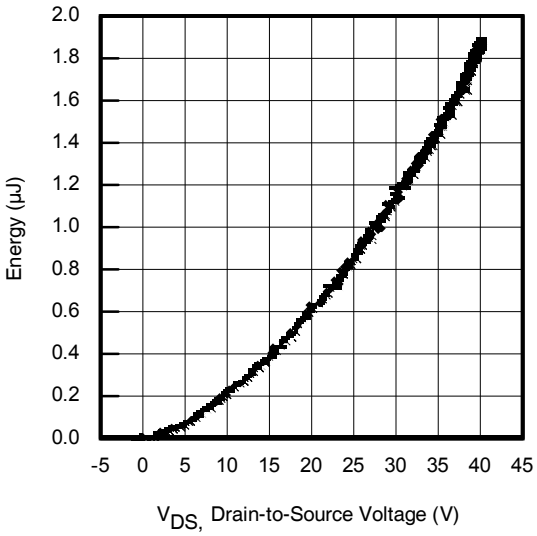



**Fig 11.** Typical Coss Stored Energy

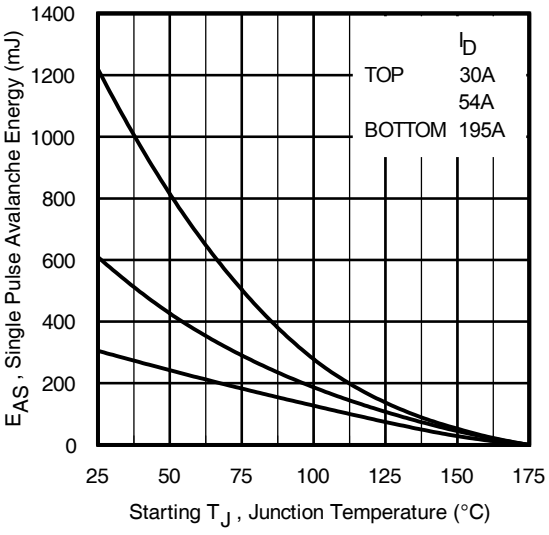



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

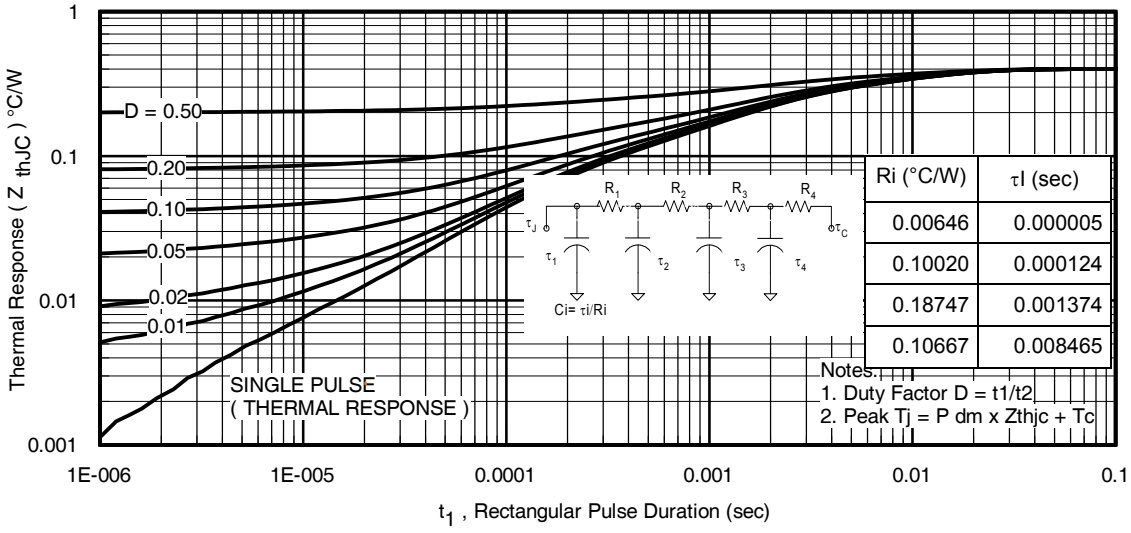



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

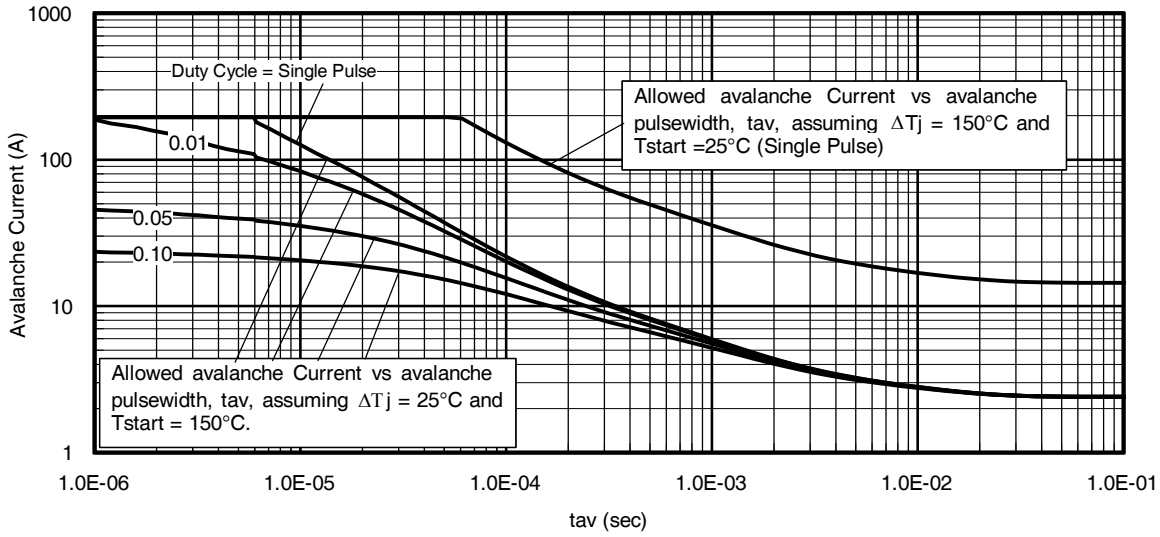



**Fig 14.** Avalanche Current vs. Pulse width

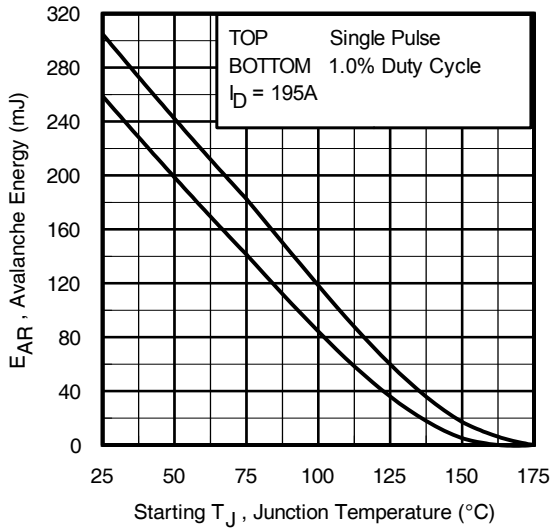



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 13, 14).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

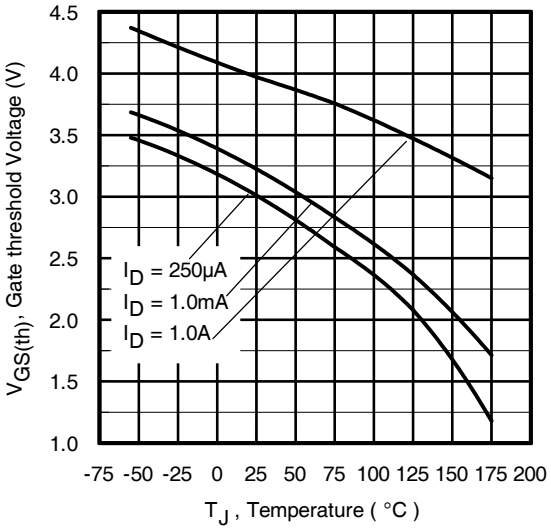



**Fig 16.** Threshold Voltage vs. Temperature

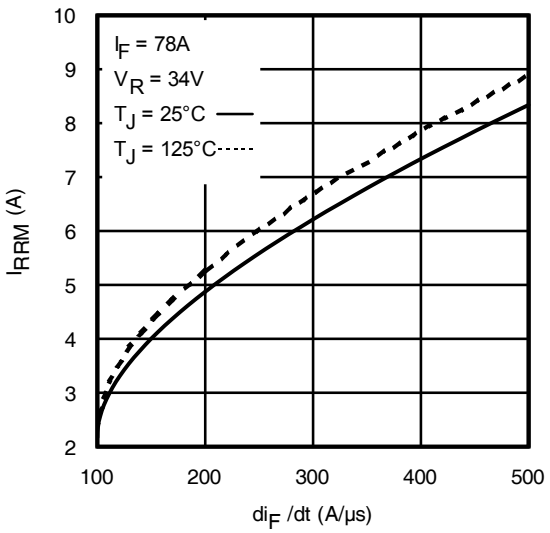



**Fig. 17** - Typical Recovery Current vs. dif/dt

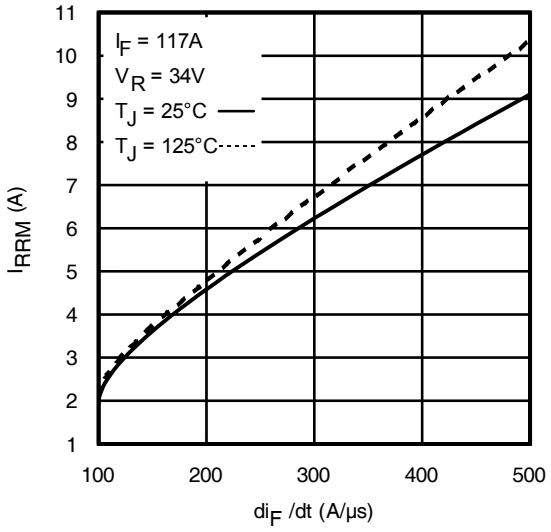



**Fig. 18** - Typical Recovery Current vs. dif/dt

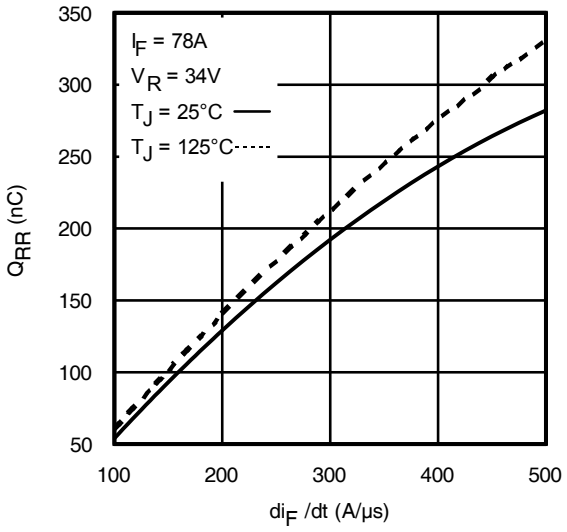



**Fig. 19** - Typical Stored Charge vs. dif/dt

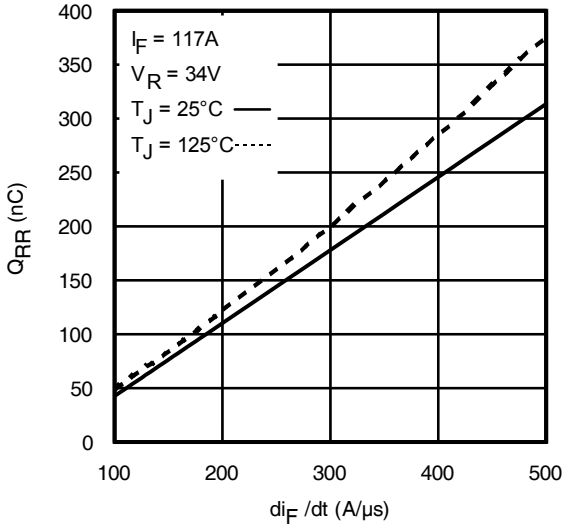



**Fig. 20** - Typical Stored Charge vs. dif/dt

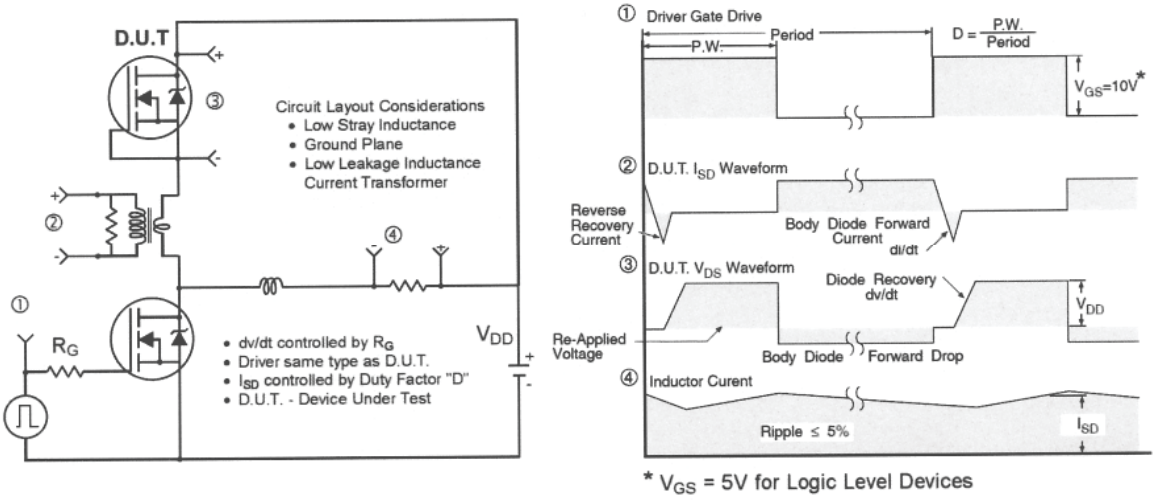



**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

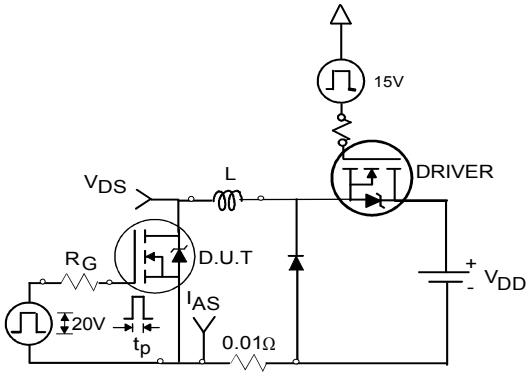



**Fig 22a.** Unclamped Inductive Test Circuit

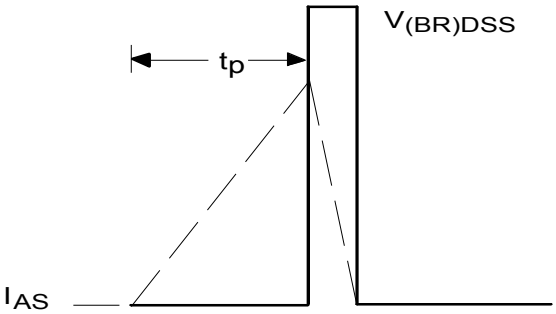



**Fig 22b.** Unclamped Inductive Waveforms

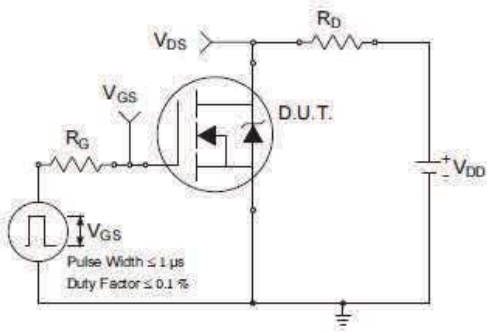



**Fig 23a.** Switching Time Test Circuit

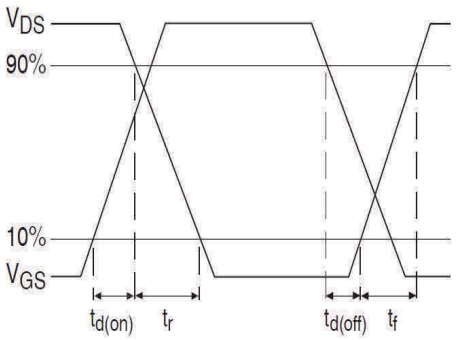



**Fig 23b.** Switching Time Waveforms

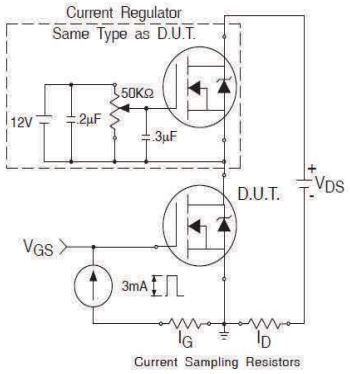



**Fig 24a.** Gate Charge Test Circuit

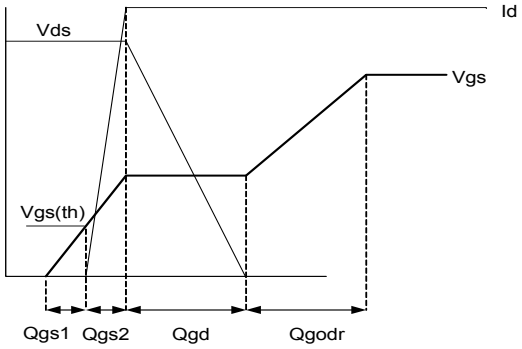
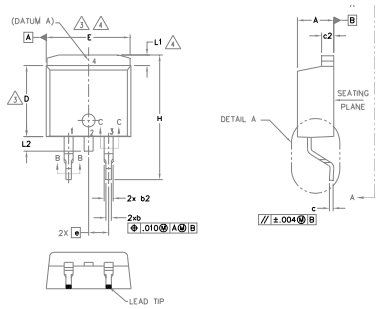


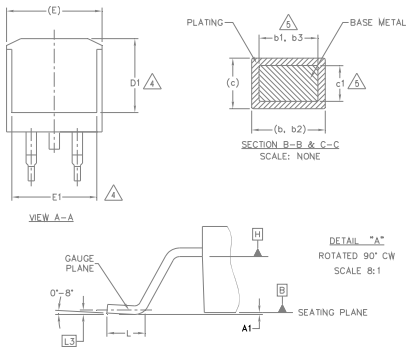

**Fig 24b.** Gate Charge Waveform

## D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.







| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 0.00 | 0.254 | .000 | .010 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | – | .270 | – | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | – | .245 | – | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | – | 1.68 | – | .066 | 4 |
| L2 | – | 1.78 | – | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | |

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

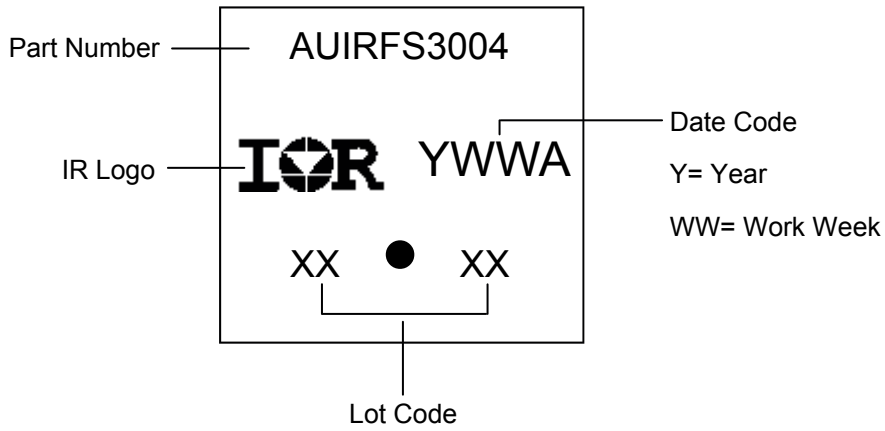
HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

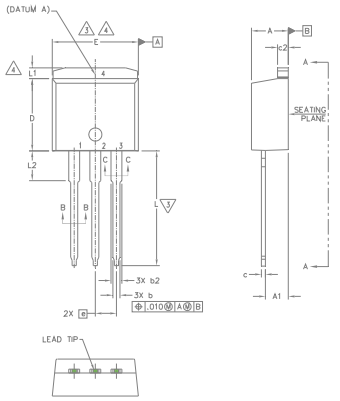
IGBTs, CoPACK

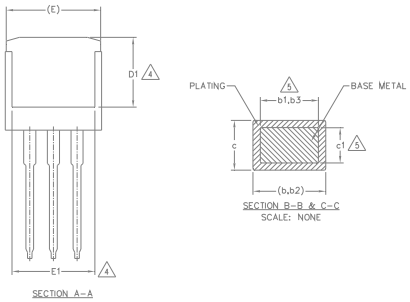
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

## D²Pak (TO-263AB) Part Marking Information



## TO-262 Package Outline (Dimensions are shown in millimeters (inches)




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

HEXFET

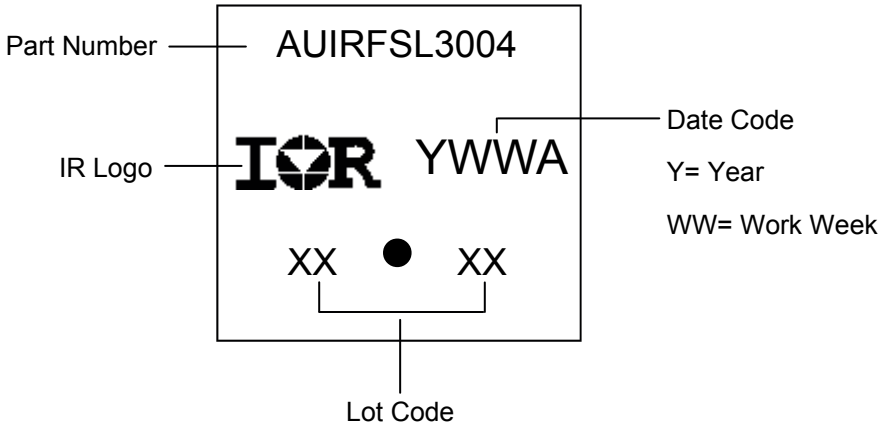
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

DIODES

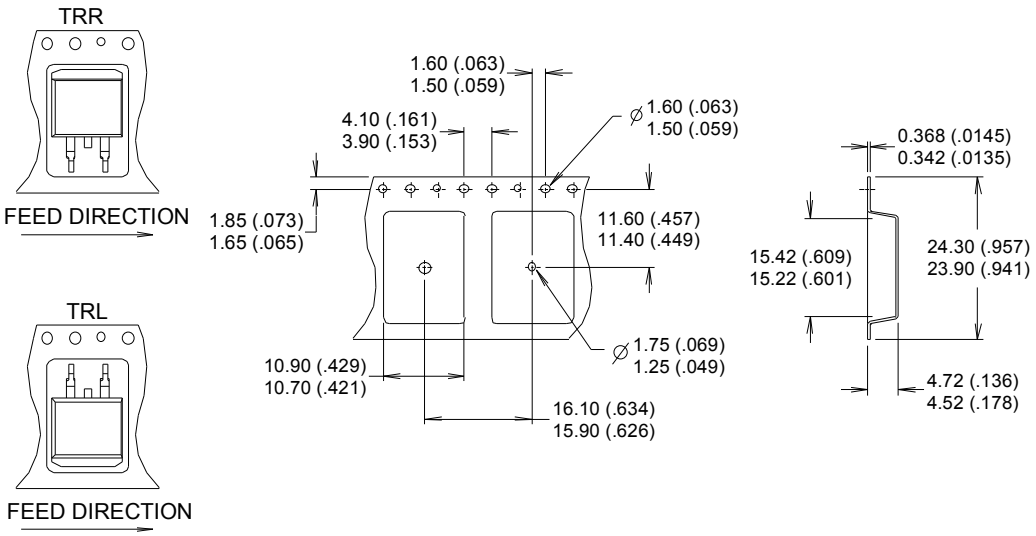
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

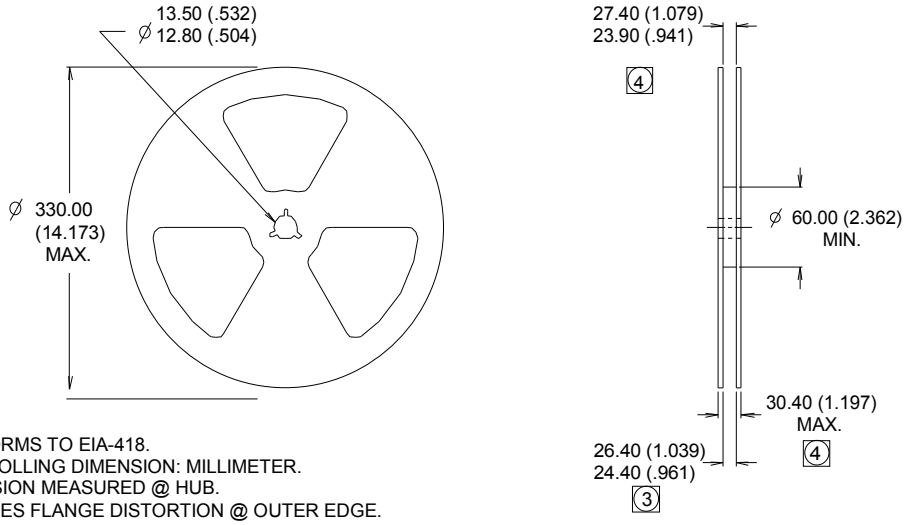
| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 3.02 | .080 | .119 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | – | .270 | – | 4 |
| E | 9.65 | 10.67 | .380 | .420 | 3,4 |
| E1 | 6.22 | – | .245 | | 4 |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.10 | .530 | .555 | |
| L1 | – | 1.65 | – | .065 | 4 |
| L2 | 3.56 | 3.71 | .140 | .146 | |

## TO-262 Part Marking Information



**D²Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))




NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Qualification Information**

| | | | |
|---|---|---|---|
| **Qualification Level** | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| **Moisture Sensitivity Level** | | $D^2$-Pak | MSL1 |
| | | TO-262 | |
| **ESD** | Machine Model | Class M4 (+/- 800V)† AEC-Q101-002 | |
| | Human Body Model | Class H3A (+/- 6000V)† AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 2000V)† AEC-Q101-005 | |
| **RoHS Compliant** | | Yes | |

† Highest passing voltage.

**Revision History**

| Date | Comments |
|---|---|
| 10/20/2015 | • Updated datasheet with corporate template<br>• Corrected ordering table on page 1. |
| 10/11/2017 | • Corrected typo error on part marking on page 8,9. |

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