TPS2398EVM/TPS2399EVM Evaluation Modules for -48-V Hot Swap Controllers

User's Guide

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Evaluation Modules for −48-V Hot Swap Controllers

Systems Power

Contents

1 Introduction

This User's Guide describes the use and features of the simple −48-V hot swap evaluation module (EVM). This EVM can be used to learn about the TPS2398 and TPS2399 hot swap controller integrated circuits (ICs) from Texas Instruments (TI). The TPS2398 and TPS2399 are negative voltage hot swap controllers intended for use in systems needing to hot swap telecom distribution-level voltages. They integrate inrush current control, peak current limiting, electronic circuit breaker, enable input, and current fault indication. The EVM is a PCB-based tool featuring either device, and can be used to evaluate device operation in simulated live insertion events.

1.1 Features

The following list highlights some of the features of the TPS2398 and TPS2399.

- Wide input supply range of −36 V to −80 V
- Transient rating to −100 V
- Programmable current limit
- Programmable current slew rate
- Enable input (EN)
- Fault timer to eliminate nuisance trips
- Open-drain power good output ($\overline{PG}$)
- 8-pin MSOP package

1.2 Description

The TPS2398 and TPS2399 simple −48-V hot swap controllers are integrated solutions optimized for use in nominal −48-V systems. They are used in conjunction with an external N-channel MOSFET and sense resistor to enable hot swap, the insertion and removal of plug-in cards or modules in powered systems. Both devices feature inrush current slew rate and peak magnitude limiting, which are easily programmed by the sense resistor value, and a single external capacitor. They facilitate implementation of platform control of the electrical connection or isolation of the protected load, and provide single-line load fault reporting. An on-chip timer, also set by a single capacitor, provides filtering against nuisance breaker trips. These features are all incorporated into a tiny 8-pin MSOP package.

The TPS2398 latches off in response to current faults. The TPS2399 periodically retries the load, to test for the continued existence of a fault.

2 The −48-V Hot Swap Controller EVM

2.1 Module Description

The −48-V hot swap EVM contains all the components needed to implement a complete telecom hot swap interface. In addition, it contains some additional components and PCB patterns to facilitate evaluation of the device.

Banana jacks are provided for connection of the user's power supply. On the switched side of the hot swap circuit, jacks are also provided for connection of the user's electronic or resistive load, if desired. The board also contains two through-hole patterns for the installation of large-value aluminum electrolytic capacitors. This capacitance is used to simulate the input bulk capacitance present at a plug-in's power inputs. The EVM is supplied from the factory with a 100-µF capacitor installed in one of the locations. The second pattern, connected in parallel with the first, can be used to increase or otherwise modify the amount of load capacitance.

From the input power jacks, power is applied to the hot swap circuit via a toggle switch connected in-line with the high-side of the power bus. Bounce of the switch contacts helps the user observe the response of the devices under power-up conditions resembling those of an actual application. An on-board slide switch is also provided to independently toggle the status of the device enable input (EN pin).

With the TPS2398 and TPS2399, both inrush slew rate limiting and a fault time-out period are externally programmable using capacitors. On the EVM, several options are provided for slew rate limiting, for quick comparison of the effect of capacitor value on this function. The capacitors can be quickly switched in and out of the circuit via the DIP switch. Fault timing programming is set up in a similar manner; some amount of capacitance is hard-wired into the circuit, with the option of switching in additional capacitance.

Test points are provided throughout the circuit for easy voltage monitoring via oscilloscope or voltmeter. The test point connections are listed in Table 4.

A pictorial of the −48−V hot swap EVM is shown in Figure 1.

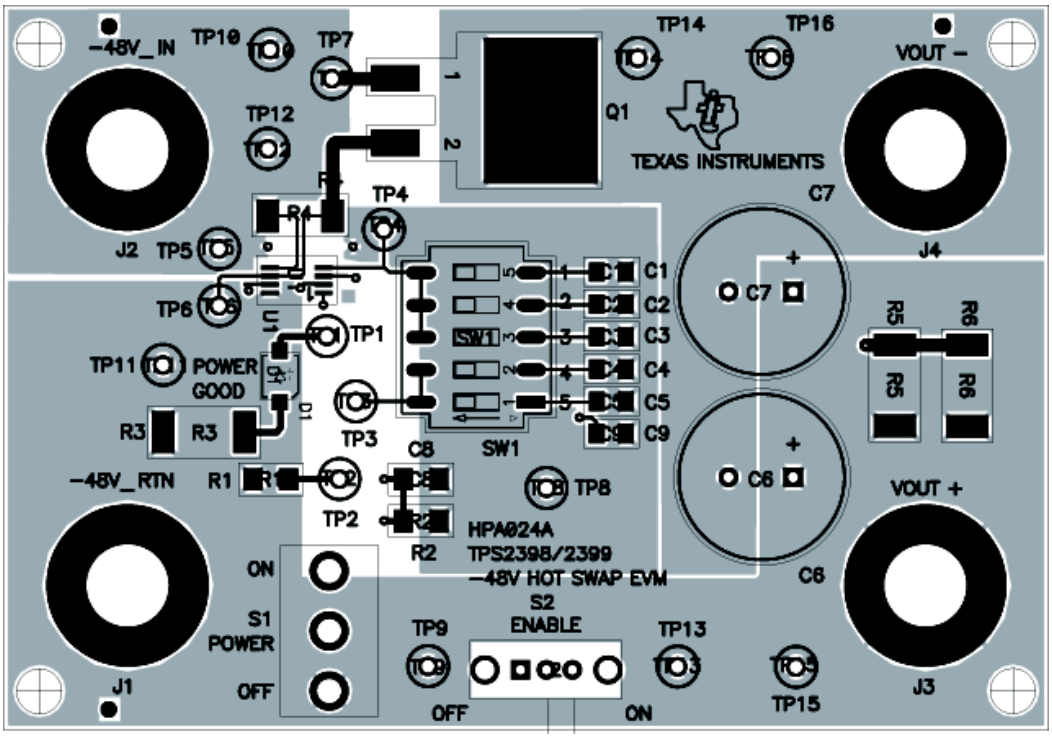

Figure 1. Evaluation Module Top Assembly

2.2 EVM Schematic Diagram and List of Materials

The EVM schematic diagram is shown in Figure 2.

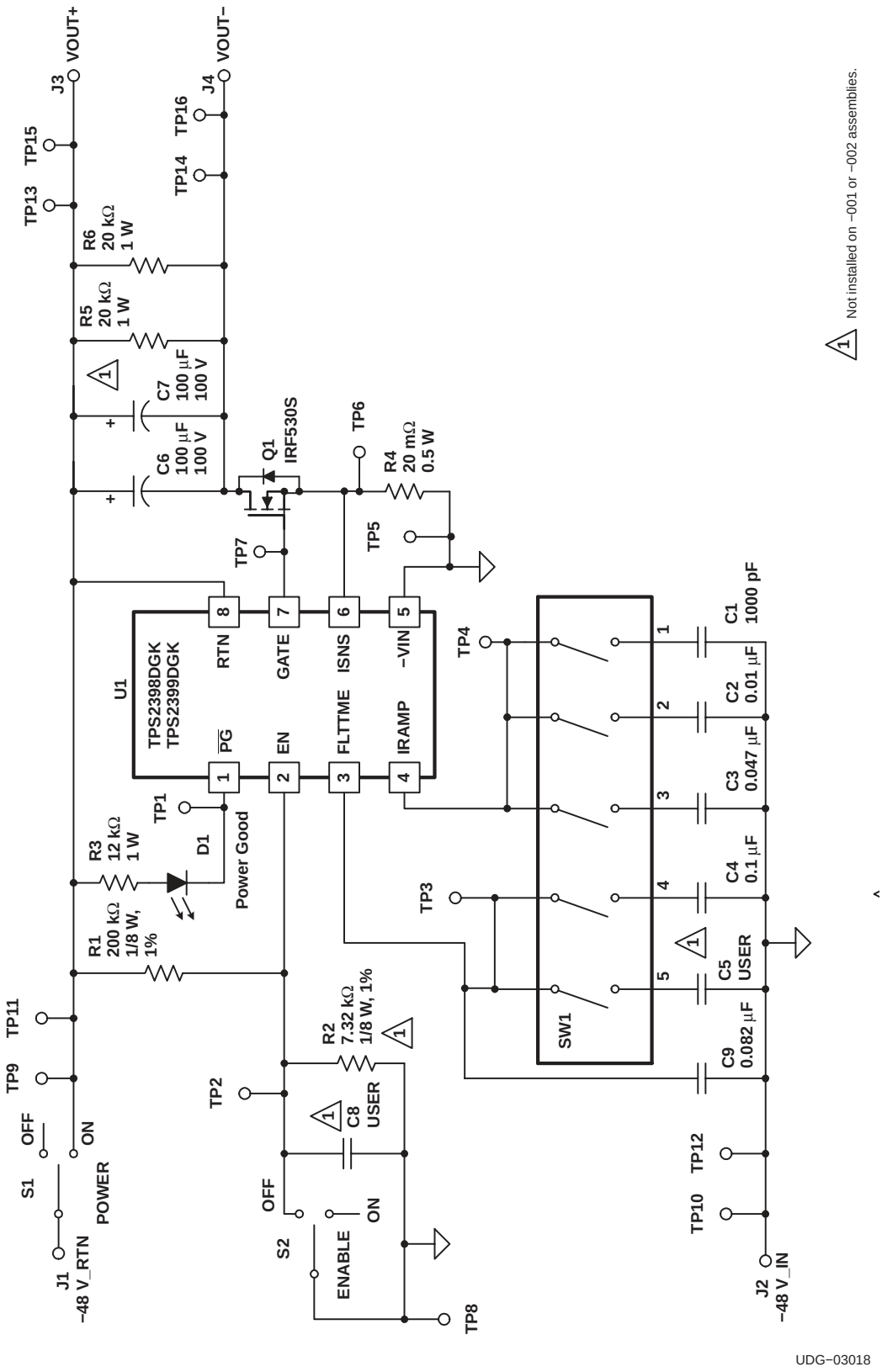

Figure 2. −48-V Hot Swap Evaluation Module Schematic

Table 1. List of Materials

REFERENCE DESIGNATOR	QUANTITY		DESCRIPTION	MANUF	PART NUMBER
	−002	−001			
U1	1	−	IC, −48-V Hot Swap Controller, w/Retry	Texas Instruments	TPS2399DGK
U1	−	1	IC, −48-V Hot Swap Controller, Latching	Texas Instruments	TPS2398DGK
TP1−TP4, TP6, TP7, TP9, TP11, TP13, TP15	10	10	Jack Test Point, red	Farnell	240−345
TP5, TP8, TP10, TP12, TP14, TP16	6	6	Jack, test point, black	Farnell	240−333
S1	1	1	Switch, toggle, SPDT, PC Mnt.	E−Switch	100SP1T1B1M2QE
S2	1	1	Switch, slide, SPDT, right angle, 200 mA	E−Switch	EG1213
SW1	1	1	Switch, dip, 5-position, SPST	CTS	219−05MS
R1	1	1	Resistor, 200 kΩ, 0.125W, 1%	Panasonic	ERJ−8ENF2003
R2	−	−	Resistor, 0.125W, 1%	Standard	Standard
R3	1	1	Resistor, 12 kΩ, 1W, 5%	Venkel	CR2512−1W123J
R4	1	1	Resistor, 0.02 Ω, 0.5W, 1%	Vishay−Dale	WSL−2010 .020<1%
R5, R6	2	2	Resistor, 20 kΩ, 1W, 5%	Venkel	CR2512−1W203J
Q1	1	1	XSTR, MOSFET, N−channel, $V_{(BR)}$ > 100V	Int'l Rectifier	IRF530S
J1, J2, J3, J4	4	4	Jack, banana, non-insulated, PC mount	Pomona	3267
D1	1	1	Diode, LED, green	Panasonic	LN1361C
C1	1	1	Capacitor, ceramic, 1000 pF, 25 V, 10%, X7R	Vitramon	VJ0805Y102KXXA
C2	1	1	Capacitor, ceramic, 0.01 µF, 16 V, 10%, X7R	Vitramon	VJ0805Y103KXJA
C3	1	1	Capacitor, ceramic, 0.047 µF, 16 V, 10%, X7R	Vitramon	VJ0805Y473KXJA
C4	1	1	Capacitor, ceramic, 0.1 µF, 16 V, 10%, X7R	Vitramon	VJ0805Y104KXJA
C5	−	−	Capacitor, ceramic, 0805	Standard	Standard
C6	1	1	Capacitor, aluminum. electrolytic, 100 µF, 100 V, 20%	Vishay	EKA00DE310L00
C7	−	−	Capacitor, aluminum. electrolytic, 100 µF, 100 V, 20%	Vishay	EKA00DE310L00
C8	−	−	Capacitor, ceramic, 1206	Standard	Standard
C9	1	1	Capacitor, ceramic, 0.082 µF, 16 V, 10%, X7R	Vitramon	VJ0805Y823KXJA
N/A	4	4	Spacer, nylon, hex, #6−32, 0.625"	Eagle	14HTSP020
N/A	4	4	Screw, nylon, round head, #6−32, 0.25"	Eagle	010632R025
N/A	1	1	PCB, FR−4, 2−layer, SMOBC, 3.225" x 2.237", 0.062" thk.	Texas Instruments	HPA024

2.3 −48-V Hot Swap EVM Operating Specifications

The −48−V hot swap EVM is intended to allow some degree of user reconfiguration. This allows designers to set up the circuit to better represent the characteristics of their target application. Potential modifications include changing the current limit threshold, the inrush limiting, the fault timing, and load characteristics. However, under no circumstances should the EVM kit be operated beyond the absolute maximum conditions specified in Table 2.

Table 2. Absolute Maximum Ratings (1)(2)

PARAMETER	MIN	MAX	UNITS
Input voltage range, J1	−0.3	100	V
Load current, J3		−2.25	A
Load return current, J4		2.25	
Ambient operating temperature range	−40	85	°C

(1) All voltages are with respect to the PCB −48-V_IN node at J2.

(2) Currents are positive into and negative out of the specified terminal.

As supplied from the factory, the −48-V hot swap EVM is configured for operation under the following target conditions, shown in Table 3.

Table 3. Recommended Operating Conditions (1)(2)

PARAMETER	MIN	TYP	MAX	UNITS
Input supply voltage, J1	36	48	80	V
Nominal load current, J3		−1		A
Nominal load return current, J4		1		
Operating temperature range	−40		85	°C

(1) All voltages are with respect to the PCB −48-V_IN node at J2.

(2) Currents are positive into and negative out of the specified terminal.

3 Getting Started

3.1 Equipment Requirements

The following test equipment is required to use the −48-V hot swap EVM (TPS2398EVM or TPS2399EVM).

- Power supply, 80 Vdc at 3-A minimum
- Oscilloscope
- Digital voltmeter (DVM)

The individual DIP switches of SW1 are labeled numerically on the PCB silkscreen. Throughout this document, references to the DIP switches (e.g., SW1−1) apply to these screened labels, not to any marking on the switch. However, to determine the ON and OFF positions of the switches, use the labeling on the switch body itself.

3.2 Verifying the EVM Operation

The following procedure steps may be used to verify functional operation of the EVM after receipt.

3.2.1 Equipment Setup

1. On the EVM board, place the POWER switch in the OFF position, and verify that the ENABLE switch is in the OFF position.
2. Set the DIP switches 1 through 4 of switch SW1 to the ON position.
3. Turn on the power supply and adjust the output for about 48 V. Verify the supply current limit is set to allow at least 3 A. Turn off the power supply.
4. Connect the EVM and test equipment as shown in Figure 3.
5. On the oscilloscope, set the channel amplifiers to the following scales:
   - CH1: 20 V/div
   - CH2: 2 V/div
   - CH3: 5 V/div
   - CH4: 20 V/div

   For easier correlation to the information in this document, the scope trace baselines can be positioned as shown in Figure 4.
6. Set the scope to trigger on the rising edge of Channel 1, at approximately a 10-V level. Set the scope timebase to 10 ms, and the trigger mode to NORMAL.

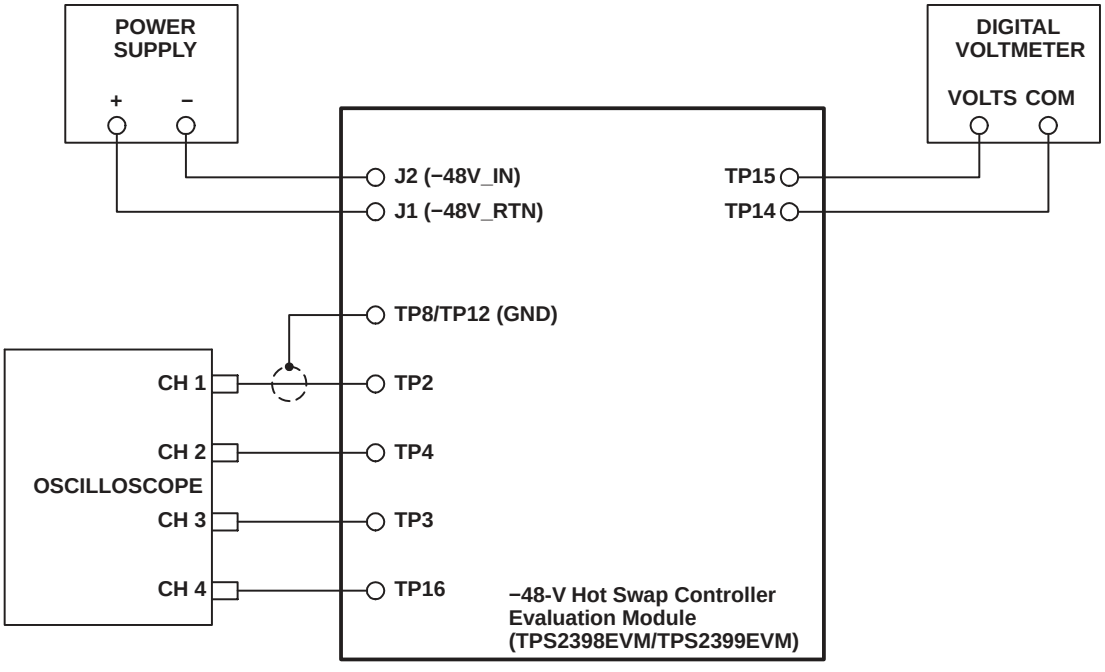

Figure 3. Evaluation Module Setup

3.2.2 Functional Test

1. Turn on the power supply. On the EVM, place the POWER switch in the ON position. Verify the power good LED (D1) is OFF. Verify the DVM reading is 0 ±100 mV.

2. Place the ENABLE switch in the ON position. Verify the green power good LED turns on, and the DVM now displays approximately the input supply voltage level. The scope should have acquired a sweep similar to that shown in Figure 4.

   The brief fault timing ramp which is shown in Figure 4 FLTTIME trace may or may not be present, depending on the actual values of the timing parameters for the particular board being used. If the load voltage ramps to full input potential during the initial reduced rate ramp period, then fault timing does not initiate.

3. Place either the POWER or ENABLE switch (or both) in the OFF position to remove power from the VOUT terminals.

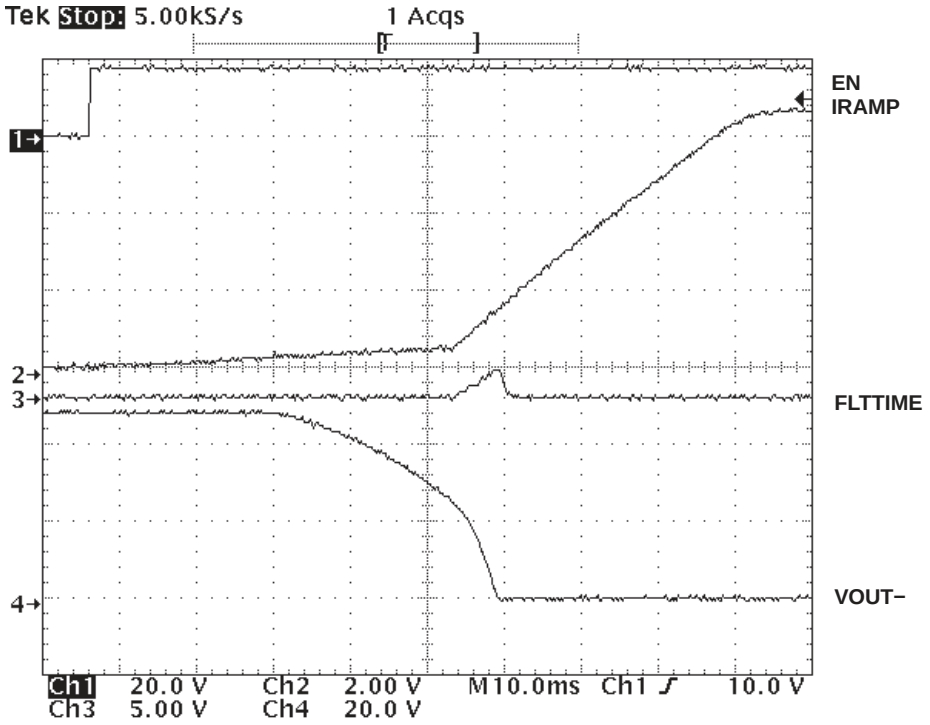

Figure 4. Load Ramp-Up Waveforms

4 Using the Evaluation Module to Evaluate the TPS2398/99

Procedures similar to the steps of Section 3.2.2 for functional test of the EVM can also be used to continue evaluation of the TPS2398 and TPS2399 hot swap controllers. Additional details about the EVM features are provided in this section.

The ENABLE switch can be used to enable and disable power to the load (i.e., the VOUT+ and VOUT− terminals), when the POWER switch is in the ON position.

Also, with the ENABLE switch in the ON position, the POWER switch can be toggled ON and OFF to simulate hot swap events with the device set up to automatically power up the load.

4.1 Test Points

The −48-V hot swap EVM contains the test points listed in Table 4, for waveform and voltage monitoring.

Table 4. Test Points

TEST POINT	SIGNAL NAME	DESCRIPTION
TP1	$\overline{PG}$	Open-drain, active-low indication of a load power good condition. On the EVM, this signal drives the green LED.
TP2	EN	Device enable input to turn on/off power to the load.
TP3	FLTTIME	Fault timing waveform of the TPS2398/99.
TP4	IRAMP	Current ramp control output waveform.
TP5	−VIN	Negative supply input and reference pin for the TPS2398/99. On the EVM, this is connected to −48V_IN.
TP6	ISENS	Current sense input of the controller.
TP7	GATE	Gate drive for external FET Q1.
TP8	−VIN	Secondary test point on device reference node.
TP9	−48V_RTN	The high side of input power to the EVM. When used in conjunction with a lab supply, this connects to the (+) jack. (Test points are on plug-in side of the POWER switch.)
TP11		
TP10	−48V_IN	The low side of input power to the EVM. When used in conjunction with a lab supply, this connects to the (−) jack.
TP12		
TP13	VOUT+	High side of switched (load) output power.
TP15		
TP14	VOUT−	Low side of switched (load) output power.
TP16		

4.2 Load Capacitors

Capacitor patterns C6 and C7 are available on the EVM for installation of components to represent the module input bulk capacitance; i.e., the load capacitance seen by the hot swap interface circuit. As supplied from the factory, the EVM contains a 100-µF aluminum electrolytic installed at C6. Further customization to approximate the user's application can be done using either C6 or C7. When installing capacitors in these mounting locations, care should be taken to observe the polarity marking on the PCB silkscreen, and to use appropriately rated capacitors for voltage withstanding. Generally, telecom applications should use 100-V minimum rated capacitors.

Banana jacks J3 and J4 are also connected across the output terminals, in parallel with C6 and C7. These jacks can be used to connect additional loads to the EVM board.

4.3 Changing the Current Limit Threshold

During power-up of a plug-in card, the TPS2398 and TPS2399 limit the peak inrush current drawn by the discharged bulk capacitance. The LCA senses load current as the drop across an external sense resistor. Current is regulated by slewing the gate of the pass FET to maintain the voltage drop at an internally set level, nominally 40 mV. Therefore, the peak current level can be established by selecting the appropriate sense resistor value. On the −48-V hot swap EVM, this resistor is R4. The default value of R4 is 20 mΩ. To modify the current limit threshold, a new sense resistor value can be determined from Equation 1.

$$R4 \leq \frac{V_{MAX}}{I_{MAX}} \quad (1)$$

where

- V_{MAX} is the sense voltage limit
- I_{MAX} is the desired current limit threshold

Using the device minimum value of 33 mV for V_{MAX} along with the required minimum load current ensures that minimum amount of current can always be supplied to the load. For example, a particular line card is expected to draw a maximum of 1.2 A, when the power bus is at its operating minimum level of −36 V, once the card is powered up and operating normally. For this load characteristic, a sense resistor value less than 33 mV/1.2 A, or 27 mΩ, is selected. A 25-mΩ resistor is the closest approximate standard value that is readily available. A smaller-value resistor is also acceptable, but carries a corresponding increase in the maximum current limit.

4.4 Changing the Inrush Slew Rate

The TPS2398 and TPS2399 also feature slew rate limiting as current is ramped to charge the load capacitance. The slew rate is easily programmed, once the sense resistor is determined, with a small-value capacitor connected between the IRAMP and −VIN pins. The EVM comes equipped with three preset capacitor values, selectable either individually or in combination by closing the appropriate DIP switches of SW1. The default values of the capacitors, and the corresponding nominal slew rates, are given in Table 5.

Table 5. Default Slew Rates

SW1 DIP	REFERENCE DESIGNATOR	INSTALLED VALUE	SLEW RATE (A/s)
1	C1	1000 pF	5000
2	C2	0.01 μF	500
3	C3	0.047 μF	106

The EVM can be used to illustrate the relationship between current limit, inrush slew rate, load values, and the circuit's fault timing requirements. With only DIP switch SW1−1 closed, the fastest of the preset slew rates is selected, and only the hard-wired timing capacitor C9 is connected to the TPS2398 or TPS2399 controller. However, this is sufficient to allow the bulk capacitor C6 to fully charge, from 0 volts, across the full range of input supply voltages, down to −80 V. This can be observed by connecting input power as shown in Figure 3, displaying the VOUT− node on an oscilloscope, and enabling the device.

To observe the controller response to a load that does not charge up as expected (a shorted or otherwise excessive load), set switches SW1−1, SW1−2, and SW1−3 to the ON position. This greatly reduces the inrush (load charging) current slew rate at turn-on, with a corresponding increase in the amount of time needed to successfully charge the intended load. Increase the supply level to between approximately 60 V and 80 V, and again enable the device. In this case, the voltage ramp time is excessively long relative to the programmed fault timer; the controller times out and turns off the load(1). Again, this can be viewed on an oscilloscope and also in the failure of the green powergood LED to illuminate. When evaluating the TPS2399, the LED may ultimately illuminate, indicating capacitor charging is eventually completed on a successive retry.) If this combination represented the parameters of the target plug-in module, then the timing capacitance of C9 and C4 (SW1−4 closed) would be more appropriate. The intended load, in this case, the 100-µF capacitor, can again be charged up over the input voltage range.

The inrush slew rate can be changed, to better match the application requirement, by replacing any capacitor C1, C2 or C3. The PCB patterns are sized for 0805 ceramic chip capacitors. Use equation 2 to calculate the new ramp capacitor, C_{RAMP}, value in microfarads.

$$C_{RAMP} = \frac{11}{100 \times R4 \times \left(\frac{di}{dt}\right)_{MAX}} \quad (2)$$

where

- R4 is the selected sense resistor value, in ohms
- $(di/dt)_{MAX}$ is the desired maximum slew rate, in amperes/second.

4.5 Fault Timing with the TPS2398/TPS2399

Whenever the hot swap controller is limiting current to the load, an on-chip timer is monitoring this operation against an established time limit. The timeout period is generated by the constant-current charging of a capacitor at the FLTTIME pin. If current regulation ceases prior to expiration of the timer, the capacitor is discharged, and normal steady-state operation of the load either starts or resumes. However, if the timer expires, then the pass FET is turned off, disabling power to the load, and the $\overline{PG}$ output assertion is either inhibited or cleared.

On the −48-V hot swap EVM, several capacitor patterns are provided for increasing or otherwise modifying the timeout period. Capacitor C9 is hard-wired to the device FLTTIME pin, and provides a minimum fault timer for the default load. C4 and C5 can be switched into the circuit via DIP switches SW1−4 and SW1−5, respectively. The EVM ships from the factory with a 0.1-µF capacitor installed at C4; C5 is not populated for easier subsequent user modification as required.

(1) Due to tolerances of various EVM parameters, some units may not fault out under these conditions. Generally, this is due to the fact that the amount of voltage ramping during the reduced-rate turn-on period will vary from device to device. Some units may be able to charge the load almost completely during this period, when fault timing is inhibited. A more severe load fault is needed to view the fault response. Additional capacitance, or even a resistor, can be connected across the VOUT terminals, J3(+) and J4(−) or at C7. If the user is confident the module is operating correctly, the load can also be shorted out to do this demonstration.

If the target application requires fault timing other than that provided by the default EVM setup, a new value of timing capacitor can be calculated from equation (3). When selecting from the readily available capacitor values for the result of equation (3), default to a slightly larger, rather than smaller, capacitor.

$$C_{FLT} = \frac{\left(55 \times t_{FLT}\right)}{3.75} \quad (3)$$

where

- C_{FLT} is the calculated value in microfarads,
- t_{FLT} is the desired timeout period in seconds

4.6 Using the EN Pin to Adjust Undervoltage Lockout (UVLO)

The TPS2398 and TPS2399 devices have an internal UVLO circuit, which keeps the load disabled when the input supply voltage is low. The internal threshold is set to a nominal 30 V, at the RTN input with respect to −VIN, with a maximum specification value of 36 V. This setting is targeted at general telecom applications. However, it is possible to raise the minimum start-up threshold, and potentially tighten the tolerance window of the UVLO function, by using the enable input comparator.

Where the desired UVLO voltage is greater (more negative) than the internal threshold, a resistor divider on the input supply can be used to enable the load at this minimum voltage level. The divided down input voltage then drives the EN pin. Resistor patterns R1 and R2 are provided on the EVM to implement this function. The nominal enable comparator threshold is 1.4 V. Assuming the default R1 value of 200 kΩ is used, the value of R2 is determined from Equation 4.

$$R2 = \frac{1.4\ V}{\left(V_{UV} - 1.4V\right)} \times 200\ k\Omega \quad (4)$$

where V_{UV} is the desired UVLO threshold.

For example, to adjust the nominal UVLO to 40 V, the value of R2 required is 7.25 kΩ, per equation (4). Using the standard value of 7.32 kΩ, the expected threshold is 39.65 V.

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