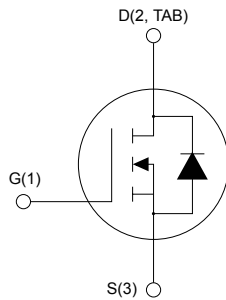
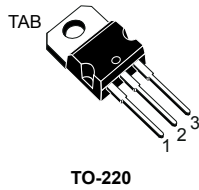



Automotive N-channel 100 V, 3.6 mΩ typ., 110 A, STripFET F7 Power MOSFET in a TO-220 package



AM01475v1_noZen

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STP150N10F7AG	100 V	4.2 mΩ	110 A

- Designed for automotive application 
- Standard level V_{GS(TH)}
- 175°C junction temperature
- 100% avalanche rated

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STP150N10F7AG](#)

Product summary

Order code	STP150N10F7AG
Marking	150N10F7AG
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	110	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$		
$I_{DM}^{(2)}$	Drain current (pulsed)	440	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
I_{AV}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	30	A
E_{AS}	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 25\text{ V}$)	650	mJ
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Current limited by package.
2. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.6	$^\circ\text{C/W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	62.5	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = max ratings			1	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5	3.5	4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 55 A		3.6	4.2	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V		9000		pF
C _{oss}	Output capacitance		-	2000	-	pF
C _{rss}	Reverse transfer capacitance			80		pF
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 110 A, V _{GS} = 10 V (see Figure 13. Test circuit for gate charge behavior)	-	127	-	nC
Q _{gs}	Gate-source charge		-	56	-	nC
Q _{gd}	Gate-drain charge		-	32	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 55 A, R _G = 4.7 mΩ, V _{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 16. Unclamped inductive waveform)	-	37	-	ns
t _r	Rise time		-	54	-	ns
t _{d(off)}	Turn-off delay time		-	68	-	ns
t _f	Fall time		-	33	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 110\text{ A}$, $V_{GS} = 0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 110\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$, $T_j = 25^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	60	-	ns
Q_{rr}	Reverse recovery charge		-	83	-	nC
I_{RRM}	Reverse recovery current		-	2.75	-	A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

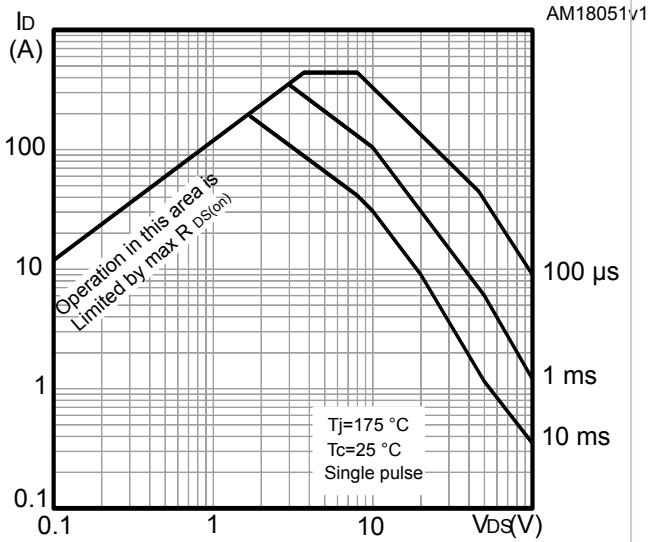


Figure 2. Thermal impedance

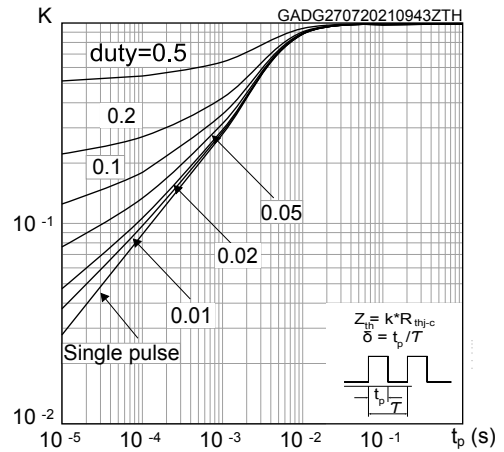


Figure 3. Typical output characteristics

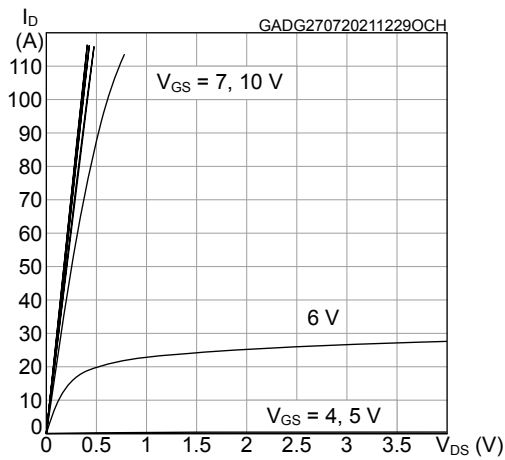


Figure 4. Typical transfer characteristics

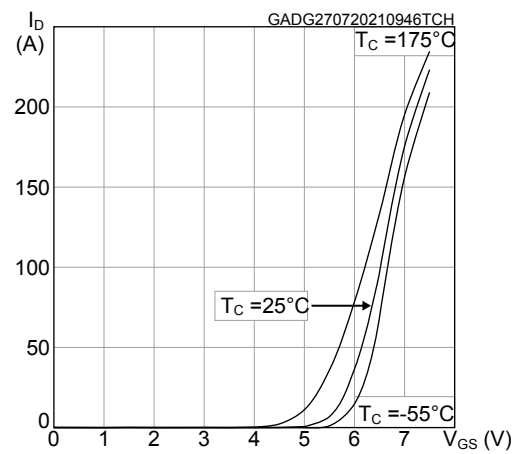


Figure 5. Typical gate charge characteristics

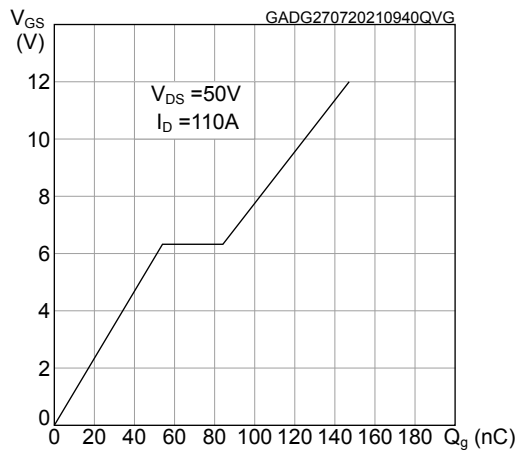


Figure 6. Typical drain-source on-resistance

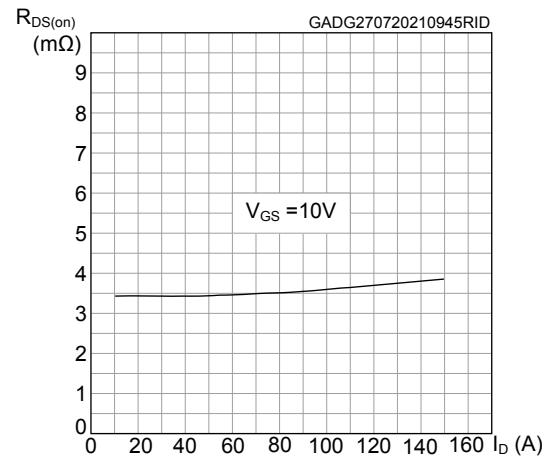


Figure 7. Typical capacitance characteristics

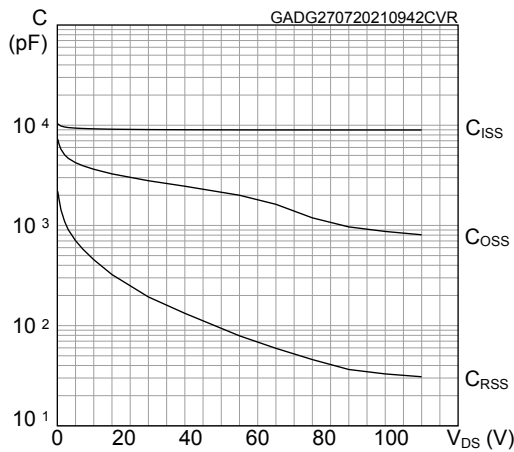


Figure 8. Normalized gate threshold voltage vs temperature

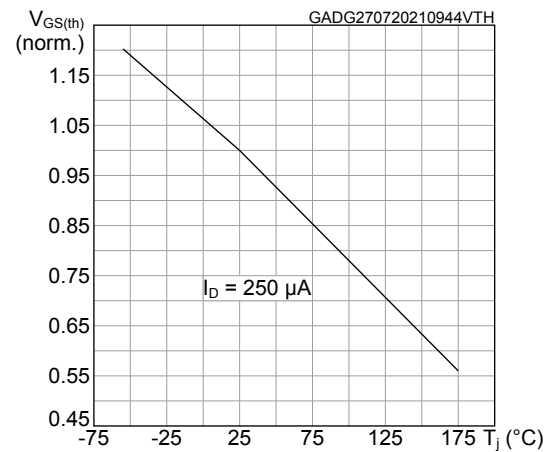


Figure 9. Normalized on-resistance vs temperature

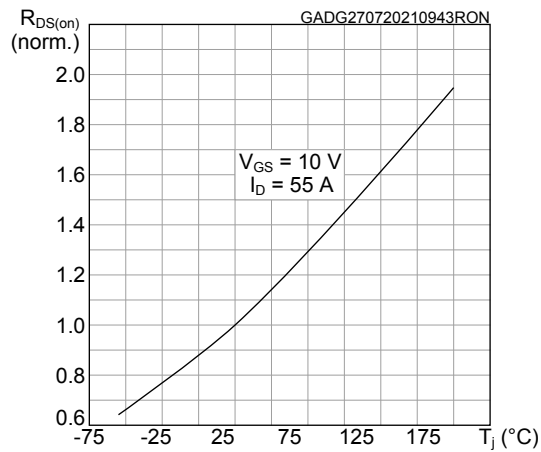


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

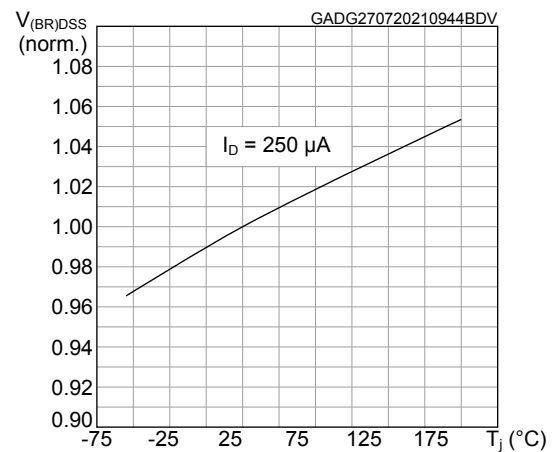
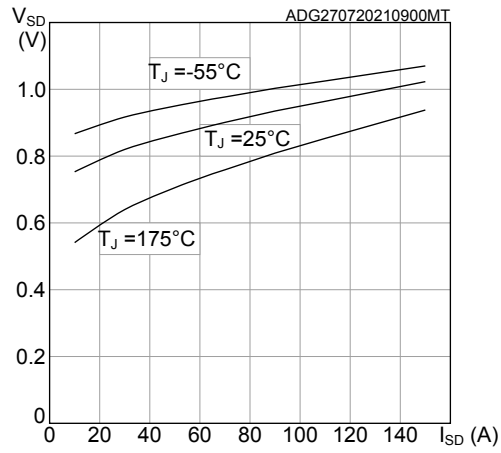
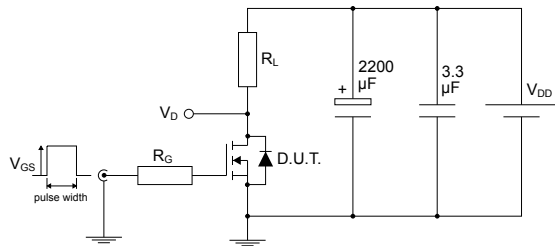


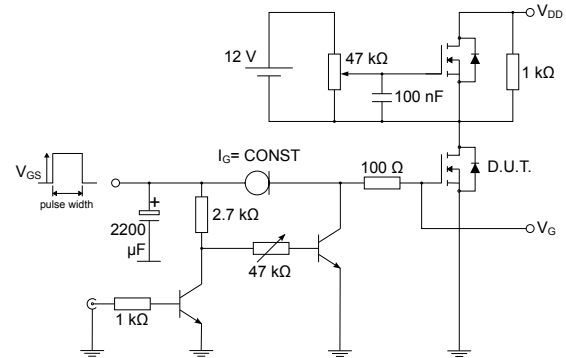
Figure 11. Source-drain diode forward characteristics



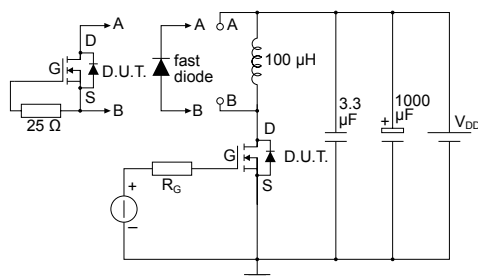
3 Test circuits

Figure 12. Test circuit for resistive load switching times


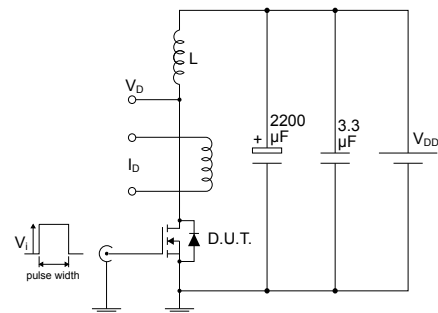
AM01468v1

Figure 13. Test circuit for gate charge behavior


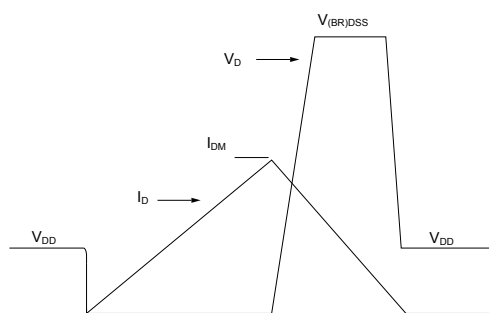
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


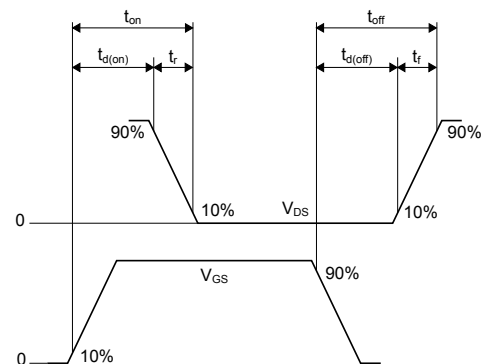
AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


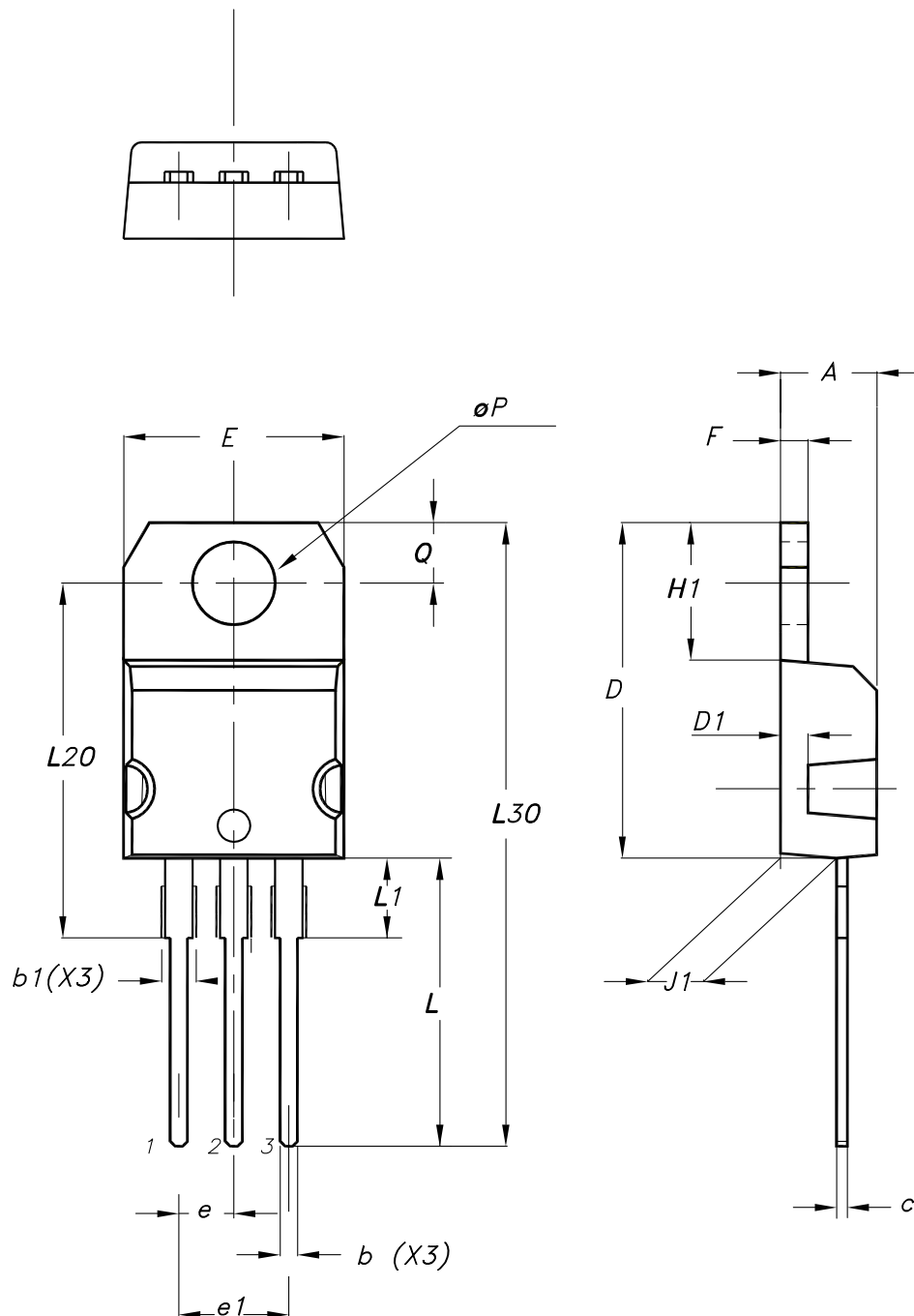
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 18. TO-220 type A package outline



0015988_typeA_Rev_23

Table 7. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 8. Document revision history

Date	Version	Changes
27-Jul-2021	1	First release
16-Mar-2023	2	Updated title in cover page

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	TO-220 type A package information	9
	Revision history	11

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved