SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
# OCTAL BUFFERS WITH 3-STATE OUTPUTS

- Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98

- P-N-P Inputs Reduce Bus Loading

- 3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively

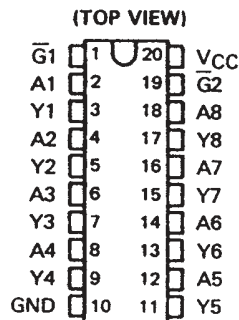| DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

description

These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any $\overline{G}$ places the affected outputs at high impedance.
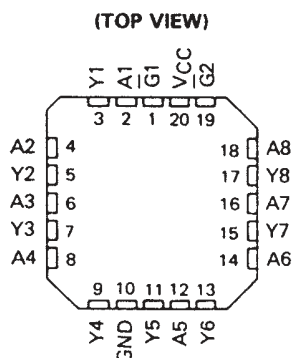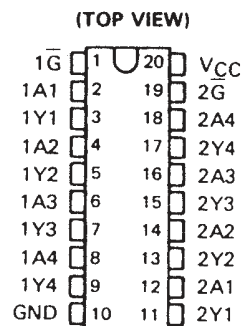
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS
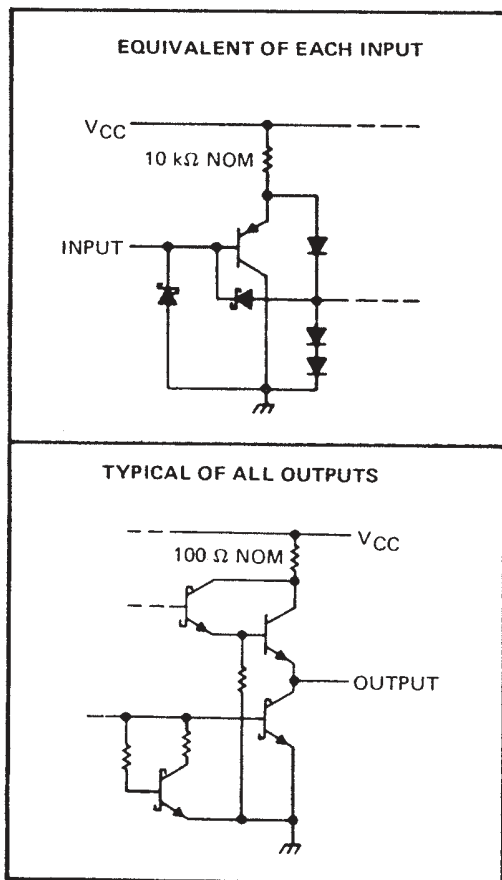
SN54LS465 AND SN54LS466 . . . J PACKAGE
SN74LS465 AND SN74LS466 . . . DW OR N PACKAGE
(TOP VIEW)

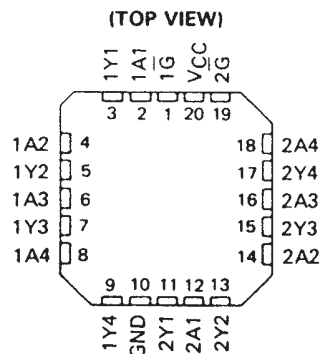|	
$\overline{G}$1 [1	20] V_{CC}
A1 [2	19] $\overline{G}$2
Y1 [3	18] A8
A2 [4	17] Y8
Y2 [5	16] A7
A3 [6	15] Y7
Y3 [7	14] A6
A4 [8	13] Y6
Y4 [9	12] A5
GND [10	11] Y5

SN54LS465 AND SN54LS466 . . . FK PACKAGE
(TOP VIEW)

SN54LS467 AND SN54LS468 . . . J PACKAGE
SN74LS467 AND SN74LS468 . . . DW OR N PACKAGE
(TOP VIEW)

1$\overline{G}$ [1	20] V_{CC}
1A1 [2	19] 2$\overline{G}$
1Y1 [3	18] 2A4
1A2 [4	17] 2Y4
1Y2 [5	16] 2A3
1A3 [6	15] 2Y3
1Y3 [7	14] 2A2
1A4 [8	13] 2Y2
1Y4 [9	12] 2A1
GND [10	11] 2Y1

SN54LS467 AND SN54LS468 . . . FK PACKAGE
(TOP VIEW)

Copyright © 1988, Texas Instruments Incorporated

TEXAS INSTRUMENTS

1

SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS

logic diagrams (positive logic)
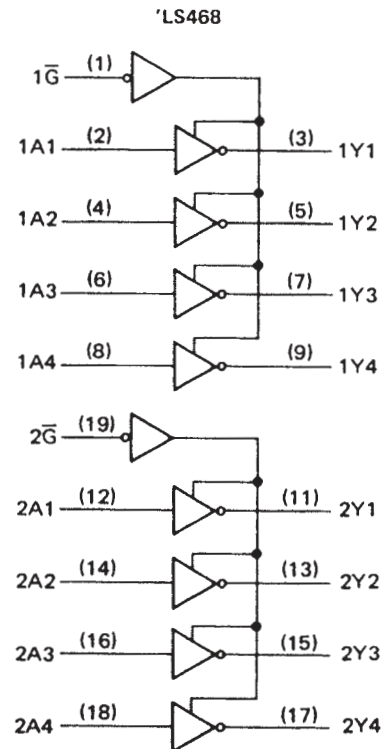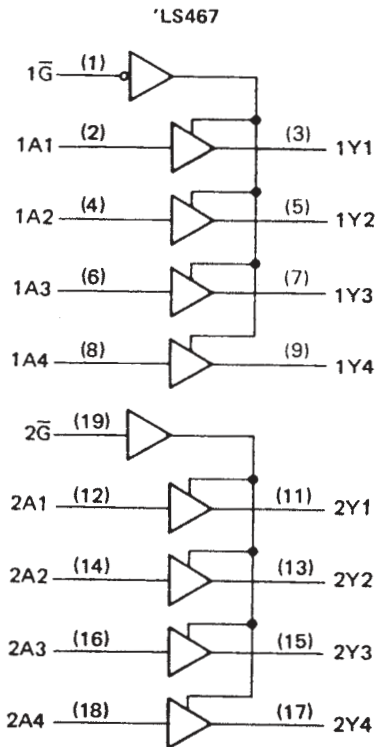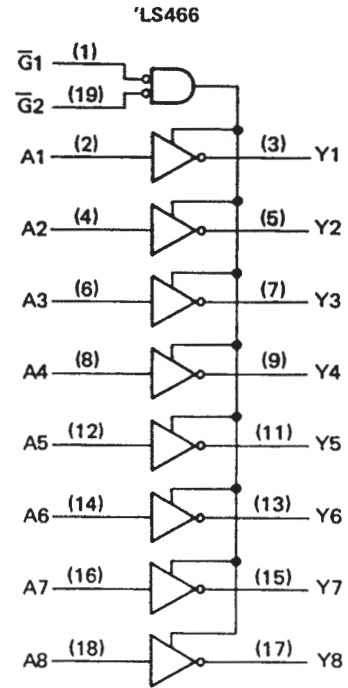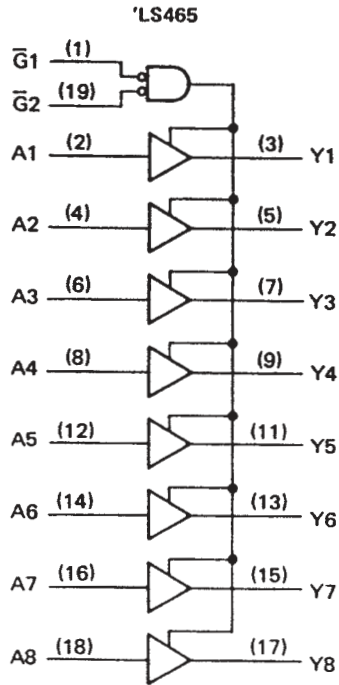
Pin numbers shown are for DW, J, and N packages.

logic symbols†

'LS465

'LS466

'LS467

'LS468
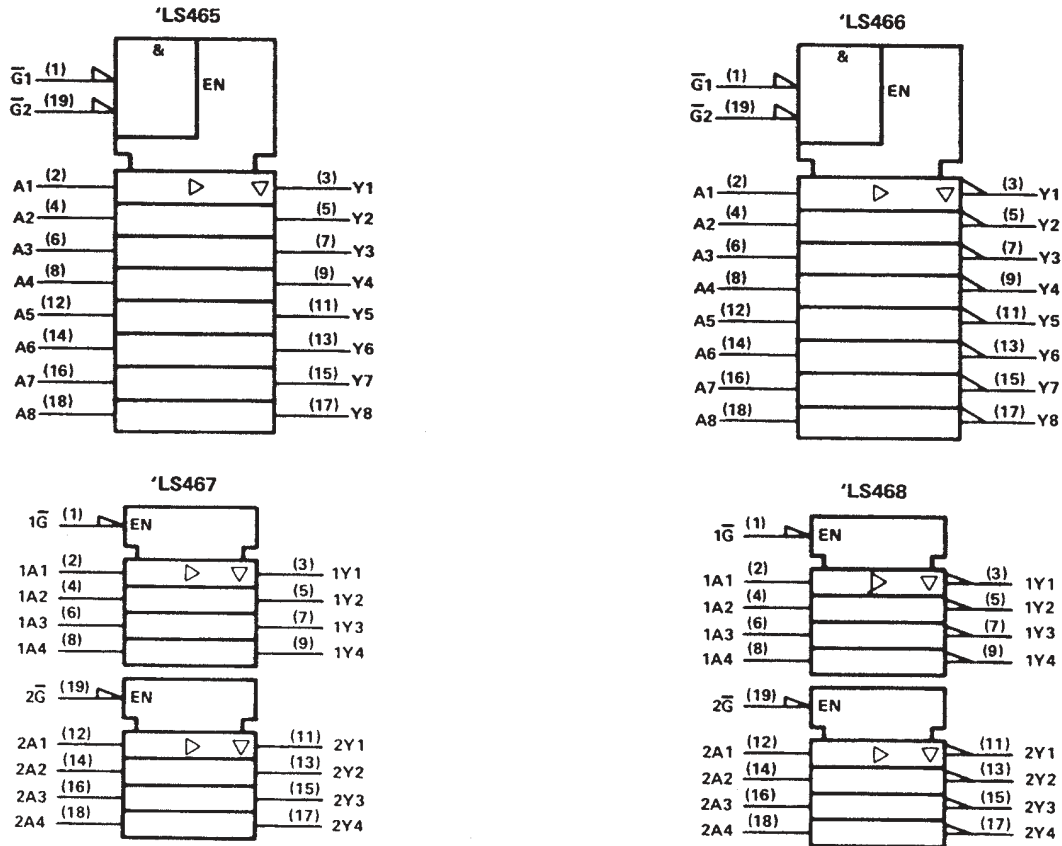
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS465 thru SN54LS468	−55°C to 125°C
SN74LS465 thru SN74LS468	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	3.3					V
			I_{OH} = −2.6 mA				2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
I_{CC}	Supply current	'LS465, 'LS467 — Outputs low	V_{CC} = MAX		19	32		19	32	mA
		'LS465, 'LS467 — Outputs high			13	22		13	22	
		'LS465, 'LS467 — Output Hi-Z			22	37		22	37	
		'LS466, 'LS468 — Outputs low			14	23		14	23	
		'LS466, 'LS468 — Outputs high			6	10		6	10	
		'LS466, 'LS468 — Outputs Hi-Z			17	28		17	28	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467 MIN	'LS465, 'LS467 TYP	'LS465, 'LS467 MAX	'LS466, 'LS468 MIN	'LS466, 'LS468 TYP	'LS466, 'LS468 MAX	UNIT
t_{PLH}	Ai	Yi	R_L = 667 Ω, C_L = 45 pF		9	15		7	12	ns
t_{PHL}	Ai	Yi			12	18		9	15	ns
t_{PZH}	$\overline{G}$ ↓	Y			25	40		25	40	ns
t_{PZL}	$\overline{G}$ ↓	Y			29	45		29	45	ns
t_{PHZ}	$\overline{G}$ ↑	Y	R_L = 667 Ω, C_L = 5 pF		25	40		25	40	ns
t_{PLZ}	$\overline{G}$ ↑	Y			30	45		30	45	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS466DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74LS466DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74LS466N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14) D
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
           B.   This drawing is subject to change without notice.
          C.   Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
          D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
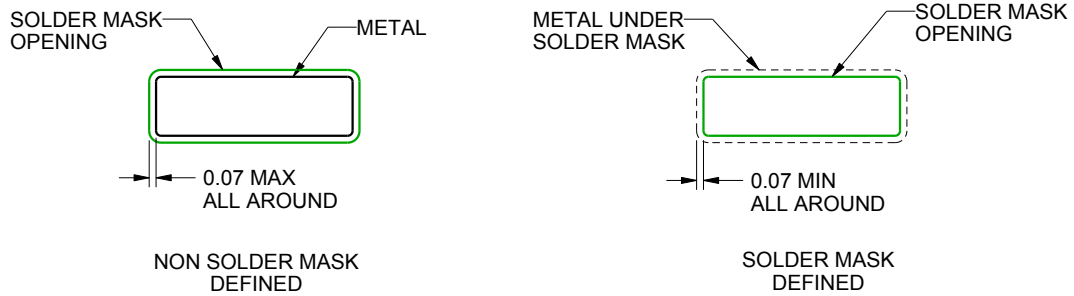5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

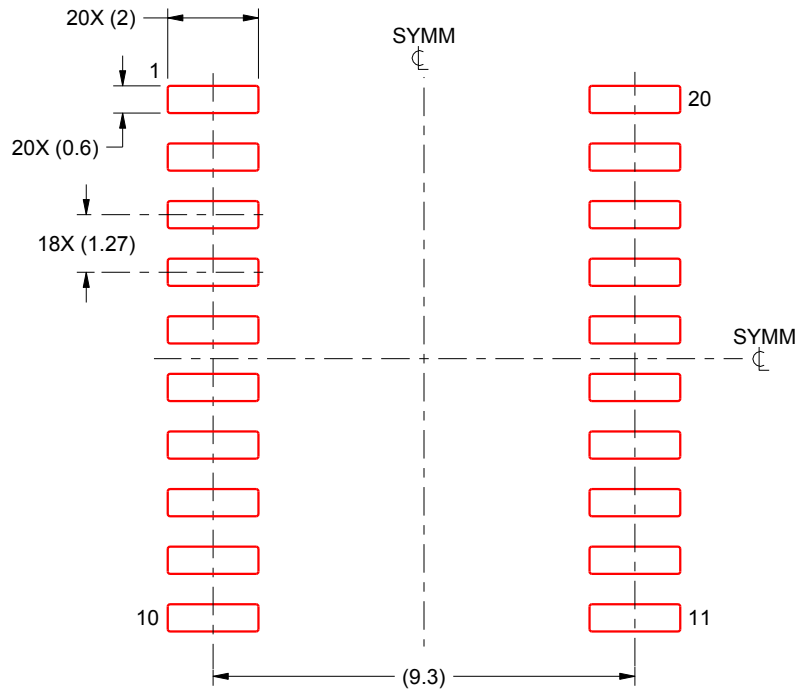**SOLDER MASK DETAILS**

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.