

# CMS06N10V8-HF

**N-Channel  
RoHS Device  
Halogen Free**

## Features

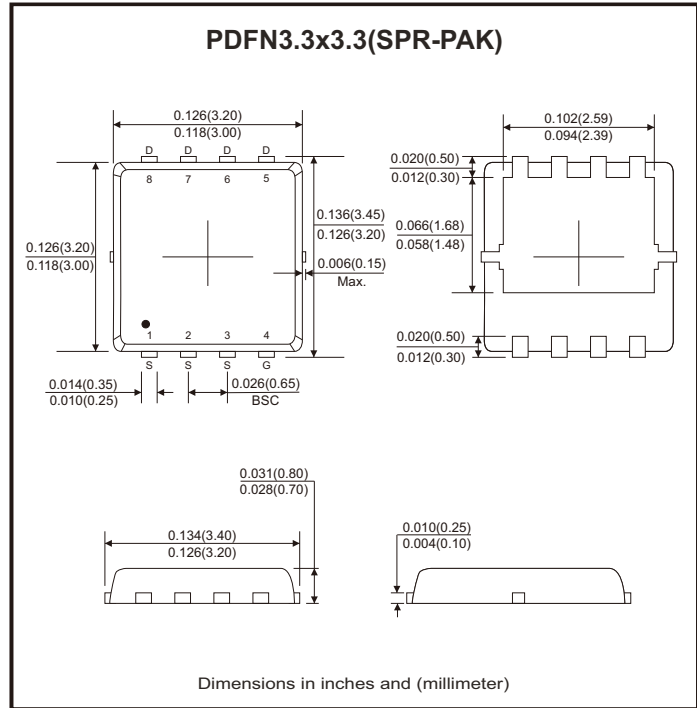
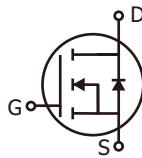
- Advanced high cell density trench technology.
- Super low gate charge.
- Excellent  $cdv/dt$  effect decline.
- Green device available.
- 100% EAS guaranteed.

## Mechanical data

- Case: PDFN3.3x3.3/SPR-PAK standard package, molded plastic.

## Circuit diagram

- G : Gate
- S : Source
- D : Drain



## Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		$V_{DS}$	100	V
Gate-source voltage		$V_{GS}$	$\pm 20$	V
Continuous drain current (Note 1)	$I_D @ T_C = 25^\circ C$		6.8	A
	$I_D @ T_C = 100^\circ C$		4.3	
Pulsed drain current (Note 1, 2)		$I_{DM}$	27	A
Total power dissipation (Note 4)	$P_D @ T_C = 25^\circ C$		10.4	W
	$P_D @ T_A = 25^\circ C$		1.7	
Single pulse avalanche energy, $L=0.1mH$ (Note 3)		$E_{AS}$	6	mJ
Single pulse avalanche current, $L=0.1mH$ (Note 3)		$I_{AS}$	11	A
Operating junction temperature range		$T_J$	-55 to +150	$^\circ C$
Storage temperature range		$T_{STG}$	-55 to +150	$^\circ C$
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	75	$^\circ C/W$
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	12	$^\circ C/W$

## Electrical Characteristics (at T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100			V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.0	1.7	2.5	
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V			±100	nA
Drain-source leakage current (T <sub>J</sub> =25°C)	I <sub>DSS</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V			1	μA
Drain-source leakage current (T <sub>J</sub> =55°C)		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V			5	
Static drain-source on-resistance (Note 2)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		95	105	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A		100	115	
Total gate charge (Note 2)	Q <sub>g</sub>	I <sub>D</sub> = 6A, V <sub>DS</sub> = 80V, V <sub>GS</sub> = 10V		26.2		nC
Gate-source charge	Q <sub>gs</sub>		4.6			
Gate-drain ("miller") charge	Q <sub>gd</sub>		5.1			
Turn-on delay time (Note 2)	t <sub>d(on)</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 10V I <sub>D</sub> = 6A, R <sub>G</sub> = 3.3Ω		4.2		nS
Rise time	t <sub>r</sub>		8.2			
Turn-off delay time	t <sub>d(off)</sub>		35.6			
Fall time	t <sub>f</sub>		9.6			
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		1535		pF
Output capacitance	C <sub>oss</sub>		60			
Reverse transfer capacitance	C <sub>rss</sub>		37			
Gate resistance	R <sub>g</sub>	f = 1MHz		2	4	Ω
<b>Source-drain diode</b>						
Diode forward voltage (Note 2)	V <sub>SD</sub>	I <sub>S</sub> = 7A, V <sub>GS</sub> = 0V, T <sub>J</sub> =25°C			1.2	V
Continuous source current (Note 1, 6)	I <sub>S</sub>	V <sub>G</sub> = V <sub>D</sub> = 0V, Force current			6.8	A
Pulsed source current (Note 2, 6)	I <sub>SM</sub>				27	A
<b>Guaranteed avalanche characteristics</b>						
Single pulse avalanche energy (Note 5)	EAS	V <sub>DD</sub> = 25V, L=0.1mH, I <sub>AS</sub> = 5A	1.25			mJ

- Notes: 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2 oz copper.  
 2. The data tested by pulsed, pulse width ≤300μs, duty cycle ≤ 2%.  
 3. The EAS data shows max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=11A.  
 4. The power dissipation is limited by 150°C junction temperature.  
 5. The min. value is 100% EAS tested guarantee.  
 6. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

## Rating and Characteristic Curves (CMS06N10V8-HF)

Fig.1 - Typical Output Characteristics

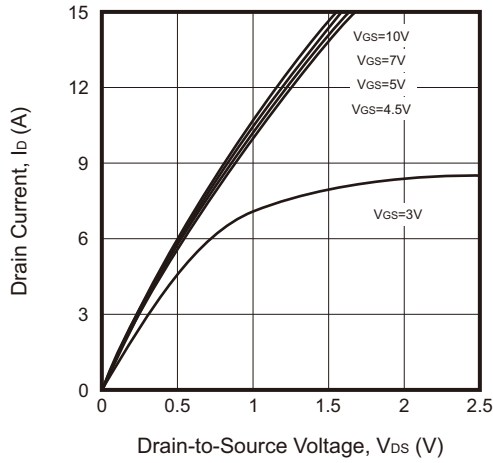


Fig.2 - On-Resistance vs. G-S Voltage

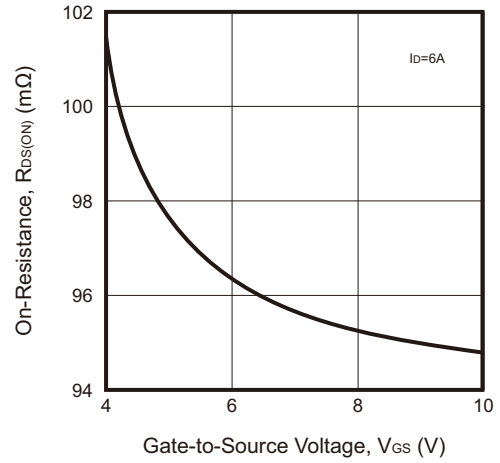


Fig.3 - Normalized  $V_{GS(th)}$  vs.  $T_J$

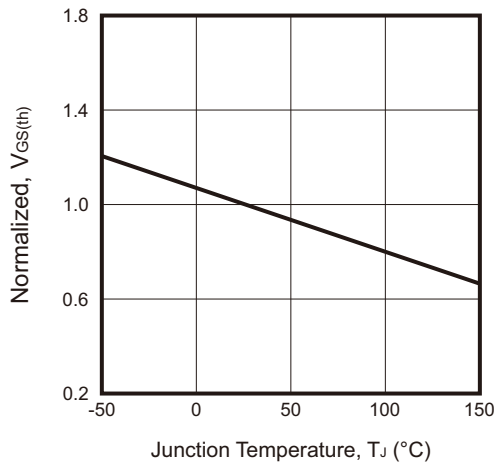


Fig.4 - Normalized  $R_{DS(ON)}$  vs.  $T_J$

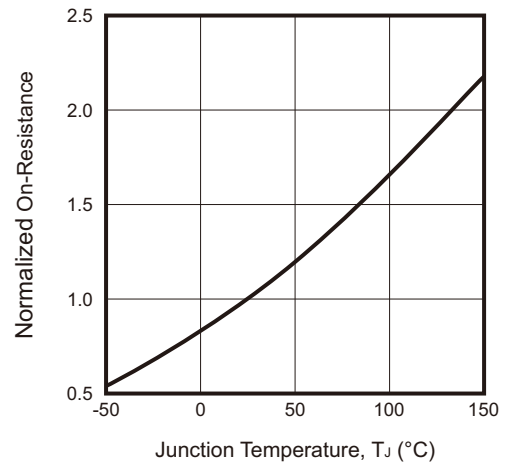


Fig.5 - Safe Operating Area

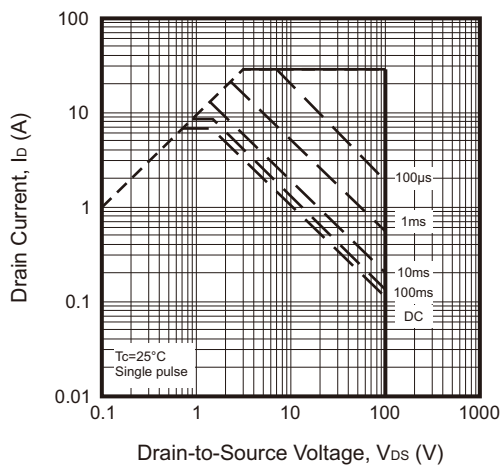
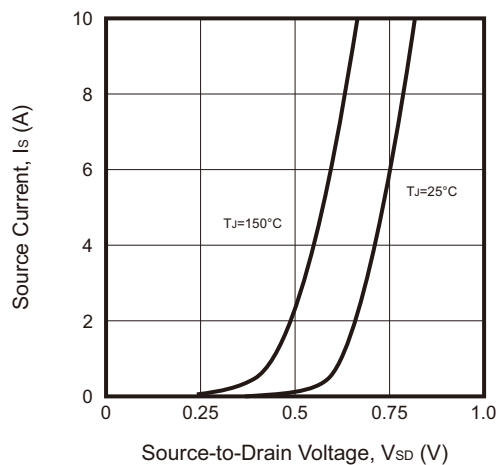


Fig.6 - Forward Characteristics of Reverse



## Rating and Characteristic Curves (CMS06N10V8-HF)

Fig.7 - Gate Charge Characteristics

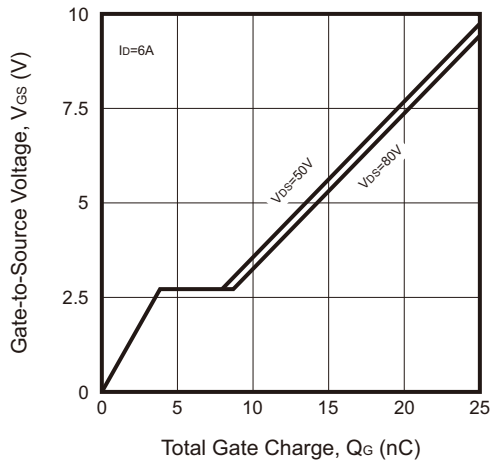
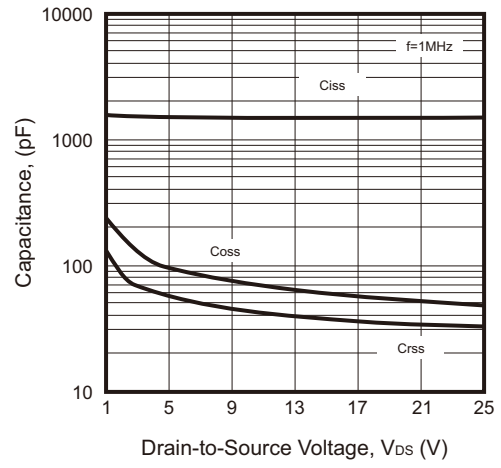
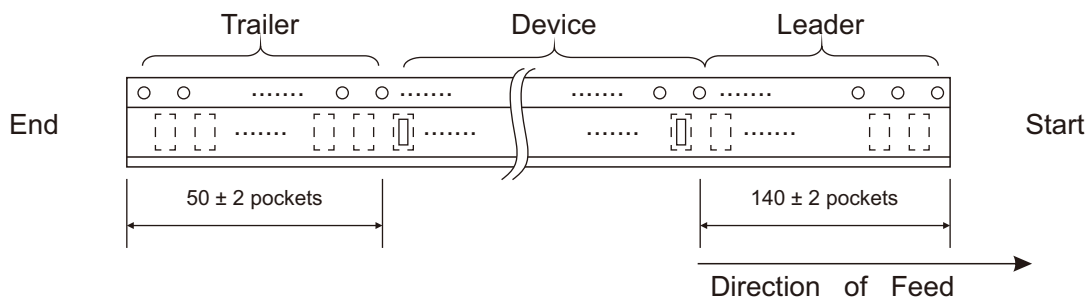
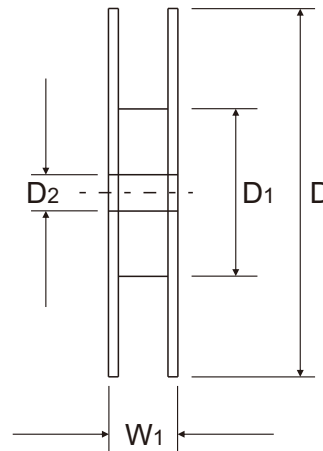
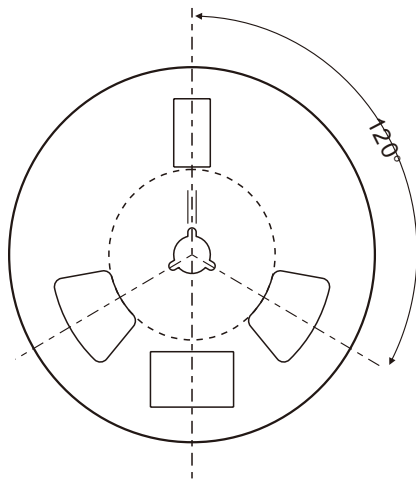
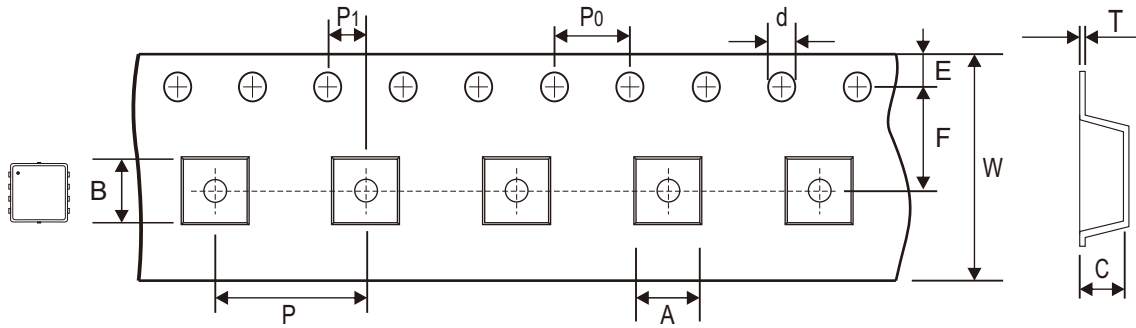


Fig.8 - Capacitance Characteristics



Reel Taping Specification



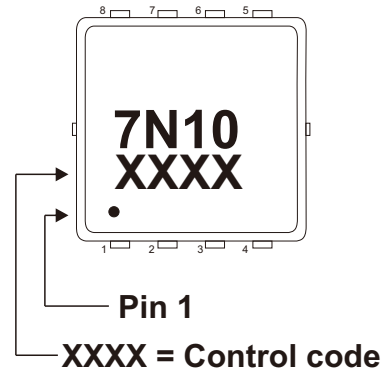
SPR-PAK	SYMBOL	A	B	C	d	D	D1	D2
	(mm)	3.55 ± 0.10	3.55 ± 0.10	1.10 + 0.10 - 0.05	1.50 + 0.10 - 0.00	330.00 ± 1.00	178.00 + 0.00 - 2.00	13.00 min.
	(inch)	0.140 ± 0.004	0.140 ± 0.004	0.043 + 0.004 - 0.002	0.059 + 0.004 - 0.000	12.992 ± 0.039	7.008 + 0.000 - 0.079	0.512 min.

SPR-PAK	SYMBOL	E	F	P	P0	P1	T	W	W1
	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 + 0.30 - 0.10	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 + 0.012 - 0.004	0.724 ref.

Company reserves the right to improve product design , functions and reliability without notice. REV:A

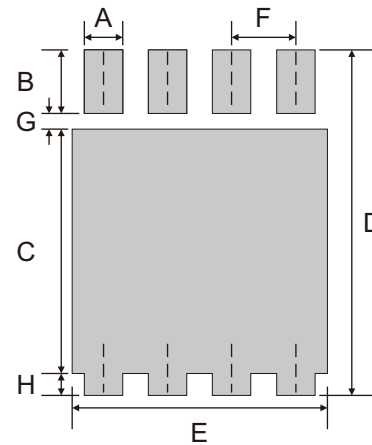
## Marking Code

Part Number	Marking Code
CMS06N10V8-HF	7N10 XXXX



## Suggested PAD Layout

SIZE	SPR-PAK (PDFN3.3x3.3)	
	(mm)	(inch)
A	0.40	0.016
B	0.60	0.024
C	2.35	0.093
D	3.55	0.140
E	2.80	0.110
F	0.65	0.026
G	0.35	0.014
H	0.25	0.010



Note: 1. The pad layout is for reference purposes only.

## Standard Packaging

Case Type	REEL PACK	
	REEL ( pcs )	Reel Size (inch)
SPR-PAK (PDFN3.3x3.3)	3000	13