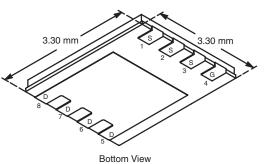


**Vishay Siliconix** 

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>f</sup>	Q <sub>g</sub> (Typ.)			
30	0.006 at V <sub>GS</sub> = 10 V	35 <sup>g</sup>	13.7 nC			
	0.0082 at $V_{GS}$ = 4.5 V	35 <sup>g</sup>	13.7 110			



PowerPAK 1212-8

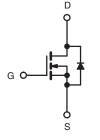


- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- **PWM Optimized**
- 100 % R<sub>a</sub> Tested
- 100 % UIS Tested

#### **APPLICATIONS**

High Side Switch





Ordering Information: Si7718DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATIN	I <b>GS</b> T <sub>A</sub> = 25 °C,	unless othe	rwise noted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	v	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		35 <sup>g</sup>		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	- I <sub>D</sub> -	35 <sup>g</sup>		
Continuous Drain Current $(1) = 150^{\circ}$ C)	T <sub>A</sub> = 25 °C		18.5 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		16.9 <sup>a, b</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	70	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	- I <sub>S</sub>	35 <sup>g</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C		3.3 <sup>a, b</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Energy		E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		52		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P	43	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 <sup>a, b</sup>	vv	
	T <sub>A</sub> = 70 °C		3.1 <sup>a, b</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>		Ŭ	260		

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, e</sup>	t ≤ 10 s	R <sub>thJA</sub>	24	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.9	2.4	0/11	

#### Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

- c. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
  d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
  e. Maximum under steady state conditions is 81 °C/W.

f. Based on  $T_C = 25$  °C. g. Package limited.





# Vishay Siliconix

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_{D} = 250 \mu A$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L _ 250 uA		30		mV/°0	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.2		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5$ V, $V_{GS}$ = 10 V	20			A	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.0048	0.006		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_{D} = 7 \text{ A}$		0.0065	0.0082	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		50		S	
Dynamic <sup>b</sup>					<b></b>		
Input Capacitance	C <sub>iss</sub>			1600		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		335			
Reverse Transfer Capacitance	C <sub>rss</sub>			115			
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		30	45	45 21 nC	
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		13.7	21		
Gate-Source Charge	Q <sub>gs</sub>			4.3			
Gate-Drain Charge	Q <sub>gd</sub>			4.3			
Gate Resistance	Rg	f = 1 MHz	0.3	0.75	1.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			22	35	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, \text{ R}_{L} = 1.5 \Omega$		13	26		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		26	45		
Fall Time	t <sub>f</sub>			12	24		
Turn-On Delay Time	t <sub>d(on)</sub>			13	26		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		9	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10$ Å, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		22	35		
Fall Time	t <sub>f</sub>	-		8	16		
Drain-Source Body Diode Characteristi	cs				1		
Continuous Source-Drain Diode Current	ا <sub>S</sub>	T <sub>C</sub> = 25 °C			35		
Pulse Diode Forward Current	I <sub>SM</sub>				70	A	
Body Diode Voltage	V <sub>SD</sub>	$I_{S} = 3 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			19	35	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			9.5	18	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		11		+	
Reverse Recovery Rise Time t <sub>b</sub>		1		8		ns	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.

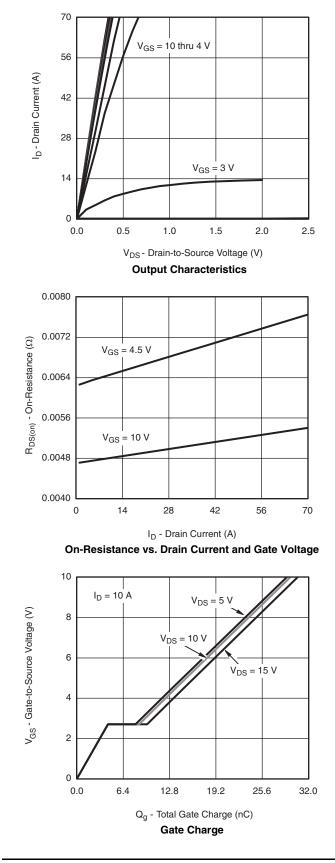
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

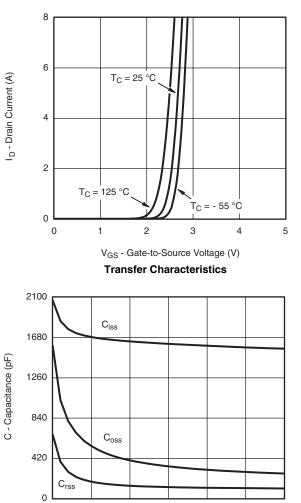




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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







15

20

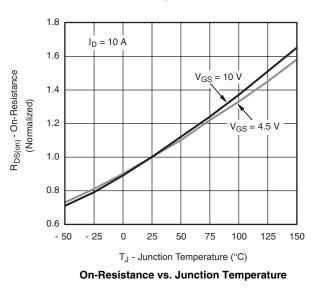
25

30

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5

10



Document Number: 68698 S-81584-Rev. A, 07-Jul-08

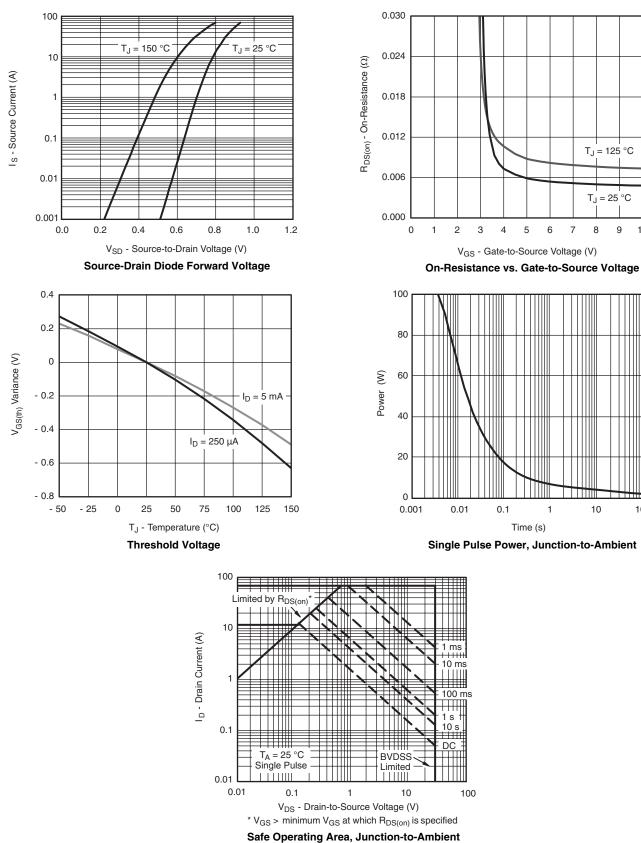
## Vishay Siliconix



10

100

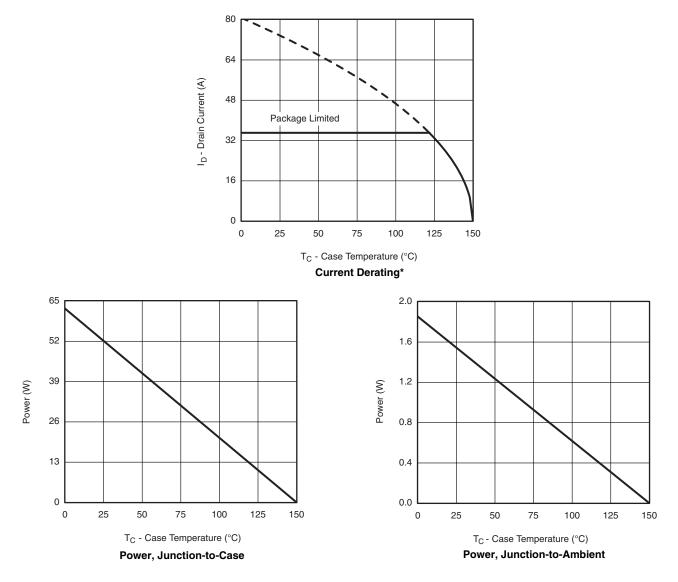
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





## Si7718DN Vishay Siliconix

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

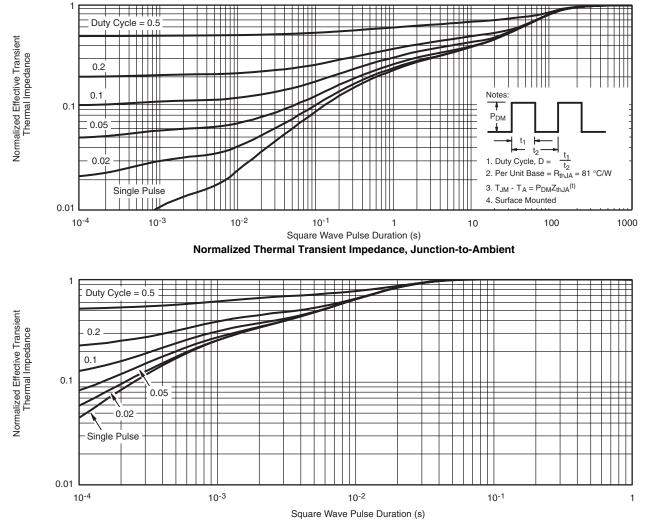


\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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## Vishay Siliconix

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68698.



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