

# 74ALVC162834A

18-bit registered driver with inverted register enable and 30  $\Omega$  termination resistors; 3-state

Rev. 3 — 13 June 2017

Product data sheet

## 1 General description

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The 74ALVC162834A is an 18-bit registered driver. Data flow is controlled by active low output enable ( $\overline{OE}$ ), active low latch enable ( $\overline{LE}$ ) and clock inputs (CP).

When  $\overline{LE}$  is LOW, the A to Y data flow is transparent. When  $\overline{LE}$  is HIGH and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

The 74ALVC162834A is designed with 30  $\Omega$  series resistors in both HIGH or LOW output stages.

When  $\overline{OE}$  is LOW the outputs are active. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 2 Features and benefits

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- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Current drive  $\pm 12$  mA at 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Output drive capability 50  $\Omega$  transmission lines at 85°C
- Integrated 30  $\Omega$  termination resistors
- Diode clamps to  $V_{CC}$  and GND on all inputs
- Input diodes to accommodate strong drivers
- Complies with JEDEC standard no. 8-1A

## 3 Ordering information

Table 1. Ordering information

Type number	Package	Name	Description	Version
	Temperature range			
74ALVC162834ADGG	-40 °C to + 85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

## 4 Functional diagram

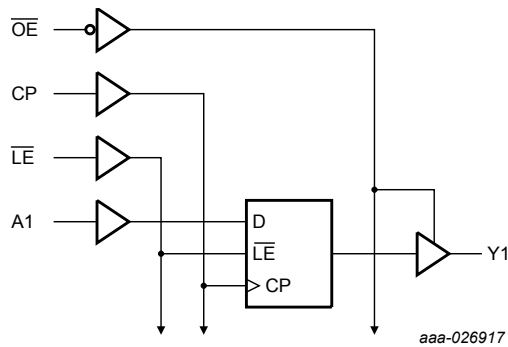


Figure 1. Logic diagram

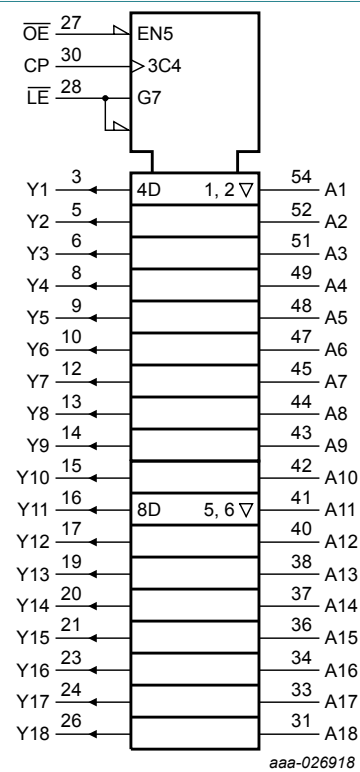


Figure 2. Logic symbol (IEEE/IEC)

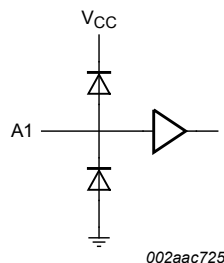


Figure 3. Typical input (data or control)

## 5 Pinning information

### 5.1 Pinning

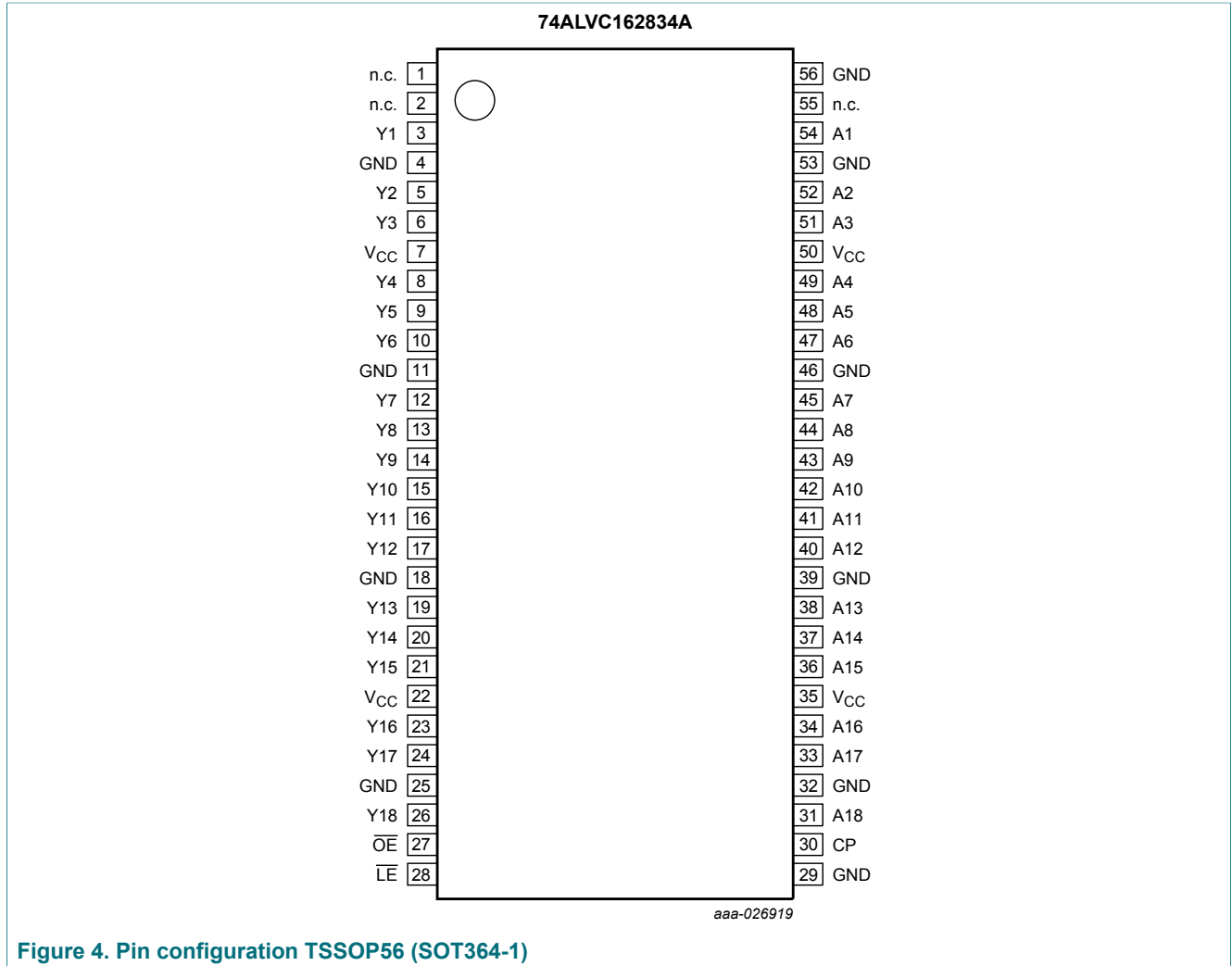


Figure 4. Pin configuration TSSOP56 (SOT364-1)

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18	54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18	3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
n.c.	1, 2, 55	no connected
$\overline{\text{LE}}$	28	latch enable input (active LOW)
$\overline{\text{OE}}$	27	output enable input (active LOW)
CP	30	clock input (LOW-to-HIGH, edge-triggered)
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Input				Output
$\overline{\text{OE}}$	$\overline{\text{LE}}$	CP	A <sub>n</sub>	Y <sub>n</sub>
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y <sub>0</sub> <sup>[2]</sup>
L	H	L	X	Y <sub>0</sub> <sup>[3]</sup>

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

[2] Y<sub>0</sub> = Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.

[3] Y<sub>0</sub> = Output level before the indicated steady-state input conditions were established.

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+4.6	V
$V_O$	output voltage		[1] -0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation		[2] -	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP56 package:  $P_{tot}$  derates linearly with 8 mW/K above 55  $^{\circ}$ C.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	maximum speed performance				
		$V_{CC} = 2.5$ V; $C_L = 30$ pF	2.3	-	2.7	V
		$V_{CC} = 3.3$ V; $C_L = 50$ pF	3.0	-	3.6	V
		LOW-voltage applications	1.2	-	3.6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	operating in free-air	-40	-	+85	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		V <sub>CC</sub> = 2.3 V to 3.6 V; I <sub>O</sub> = -100 $\mu$ A	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = -4 mA	V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.11	-	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = -6 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.17	-	V
		V <sub>CC</sub> = 2.7 V; I <sub>O</sub> = -4 mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.09	-	V
		V <sub>CC</sub> = 2.7 V; I <sub>O</sub> = -8 mA	V <sub>CC</sub> - 0.7	V <sub>CC</sub> - 0.19	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = -6 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.13	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		V <sub>CC</sub> = 2.3 V to 3.6 V; I <sub>O</sub> = 100 $\mu$ A	-	GND	0.20	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = 4 mA	-	0.07	0.40	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = 6 mA	-	0.11	0.55	V
		V <sub>CC</sub> = 2.7 V; I <sub>O</sub> = 4 mA	-	0.06	0.40	V
		V <sub>CC</sub> = 2.7 V; I <sub>O</sub> = 8 mA	-	0.13	0.60	V
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = 6 mA	-	0.09	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	$\mu$ A
		V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	$\mu$ A
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	150	750	$\mu$ A
C <sub>i</sub>	input capacitance		-	4.0	-	pF
C <sub>O</sub>	output capacitance		-	8.0	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C

Typical values for V<sub>CC</sub> = 2.3 V to 2.7 V are measured at V<sub>CC</sub> = 2.5 V

Typical values for V<sub>CC</sub> = 3.0 V to 3.6 V are measured at V<sub>CC</sub> = 3.3 V

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 11](#).

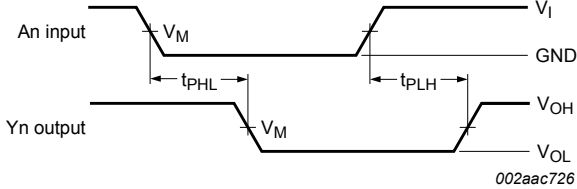
Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$t_{pd}$	propagation delay	An to Yn; <a href="#">Figure 5</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.5	5.2	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.3	5.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.9	4.2	ns
		$\overline{\text{LE}}$ to Yn; <a href="#">Figure 6</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.3	4.1	6.0	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.8	6.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	3.4	5.8	ns
		CP to Yn; <a href="#">Figure 8</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	4.0	6.8	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.7	6.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	3.3	5.4	ns
$t_{en}$	enable time	$\overline{\text{OE}}$ to Yn; <a href="#">Figure 10</a> <sup>[3]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	3.8	6.3	ns
		$V_{CC} = 2.7 \text{ V}$	-	4.0	6.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	2.4	5.9	ns
$t_{dis}$	disable time	$\overline{\text{OE}}$ to Yn; <a href="#">Figure 10</a> <sup>[4]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.6	4.4	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.2	5.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.8	3.0	5.0	ns
$t_w$	pulse width	CP HIGH or LOW; <a href="#">Figure 8</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	3.3	1.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.3	1.2	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	0.7	-	ns
		$\overline{\text{LE}}$ HIGH; see <a href="#">Figure 6</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V};$	3.3	0.7	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.3	0.6	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	0.6	-	ns
$t_{su}$	set-up time	An to CP; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$ ; <a href="#">Figure 9</a>	1.0	-	-	ns
		An to $\overline{\text{LE}}$ ; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$ ; <a href="#">Figure 7</a>	1.5	-	-	ns
$t_h$	hold time	An to CP; <a href="#">Figure 9</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	0.4	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.2	0.4	-	ns

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.9	0.7	-	ns
		An to $\overline{\text{LE}}$ ; <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	0.1	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0.4	-	ns
f <sub>max</sub>	maximum frequency	CP; <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.3 V to 2.7 V	150	190	-	MHz
		V <sub>CC</sub> = 2.7 V	150	190	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	150	240	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per driver; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>				
		transparent mode; output enabled	-	10	-	pF
		transparent mode; output disabled	-	3	-	pF
		clocked mode; output enabled	-	21	-	pF
		clocked mode; output disabled	-	15	-	pF

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C  
 Typical values for V<sub>CC</sub> = 2.3 V to 2.7 V are measured at V<sub>CC</sub> = 2.5 V  
 Typical values for V<sub>CC</sub> = 3.0 V to 3.6 V are measured at V<sub>CC</sub> = 3.3 V
- [2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [3] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.
- [4] t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

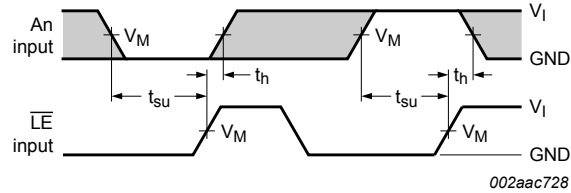


10.1 Waveforms and test circuit



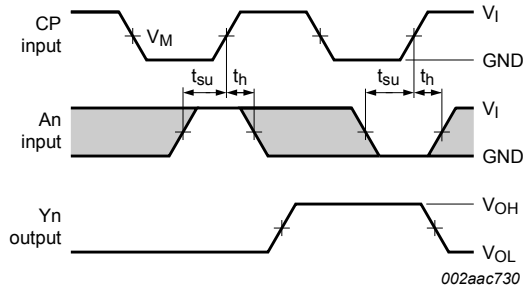
Measurement points are given in Table 8.  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Figure 5. Input (An) to output (Yn) propagation delay



Measurement points are given in Table 8. The shaded areas indicate when the input is permitted to change for predictable output performance.

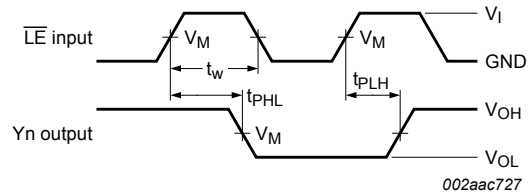
Figure 7. Data set-up and hold times, An input to LE input



Measurement points are given in Table 8.  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

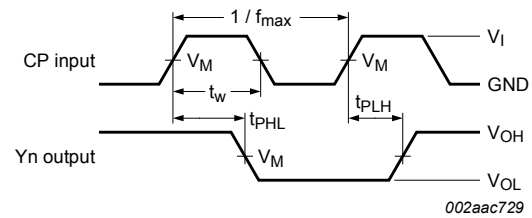
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 9. Data set-up and hold times, An input to CP input



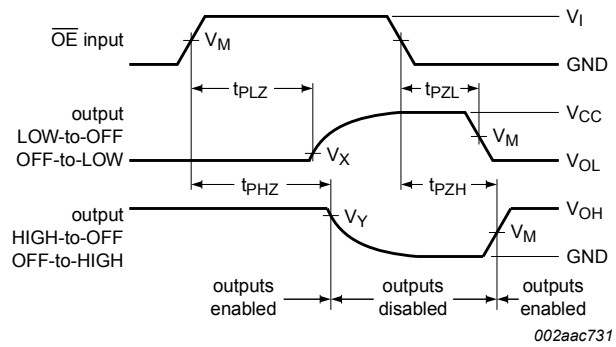
Measurement points are given in Table 8.  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Figure 6. LE input pulse width, LE input to Yn output propagation delays



Measurement points are given in Table 8.  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Figure 8. CP to Yn propagation delays, clock pulse width and maximum clock frequency



Measurement points are given in Table 8.  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Figure 10. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
≤ 2.3 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.3 V to 2.7 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

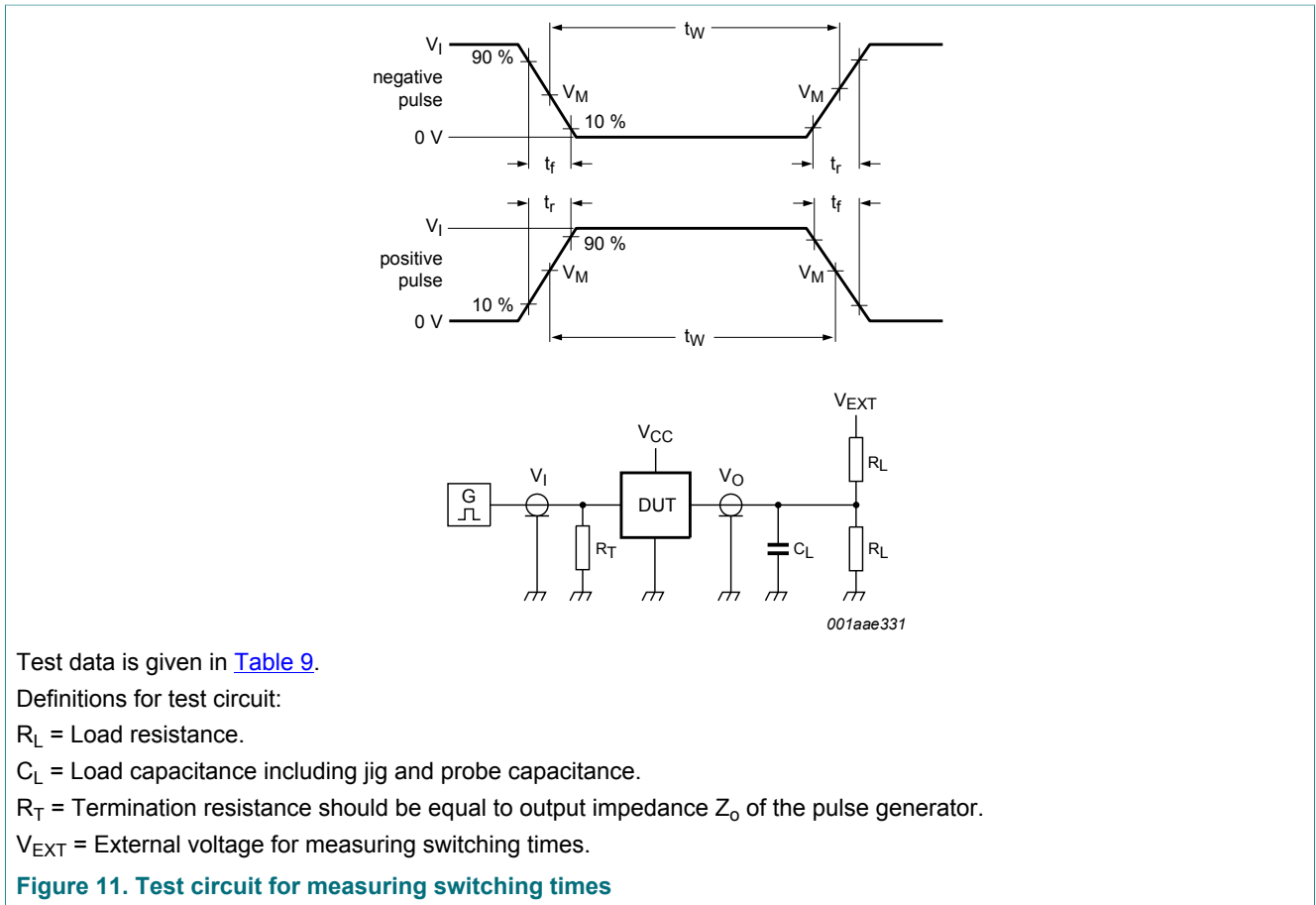


Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
≤ 2.3 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND

## 11 Package outline

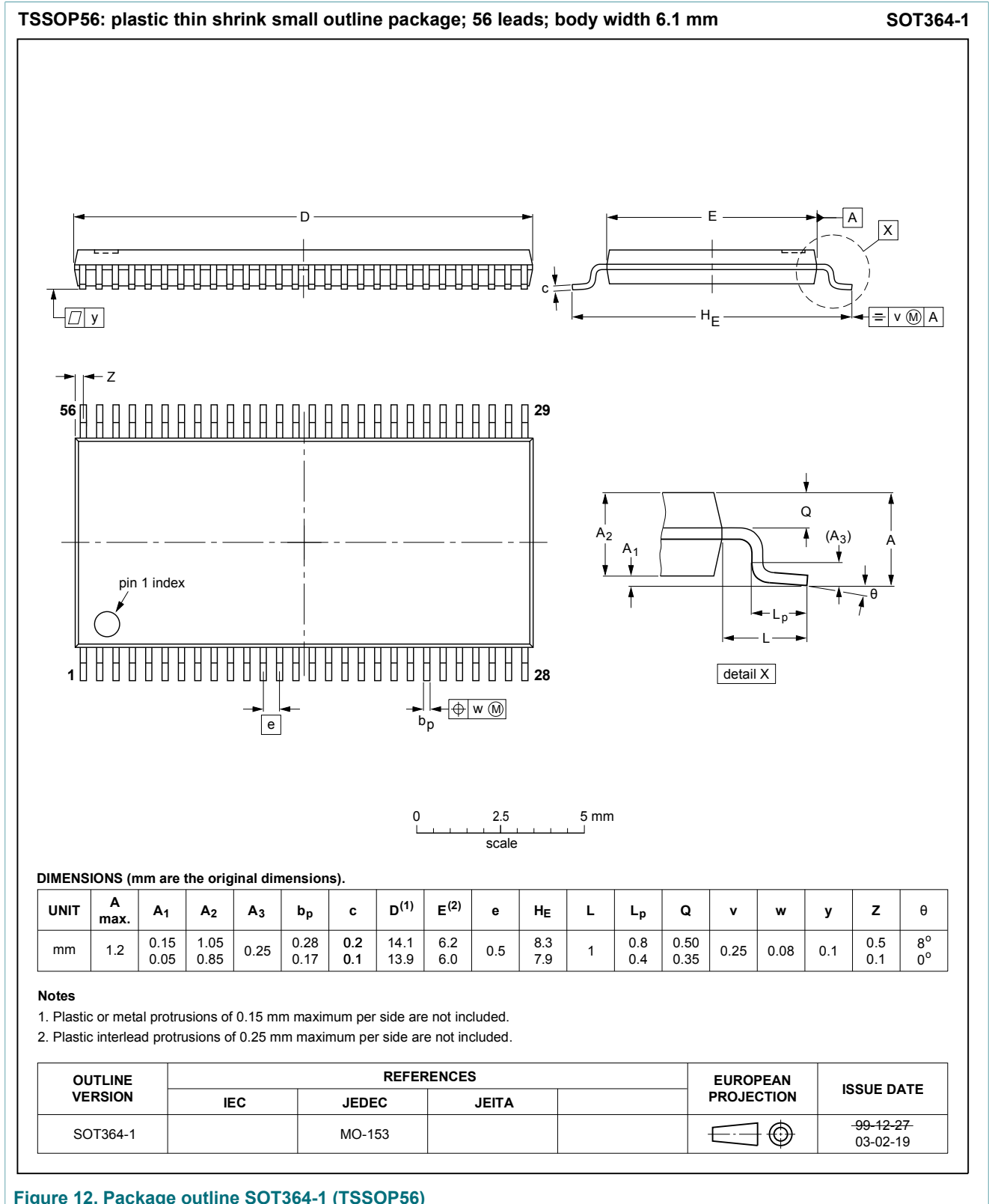


Figure 12. Package outline SOT364-1 (TSSOP56)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC162834A v.3	20170613	Product data sheet	-	74ALVC162834A v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ALVC162834A v.2	20000620	Product specification	-	74ALVC162834A v.1
74ALVC162834A v.1	20000314	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

### 14.2 Definitions

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**18-bit registered driver with inverted register enable and 30  $\Omega$  termination resistors; 3-state**

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