

74HC4020; 74HCT4020

14-stage binary ripple counter

Rev. 5 — 6 August 2012

Product data sheet

1. General description

The 74HC4020; 74HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4020B series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4020; 74HCT4020 are 14-stage binary ripple counters with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0, Q3 to Q13). The counter advances on the HIGH-to-LOW transition of \overline{CP} .

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} .

Each counter stage is a static toggle flip-flop.

2. Features and benefits

- Multiple package options
- Complies with JEDEC standard no. 7A
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4020N 74HCT4020N	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC4020D 74HCT4020D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4020DB 74HCT4020DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1



Table 1. Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
74HC4020PW 74HCT4020PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4020BQ 74HCT4020BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

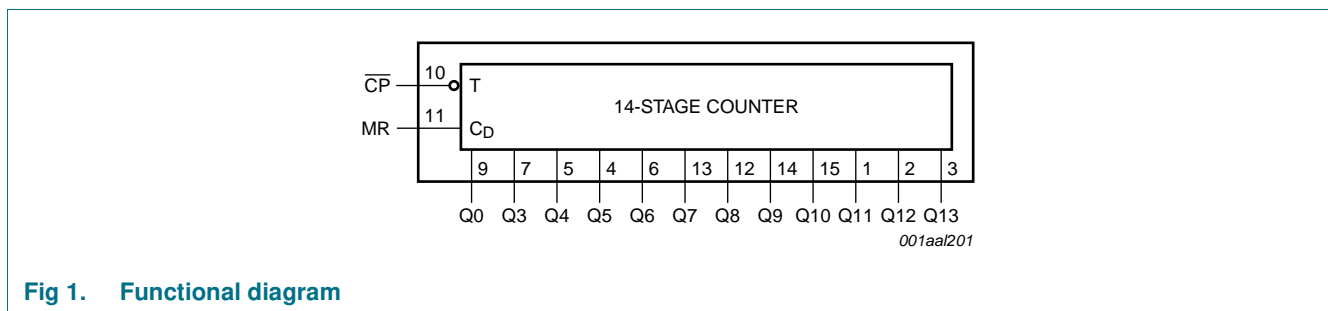


Fig 1. Functional diagram

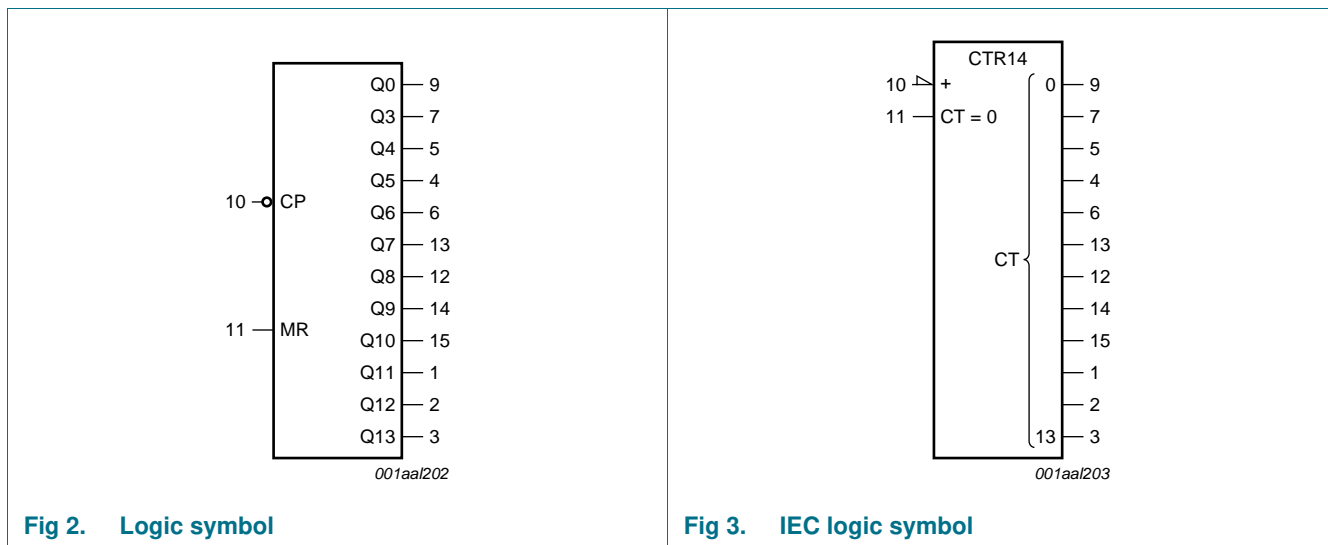


Fig 2. Logic symbol

Fig 3. IEC logic symbol

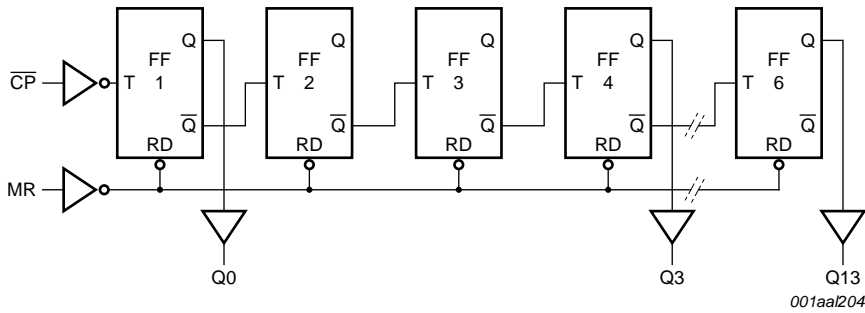


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

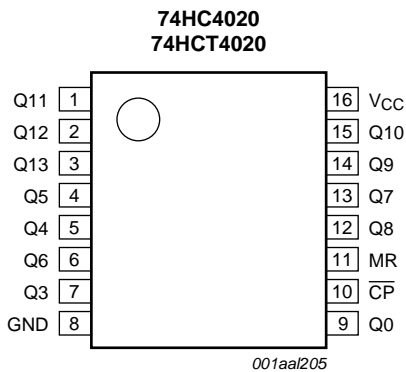
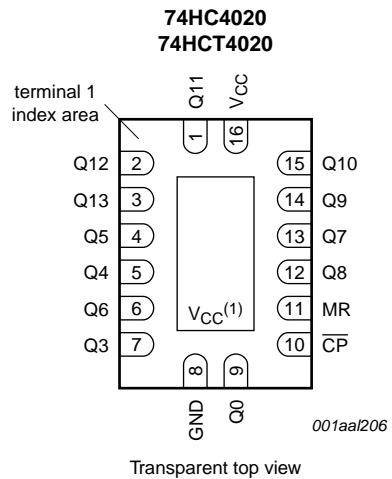


Fig 5. Pin configuration DIP16, SO16, SSOP16 and TSSOP16



- (1) The substrate is attached to this pad using conductive die attach material. It cannot be used as supply pin or input. It is recommended that no connection is made at all.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q3 to Q13	9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	output
GND	8	ground (0 V)
CP	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
VCC	16	positive supply voltage

7. Functional description

Table 3. Function table

Input		Output
CP	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

7.1 Timing diagram

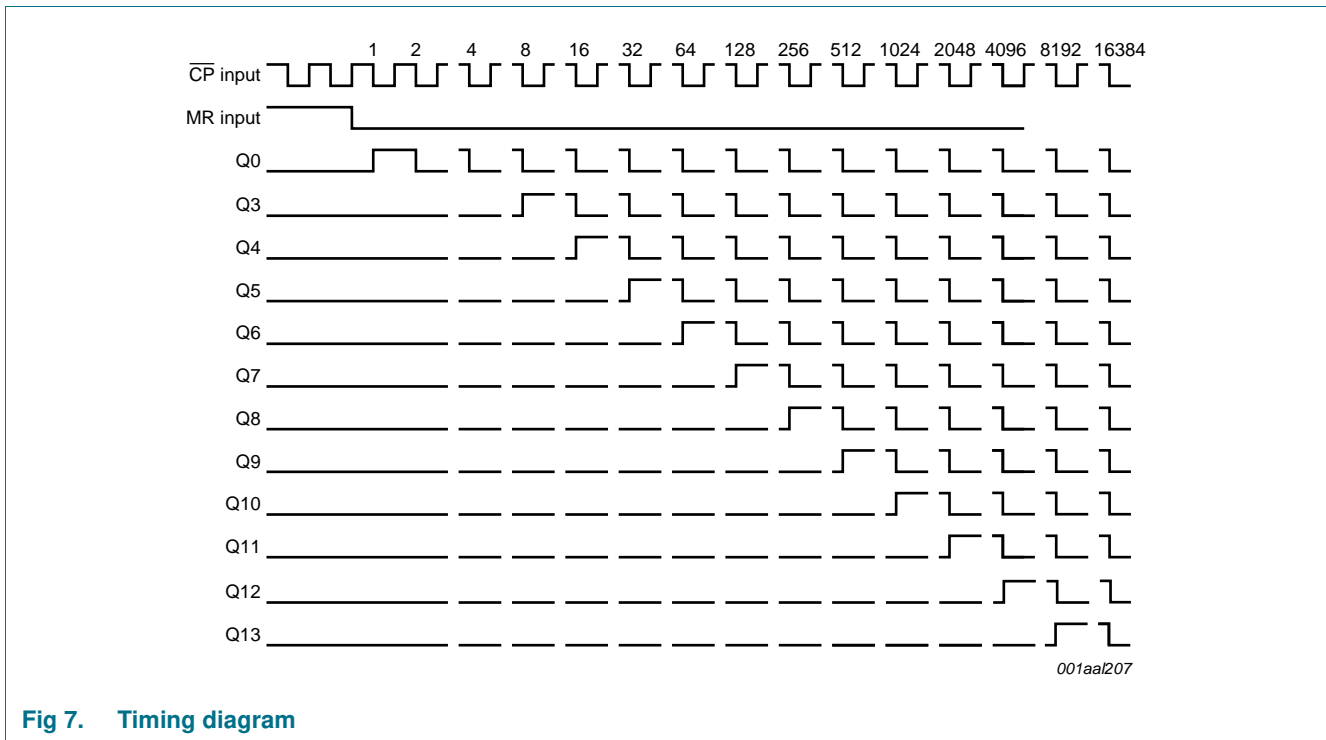


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	± 50	mA
I_{GND}	ground current		-	± 50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[1]		
	DIP16 package		-	750	mW
	SO16, SSOP16, TSSOP16 and DHVQFN16 packages		-	500	mW

- [1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4020			74HCT4020			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	except for Schmitt trigger inputs							
		$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
		I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4020										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
V _{OL}	LOW-level output voltage	I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
		V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
I _I	input leakage current	I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	μ A
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	-	-	-	-	-	-
		pin MR	-	110	396	-	495	-	539	μ A
		pin \overline{CP}	-	85	306	-	383	-	417	μ A
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020										
t_{pd}	propagation delay	\overline{CP} to Q0; see Figure 8 [1]	-	-	-	-	-	-	-	-
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	39	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	14	28	-	35	-	42	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns
	$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	11	24	-	30	-	36	ns	
	Qn to Qn+1; see Figure 9	$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	22	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	8	15	-	19	-	22	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	6	-	-	-	-	-	ns
$V_{CC} = 6.0$ V; $C_L = 50$ pF		-	6	13	-	16	-	19	ns	
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 8	-	-	-	-	-	-	-	-
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	55	170	-	215	-	225	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	20	34	-	43	-	51	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
t_t	transition time	Qn; see Figure 8 [2]	-	-	-	-	-	-	-	-
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics ...continued
 GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_w	pulse width	\overline{CP} HIGH or LOW; see Figure 8								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	16	4	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	14	3	-	17	-	20	-	ns
		MR HIGH; see Figure 8								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	16	6	-	20	-	24	-	ns
t_{rec}	recovery time	MR to \overline{CP} ; see Figure 8								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	50	6	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	10	2	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	9	2	-	11	-	13	-	ns
f_{max}	maximum frequency	see Figure 8								
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	6.0	30	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	30	92	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	101	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	35	109	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance		[3]	-	19	-	-	-	-	pF

74HCT4020

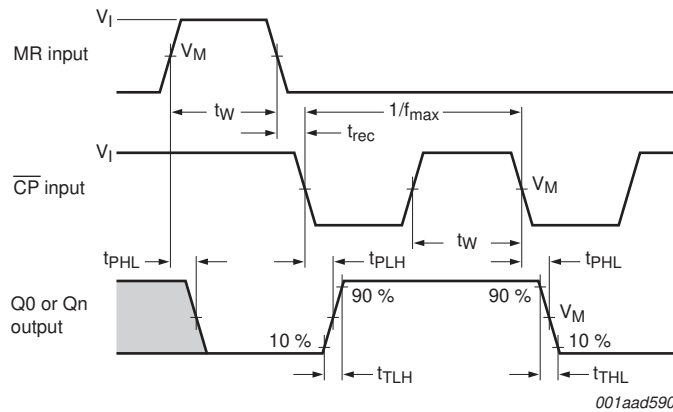
t_{pd}	propagation delay	\overline{CP} to Q0; see Figure 8		[1]						
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	18	36	-	45	-	54	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		Qn to Qn+1; see Figure 9								
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	8	15	-	19	-	22	ns
t_{PHL}	HIGH to LOW propagation delay	$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	22	45	-	56	-	68	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
t_t	transition time	Qn; see Figure 8		[2]						
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	-	7	15	-	19	-	22	ns
t_w	pulse width	\overline{CP} HIGH or LOW; see Figure 8								
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	20	7	-	25	-	30	-	ns
		MR HIGH; see Figure 8								
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	20	8	-	25	-	30	-	ns
t_{rec}	recovery time	MR to \overline{CP} ; see Figure 8								
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	10	2	-	13	-	15	-	ns

Table 7. Dynamic characteristics ...continued
 GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	see Figure 8								
		$V_{\text{CC}} = 4.5 \text{ V}; C_L = 50 \text{ pF}$	25	47	-	20	-	17	-	MHz
		$V_{\text{CC}} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	52	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	[3]	-	20	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_i is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i + \Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 $\Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

12. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Clock timing, propagation delays, pulse widths and measurement points

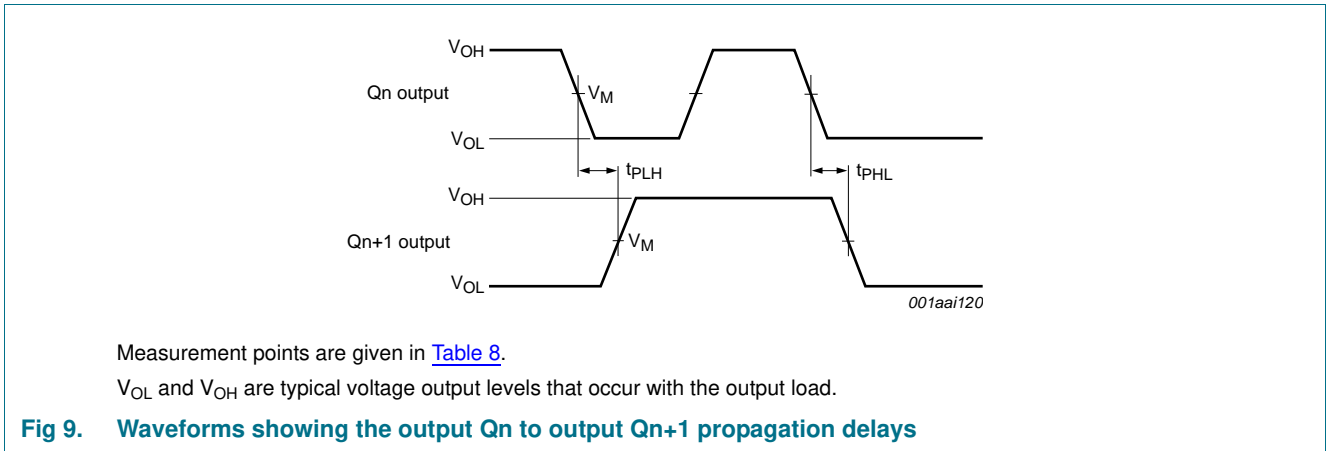
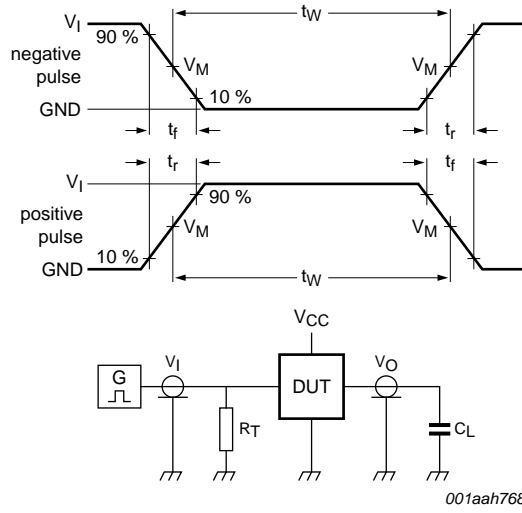


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC4020	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4020	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4020	V_{CC}	6 ns	15 pF, 50 pF
74HCT4020	3 V	6 ns	15 pF, 50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

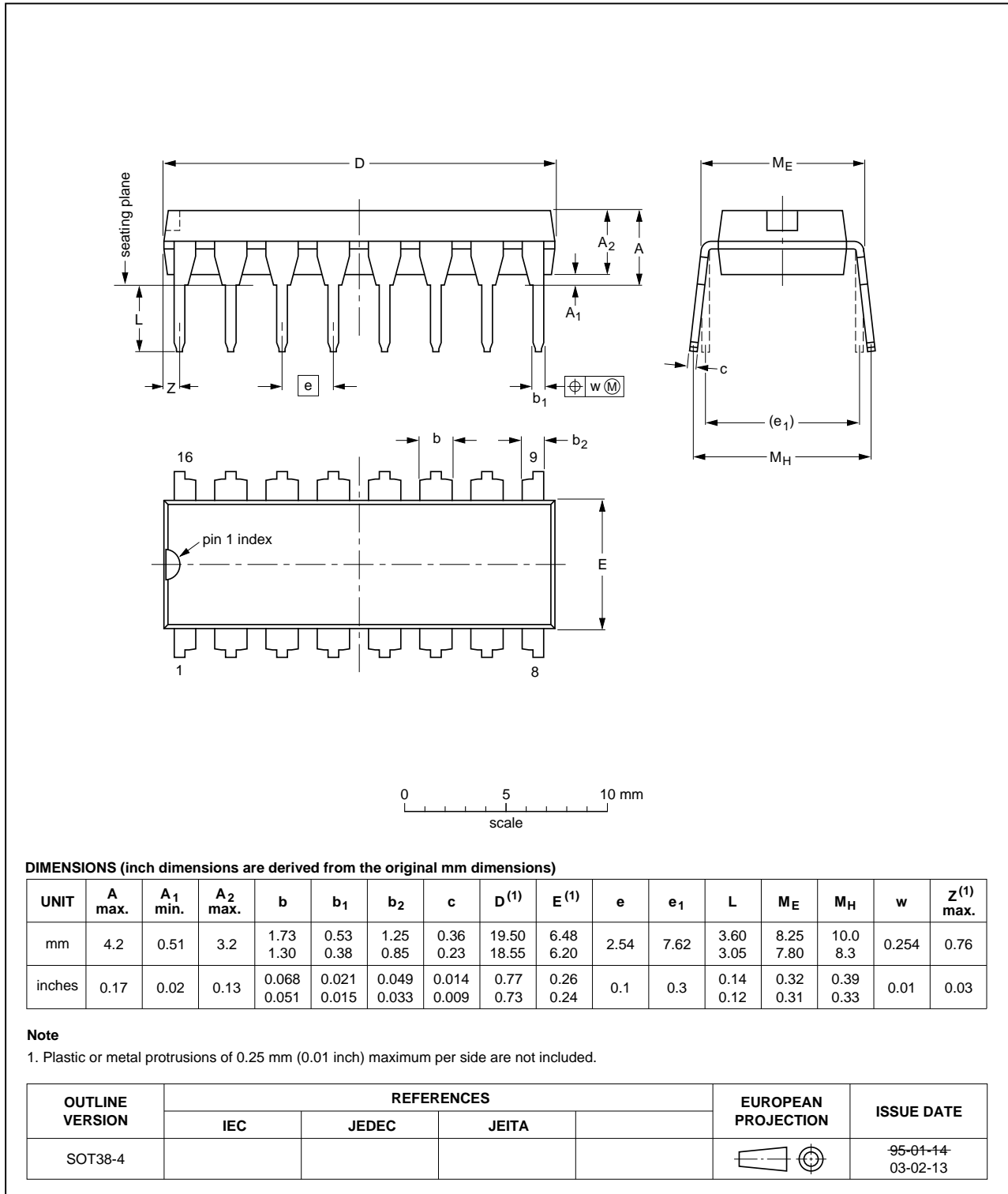


Fig 11. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

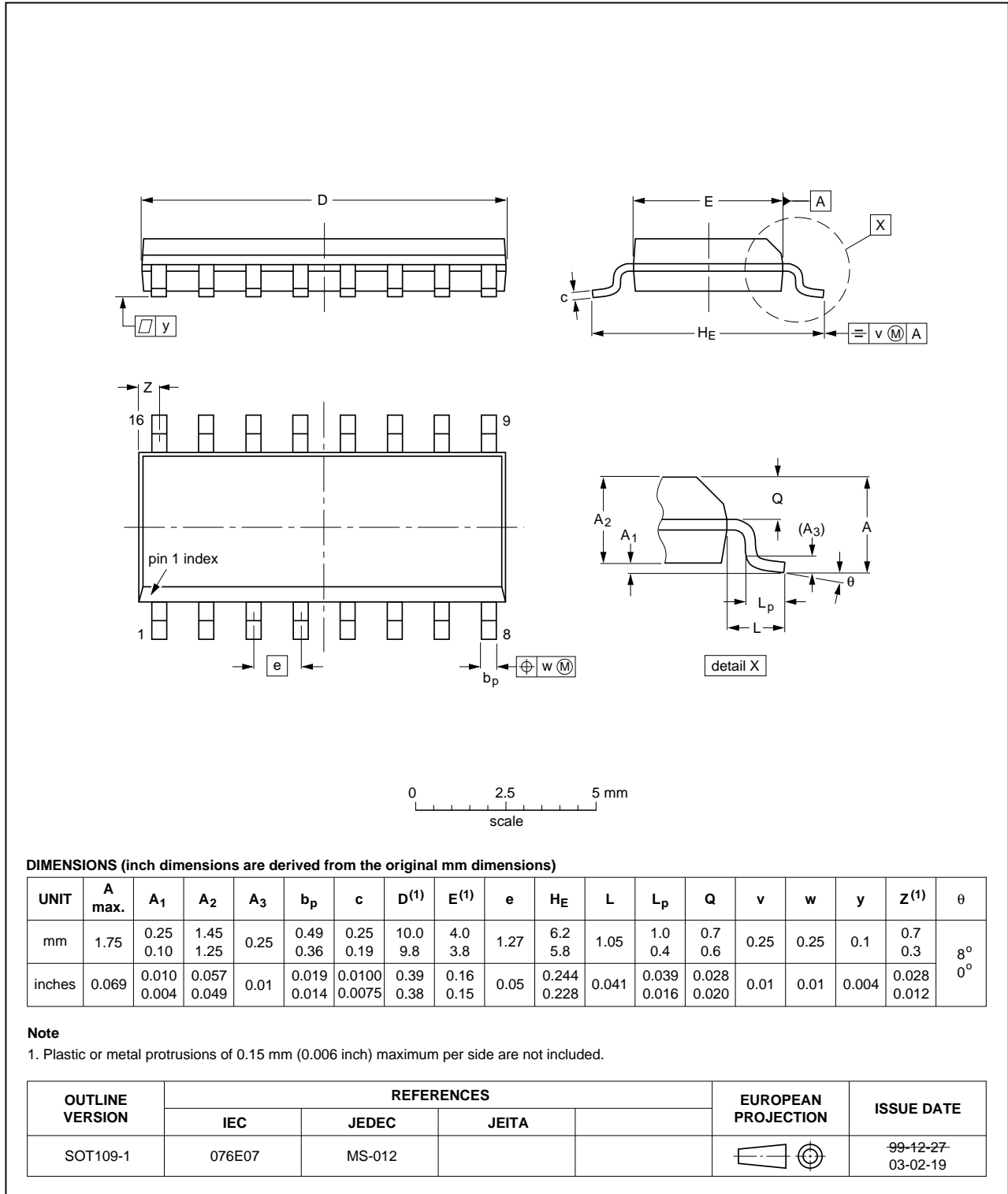


Fig 12. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

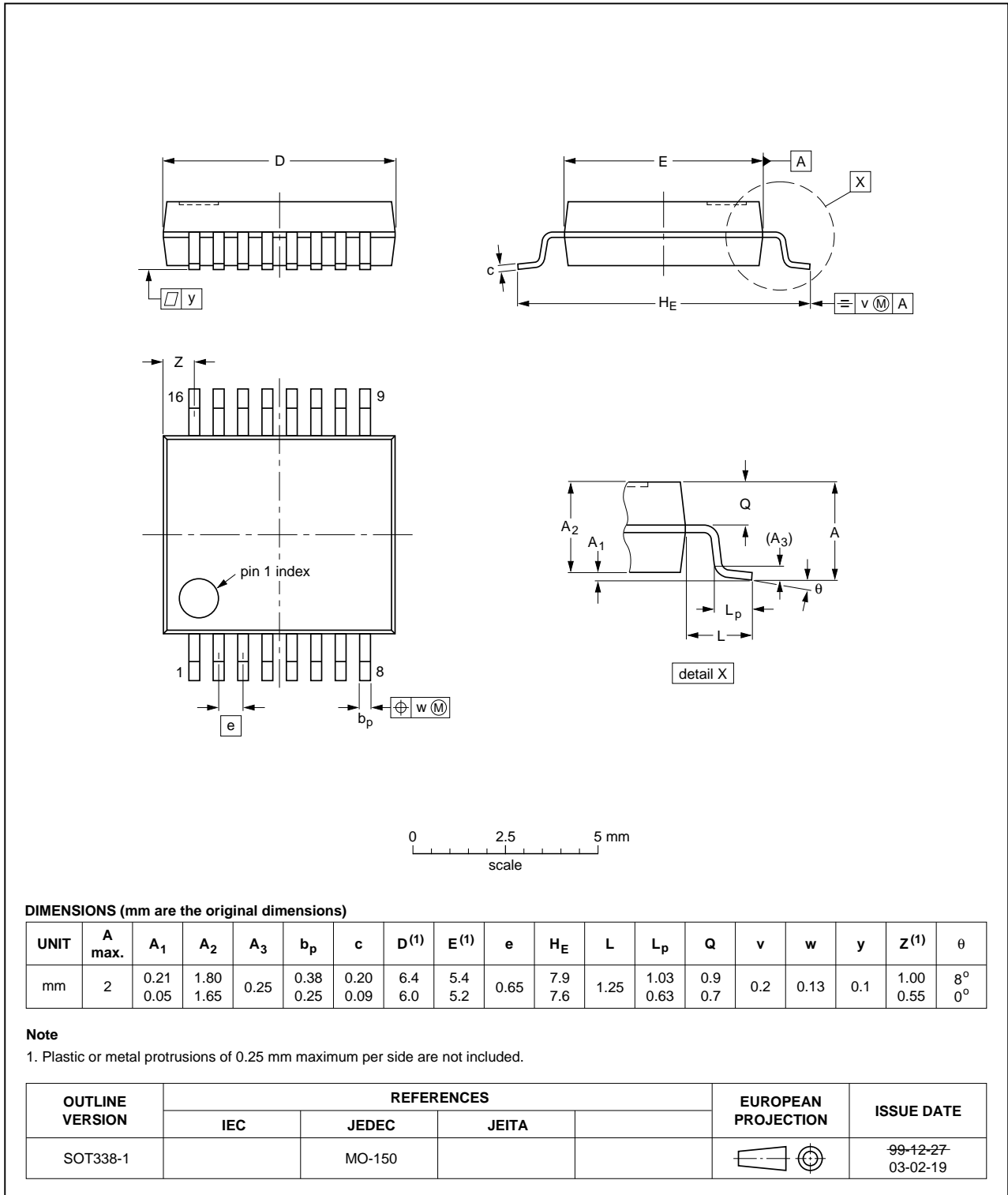


Fig 13. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

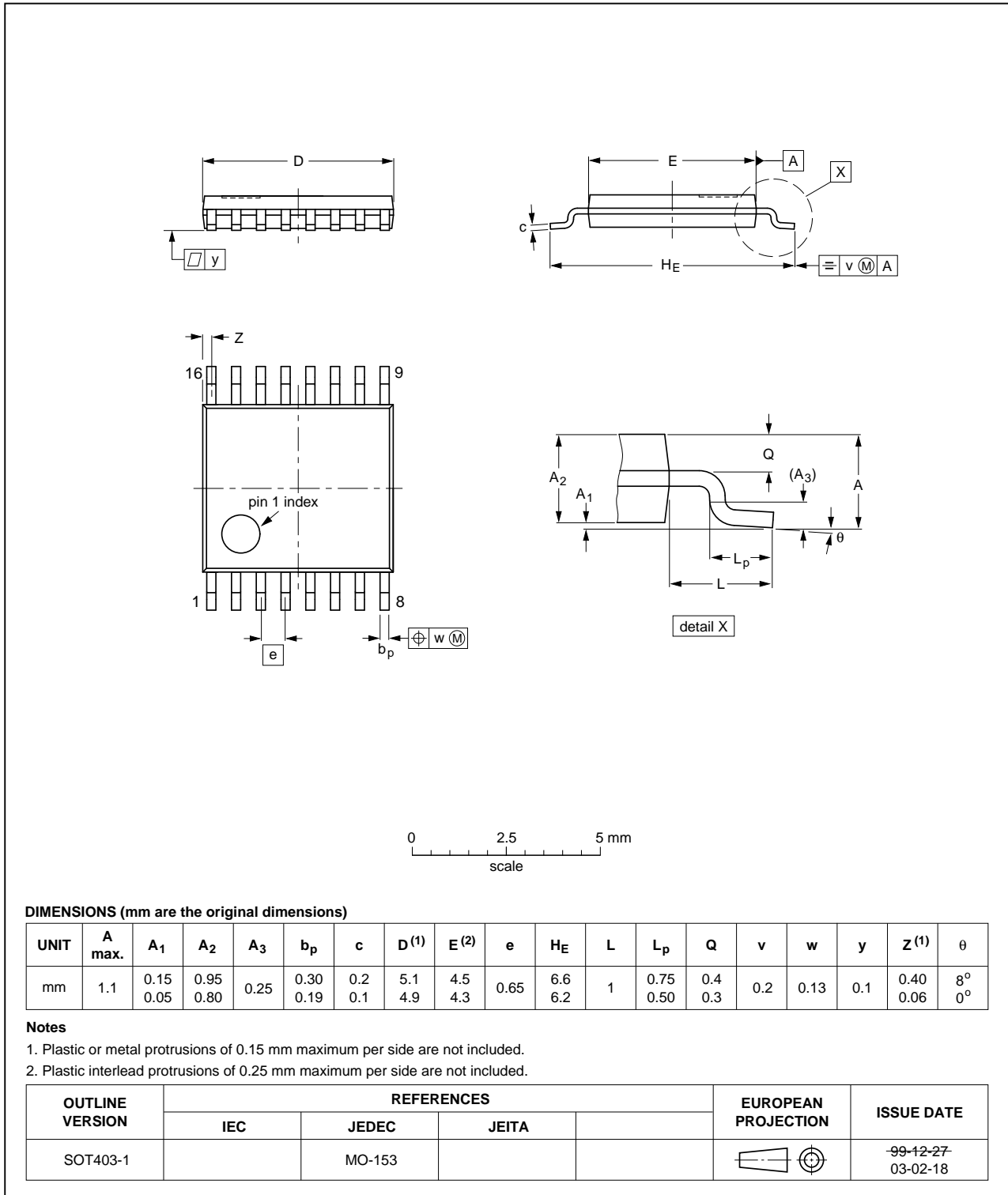


Fig 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

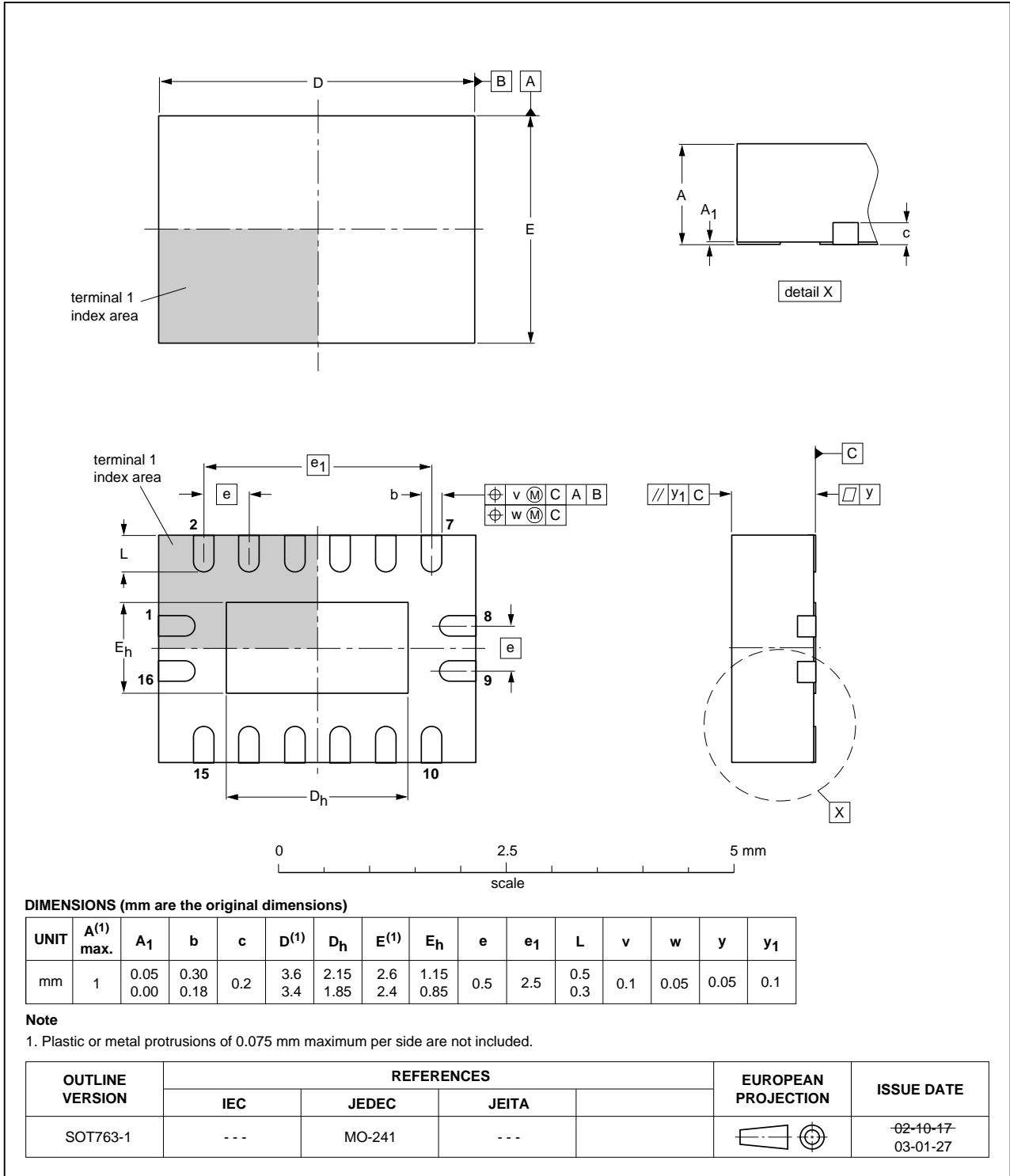


Fig 15. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4020 v.5	20120806	Product data sheet	-	74HC_HCT4020 v.4
Modifications:	• Measurement points added to figure 8 (errata).			
74HC_HCT4020 v.4	20111213	Product data sheet	-	74HC_HCT4020 v.3
Modifications:	• Legal pages updated.			
74HC_HCT4020 v.3	20100120	Product data sheet	-	74HC_HCT4020_CNV v.2
74HC_HCT4020_CNV v.2	19970901	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	1
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
7.1	Timing diagram	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	7
12	Waveforms	9
13	Package outline	12
14	Abbreviations	17
15	Revision history	17
16	Legal information	18
16.1	Data sheet status	18
16.2	Definitions	18
16.3	Disclaimers	18
16.4	Trademarks	19
17	Contact information	19
18	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 6 August 2012

Document identifier: 74HC_HCT4020