FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

May 2007

74VHC175
Quad D-Type Flip-Flop

Features

- High Speed: f_{MAX} = 210MHz (Typ.) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4μA (Max.) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.8V (Max.)
- Pin and function compatible with 74HC175

General Description

The VHC175 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

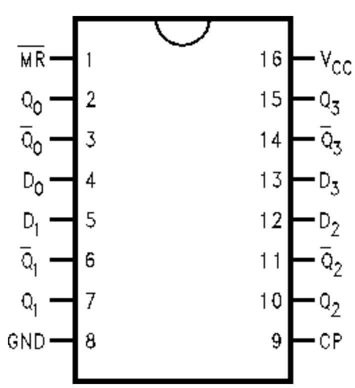
An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

Order Number	Package Number	Package Description
74VHC175M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

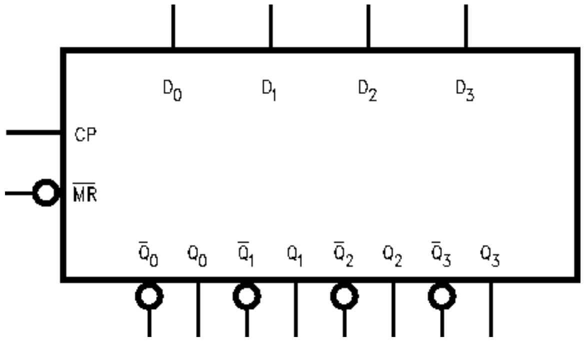
Connection Diagram



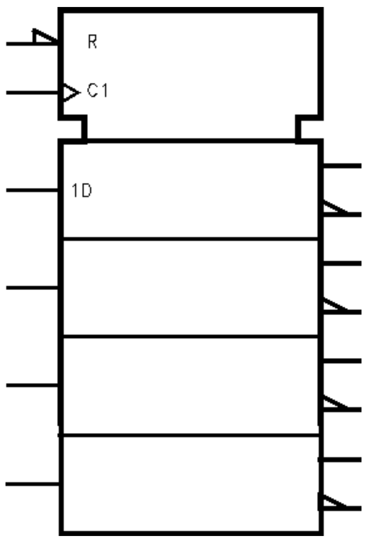
Pin Description

Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

Logic Symbol



IEEE/IEC



Functional Description

The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs @ t_n, $\overline{MR}$ = H	Outputs @ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

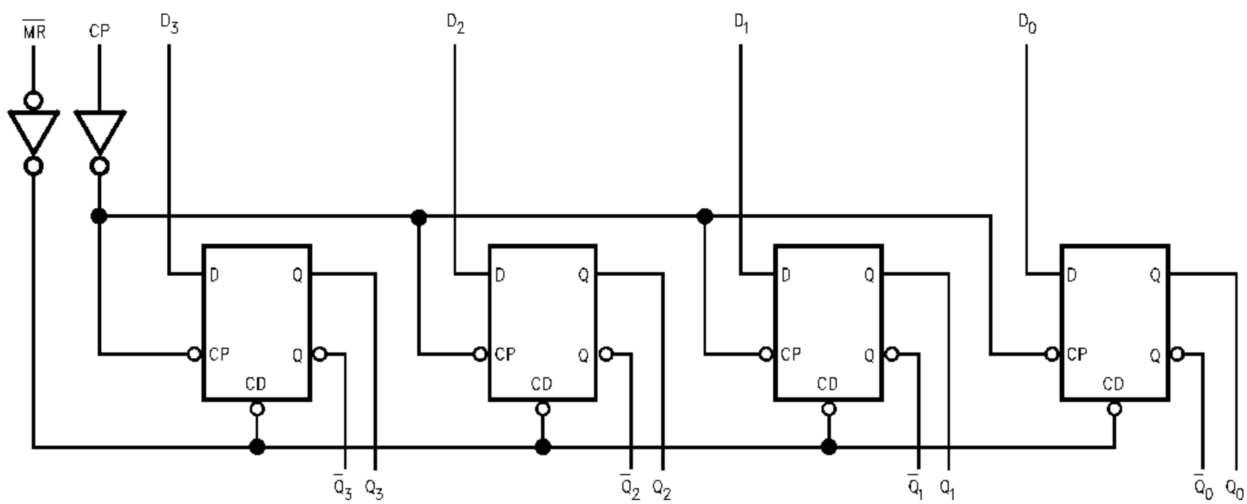
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit Time before Clock Pulse

t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time, V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	 0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		$T_A = 25°C$ Min.	Typ.	Max.	$T_A = -40°C$ to $+85°C$ Min.	Max.	Units
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = -4mA$	2.58			2.48		
		4.5		$I_{OH} = -8mA$	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		$I_{OL} = 4mA$			0.36		0.44	
		4.5		$I_{OL} = 8mA$			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	$V_{IN} = 5.5V$ or GND				±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND				4.0		40.0	µA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typ.	Limits	Units	Conditions
V_{OLP}(2)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	$C_L = 50pF$
V_{OLV}(2)	Quiet Output Minimum Dynamic V_{OL}	5.0	–0.4	–0.8	V	$C_L = 50pF$
V_{IHD}(2)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50pF$
V_{ILD}(2)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50pF$

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$			$T_A = –40°C$ to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	$C_L = 15pF$	90	140		75		MHz
			$C_L = 50pF$	50	75		45		
		5.0 ± 0.5	$C_L = 15pF$	150	210		125		MHz
			$C_L = 50pF$	85	115		75		
t_{PLH}, t_{PHL}	Propagation Delay Time, (CP to Q_n or $\overline{Q}_n$)	3.3 ± 0.3	$C_L = 15pF$		7.5	11.5	1.0	13.5	ns
			$C_L = 50pF$		10.0	15.0	1.0	17.0	
		5.0 ± 0.5	$C_L = 15pF$		4.8	7.3	1.0	8.5	ns
			$C_L = 50pF$		6.3	9.3	1.0	10.5	
t_{PLH}, t_{PHL}	Propagation Delay Time, ($\overline{MR}$ to Q_n or $\overline{Q}_n$)	3.3 ± 0.3	$C_L = 15pF$		6.3	10.1	1.0	12.0	ns
			$C_L = 50pF$		8.8	13.6	1.0	15.5	
		5.0 ± 0.5	$C_L = 15pF$		4.3	6.4	1.0	7.5	ns
			$C_L = 50pF$		5.8	8.4	1.0	9.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3	$C_L = 50pF$			1.5		1.5	
		5.0 ± 0.5	$C_L = 50pF$ [3]			1.0		1.0	
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		[4]		44				pF

Notes:

3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHmax} – t_{PLHmin}|$; $t_{OSHL} = | t_{PHLmax} – t_{PHLmin}|$.
4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per F/F), and the total C_{PD} when n pcs of the Flip-Flop operate can be calculated by the following equation: C_{PD} (total) = 30 + 14 • n

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)[5]	$T_A = 25°C$		$T_A = –40°C$ to +85°C	Units
			Typ.	Guaranteed Minimum		
$t_W(L)$, $t_W(H)$	Minimum Pulse Width (CP)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
$t_W(L)$	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time (Dn to CP)	3.3		5.0	5.0	ns
		5.0		4.0	4.0	
t_H	Minimum Hold Time (Dn to CP)	3.3		1.0	1.0	ns
		5.0		1.0	1.0	
t_{REC}	Minimum Removal Time ($\overline{MR}$)	3.3		5.0	5.0	ns
		5.0		5.0	5.0	

Note:

5. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

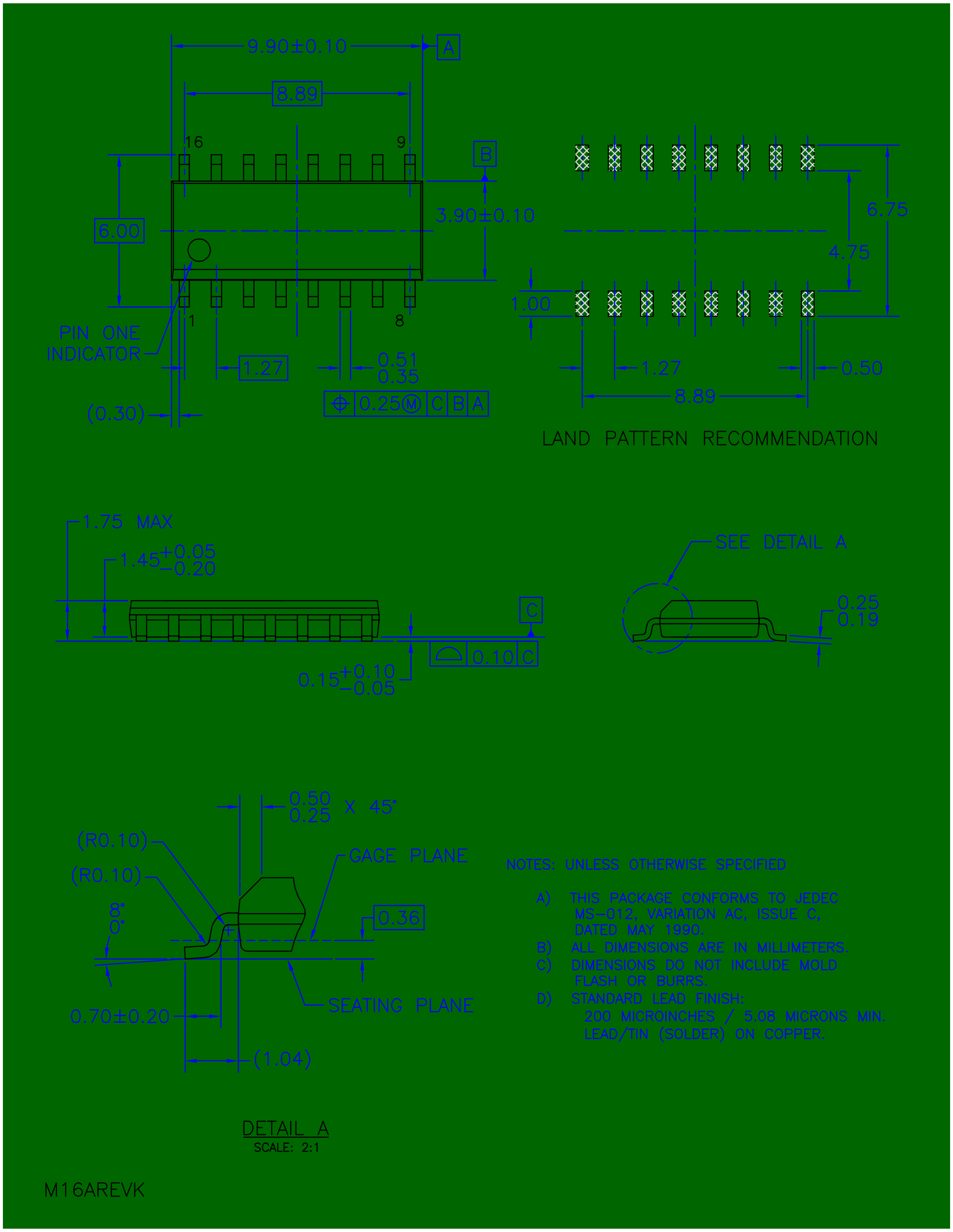


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

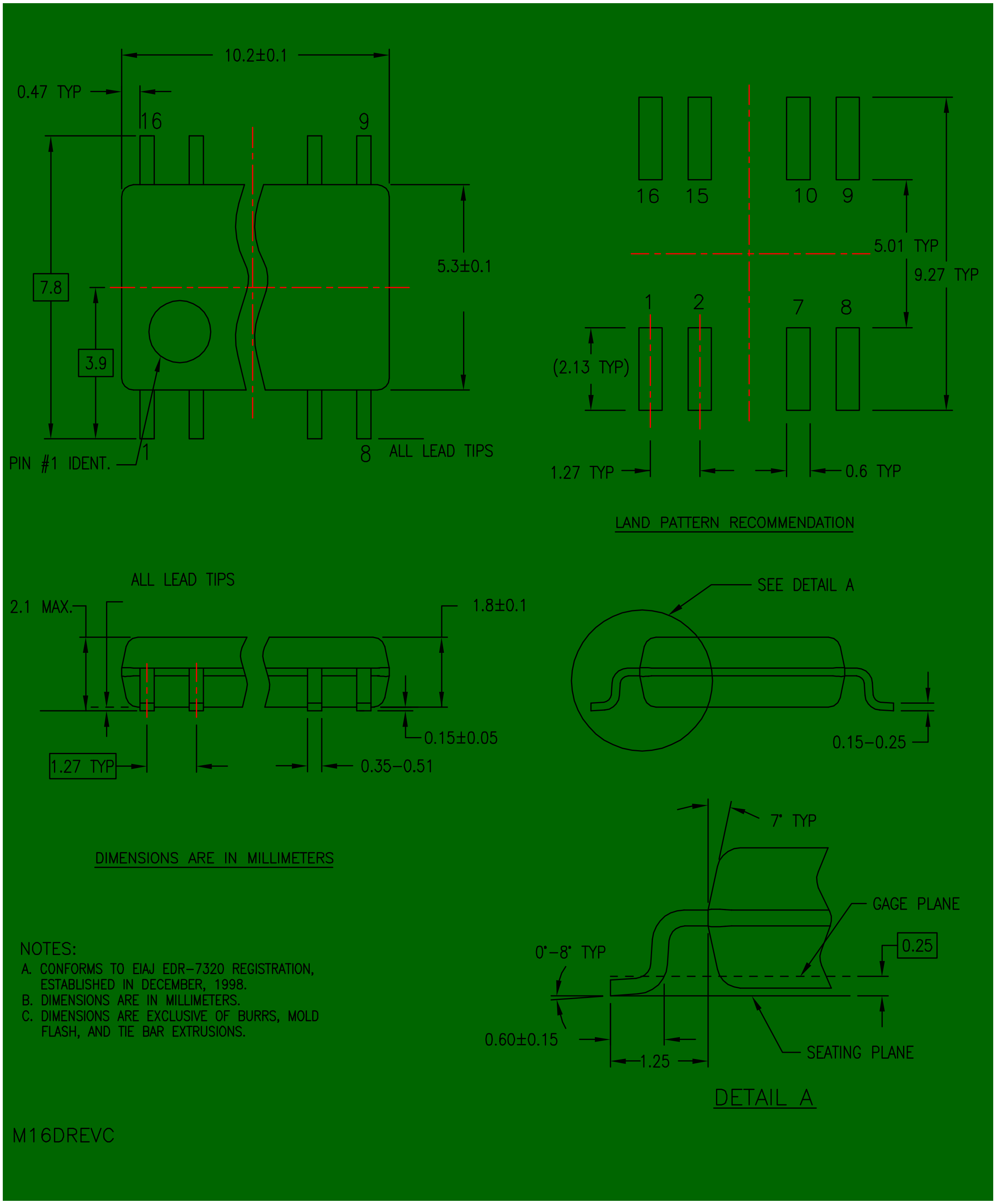


Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

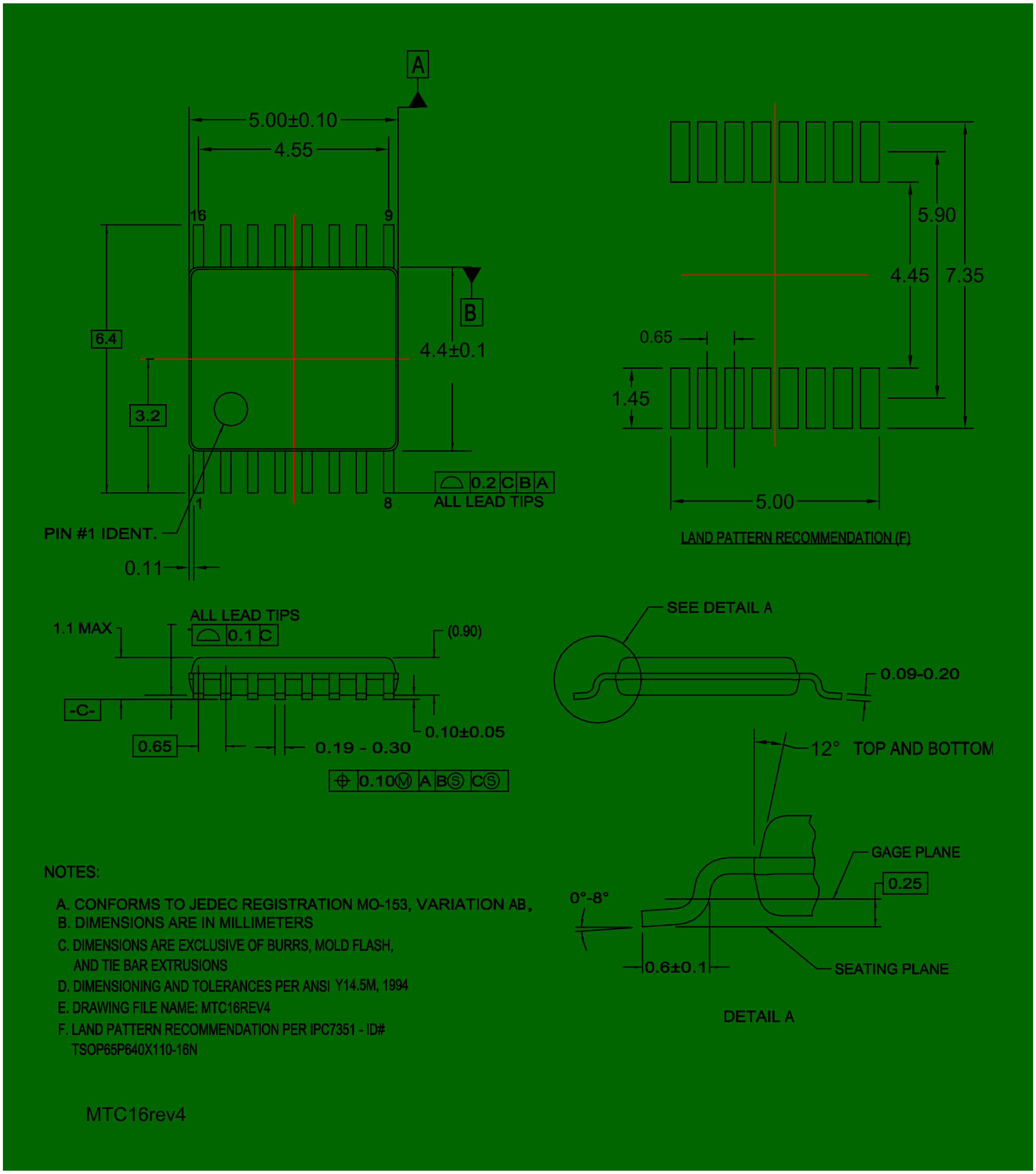


Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative