



Atmel | SMART ARM-based Flash MCU

SUMMARY DATASHEET

Description

The Atmel[®] | SMART SAM G54 is a series of Flash microcontrollers based on the high-performance 32-bit ARM[®] Cortex[®]-M4 RISC processor. They operate at a maximum speed of 96 MHz and feature up to 512 Kbytes of Flash and 96 Kbytes of SRAM. The peripheral set includes one USART, two UARTs, three I²C-bus interfaces (TWI), up to two SPIs, two three-channel general-purpose 16-bit timers, two I²S controllers with two-way, one-channel pulse density modulation, one real-time timer (RTT), one real-time clock (RTC) and one 8-channel 12-bit ADC.

The Atmel | SMART SAM G54 devices have two software-selectable low-power modes: Sleep and Wait. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. This feature, called SleepWalking, performs a partial asynchronous wake-up, thus allowing the processor to wake up only when needed.

The Event System allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

A general-purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set, the SAM G54 series sustains a wide range of applications including consumer, industrial control, and PC peripherals.

The device operates from 1.62V to 3.45V and is available in a 49-ball WLCSP package and a 100-pin LQFP package.

This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

Features

Core

- ARM Cortex-M4 up to 96 MHz
- Memory Protection Unit (MPU)
- DSP Instructions
- Floating Point Unit (FPU)
- Thumb[®]-2 instruction set

Memories

- 512 Kbytes embedded Flash
- 96 Kbytes embedded SRAM

System

- Embedded voltage regulator for single-supply operation
- Power-on reset (POR) and Watchdog for safe operation
- Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or device clock
- High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment
- Slow clock internal RC oscillator as permanent low-power mode device clock
- PLL range from 24 MHz to 96 MHz for device clock
- 28 peripheral DMA (PDC) channels
- 8 x 32-bit General-Purpose Backup Registers (GPBR)
- 16 external interrupt lines
- Power consumption in Active mode
 - 102 μA/MHz running Fibonacci in SRAM
- Low-power modes (typical value)
 - Wait mode down to 8 μA
 - Wake-up time less than 5 μs
 - Asynchronous partial wake-up (SleepWalking™) on UART and TWI

Peripherals

- One USART with SPI mode
- Two Inter-IC Sound Controllers (I²S)
- Two-way one-channel Pulse Density Modulation (PDM) (interfaces up to two microphones in PDM mode)
- Two UARTs
- Three Two-wire Interface (TWI) modules featuring two TWI masters and one high-speed TWI slave
- One fast SPI at up to 24 Mbit/s
- Two three-channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes
- One 32-bit Real-Time Timer (RTT)
- One 32-bit Real-Time Clock (RTC)



- I/O
 - Up to 38 I/O lines with external interrupt capability (edge or level), debouncing, glitch filtering and ondie series resistor termination. Individually programmable open-drain, pull-up and pull-down resistor and synchronous output
 - Two PIO Controllers provide control of up to 25 I/O lines
- Analog
 - One 8-channel ADC, resolution up to 12 bits, sampling rate up to 800 kSPS
- Package
 - 49-ball WLCSP
 - 100-pin LQFP, 14 x 14 mm, pitch 0.5 mm
- Temperature operating range
 - Industrial (-40° C to +85° C)



1. Configuration Summary

Table 1-1 summarizes the SAM G54 device configurations.

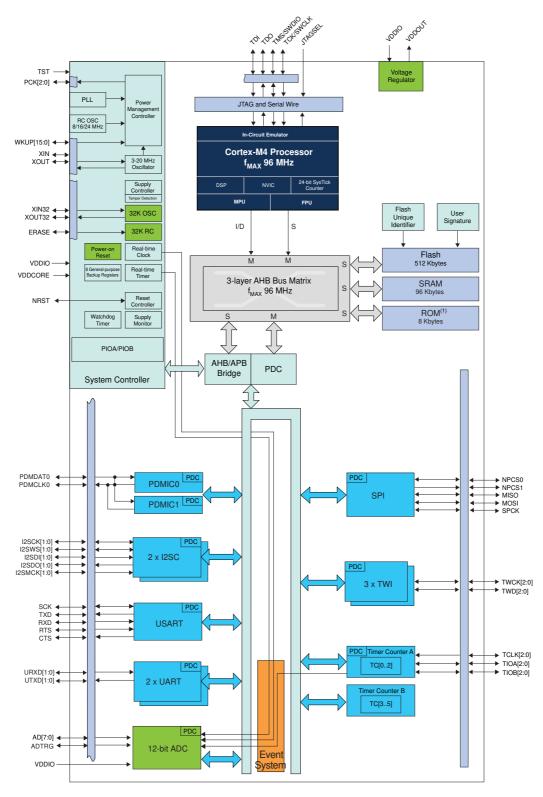
Table 1-1. Configuration Summary

Feature	SAM G54G19	SAM G54N19
Flash	512 Kbytes	512 Kbytes
SRAM	96 Kbytes	96 Kbytes
Package	WLCSP49	LQFP100
Number of PIOs	38	38
Event System	Yes	Yes
	8 channels	8 channels
	Performance:	Performance:
12-bit ADC	800 kSPS at 10-bit resolution	800 kSPS at 10-bit resolution
12-511 ADO	200 kSPS at 11-bit resolution	200 kSPS at 11-bit resolution
	50 kSPS at 12-bit resolution	50 kSPS at 12-bit resolution
	6 channels	6 channels
16-bit Timer	(3 external channels)	(3 external channels)
I2SC/PDM	2 / 1-channel 2-way	2 / 1-channel 2-way
PDC Channels	28	28
USART/UART	1/2	1/2
SPI	1	1
	2 masters at 400 Kbits/s and	2 masters at 400 Kbits/s and
TWI	1 slave at 3.4 Mbit/s	1 slave at 3.4 Mbit/s



2. Block Diagram

Figure 2-1. SAM G54 Block Diagram



Note: 1. The ROM is reserved for future use.



3. Signal Description

Table 3-1 provides details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Туре	Active Level	Voltage Reference	Comments
-	Power Su	pplies			
VDDIO	Peripheral I/O Lines, Voltage Regulator, ADC Power Supply	Power	_	_	1.62V to 3.45V
VDDOUT	Voltage Regulator Output	Power	_	_	_
VDDCORE	Core Chip Power Supply	Power	_	_	Connected externally to VDDOUT
GND	Ground	Ground	_	_	_
	Clocks, Oscillato	ors and PLLs			
XIN	Main Oscillator Input	Input	_	VDDIO	Reset state:
XOUT	Main Oscillator Output	Output	_	_	- PIO input
XIN32	Slow Clock Oscillator Input	Input	_	VDDIO	- Internal pull-up disabled
XOUT32	Slow Clock Oscillator Output	Output	_	_	- Schmitt Trigger enabled
PCK0-PCK2	Programmable Clock Output	Output	-	-	Reset state: - PIO input - Internal pull-up enabled - Schmitt Trigger enabled
	ICE and	JTAG			
TCK	Test Clock	Input	_	VDDIO	No pull-up resistor
TDI	Test Data In	Input	_	VDDIO	No pull-up resistor
TDO	Test Data Out	Output	_	VDDIO	_
TRACESWO	Trace Asynchronous Data Out	Output	_	VDDIO	_
SWDIO	Serial Wire Input/Output	I/O	_	VDDIO	_
SWCLK	Serial Wire Clock	Input	_	VDDIO	_
TMS	Test Mode Select	Input	_	VDDIO	No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDIO	Pull-down resistor
	Flash Me	emory			
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down (15 kΩ) resistor
	Reset/	Test			
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
TST	Test Mode Select	Input	_	VDDIO	Pull-down resistor
	Universal Ansynchronous Receiv	er Transceive	er - UART[x	=01]	
URXDx	UART Receive Data x	Input	_	_	_

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Туре	Active Level	Voltage Reference	Comments
UTXDx	UART Transmit Data x	Output	_	_	_
	PIO Controll	er - PIOA - PIOB			
PA0-PA24	Parallel I/O Controller A I/O – VDDIO re		Pulled-up input at reset. No pull-down for PA3/PA4/PA14.		
PB0-PB12	Parallel I/O Controller B	I/O	_	VDDIO	Pulled-up input at reset
	Wake	-up Pins			
WKUP0-15	Wake-up Pin / External Interrupt	I/O	-	VDDIO	Wake-up pins are used also as External Interrupt
	Universal Synchronous Asynchr	onous Receiver	Transmitter	USART	
SCK	USART Serial Clock	I/O	_	_	_
TXD	USART Transmit Data	I/O	_	_	_
RXD	USART Receive Data	Input	_	_	_
RTS	USART Request To Send	Output	_	_	_
CTS	USART Clear To Send	Input	_	_	_
	Timer/Coun	ter - TC[x=03]		•	
TCLKx	TC Channel x External Clock Input	Input	_	_	_
TIOAx	TC Channel x I/O Line A	I/O	_	_	_
TIOBx	TC Channel x I/O Line B	I/O	_	_	_
	Serial Periphe	ral Interface - SP	1	•	
MISO	Master In Slave Out	I/O	_	_	_
MOSI	Master Out Slave In	I/O	_	_	_
SPCK	SPI Serial Clock	I/O	_	_	High-speed pad
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	_	_
NPCS1	SPI Peripheral Chip Select 1	Output	Low	_	_
	Two-Wire Inte	rface- TWI[x=01]		
TWDx	TWIx Two-wire Serial Data	I/O	_	_	High-speed pad for TWD0
TWCKx	TWIx Two-wire Serial Clock	I/O	_	_	High-speed pad for TWDCK0
	10-bit Analog-to-Di	gital Converter -	ADCC		
AD0-AD7	Analog Inputs	Analog	_	_	_
ADTRG	ADC Trigger	Input	_		
	Inter-IC Sound Co	ntroller - I2SC[x=	:01]		
I2SMCKx	Master Clock	Output	_	-	_
I2SCKx	Serial Clock	I/O	_	_	_
I2SWSx	I ² S Word Select	I/O	_	_	_



Table 3-1. Signal Description List (Continued)

Signal Name	Function	Туре	Active Level	Voltage Reference	Comments
I2SDIx	Serial Data Input	Input	_	_	_
I2SDOx	Serial Data Output	Output	_	-	_
PDMCLK0	Pulse Density Modulation Clock	Output	_	_	_
PDMDAT0	Pulse Density Modulation Data	Input	_	ı	_

4. Package and Pinout

Table 4-1. SAM G54 Packages

Device	Package
SAM G54G19	WLCSP49
SAM G54N19	LQFP100

4.1 49-ball WLCSP Pinout

Table 4-2. SAM G54G19 49-ball WLCSP Pinout

A1	PA9
A2	GND
A3	PA24
A4	PB8/XOUT
A5	PB9/XIN
A6	PB4
A7	VDDIO
B1	PB11
B2	PB5
В3	PB7
B4	PA2
B5	JTAGSEL
В6	NRST
B7	PB12

C1	VDDCORE
C2	PA11
C3	PA12
C4	PB6
C5	PA4
C6	PA3
C7	PA0
D1	PA13
D2	PB3/AD7
D3	PB1/AD5
D4	PB10
D5	PA1
D6	PA5
D7	VDDCORE

E1	PB2/AD6
E2	PB0/AD4
E3	PA18/AD1
E4	PA14
E5	PA10
E6	TST
E7	PA7/XIN32
F1	PA20/AD3
F2	PA19/AD2
F3	PA17/AD0
F4	PA21
F5	PA23
F6	PA16
F7	PA8/XOUT32

G1	VDDIO
G2	VDDOUT
G3	GND
G4	VDDIO
G5	PA22
G6	PA15
G7	PA6



4.2 100-lead LQFP Pinout

Table 4-3. SAM G54N19 100-pin LQFP Pinout

1	NC
2	NC
3	NC
4	NC
5	VDDIO
6	VDDIO
7	NRST
8	PB12
9	PA4
10	PA3
11	PA0
12	PA1
13	PA5
14	VDDIO
15	VDDCORE
16	VDDCORE
17	TEST
18	PA7
19	PA8
20	GND
21	NC
22	NC
23	NC
24	NC
25	NC

pin EG	i i i iiiout
26	NC
27	NC
28	PA6
29	VDDIO
30	PA16
31	PA15
32	PA23
33	NC
34	NC
35	PA22
36	PA21
37	VDDIO
38	VDDIO
39	GND
40	GND
41	GND
42	GND
43	GND
44	VDDOUT
45	VDDOUT
46	VDDIO
47	VDDIO
48	VDDIO
49	NC
50	NC

51	NC
52	NC
53	PA17
54	PA18
55	PA19
56	PA20
57	PB0
58	PB1
59	PB2
60	PB3
61	VDDIO
62	PA14
63	PA13
64	PA12
65	PA11
66	VDDCORE
67	VDDCORE
68	PB10
69	PB11
70	GND
71	GND
72	PA10
73	NC
74	NC
75	NC

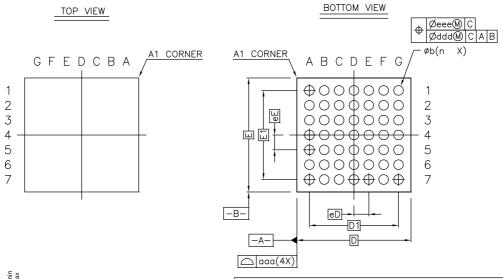
76	NC
77	NC
78	NC
79	PA9
80	PB5
81	GND
82	GND
83	GND
84	PB6
85	PB7
86	PA24
87	PB8
88	PB9
89	VDDIO
90	PA2
91	PB4
92	NC
93	JTAGSEL
94	VDDIO
95	VDDIO
96	NC
97	NC
98	NC
99	NC
100	NC

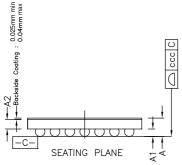


5. Mechanical Characteristics

5.1 49-lead WLCSP Package

Figure 5-1. 49-lead WLCSP Package Mechanical Drawing



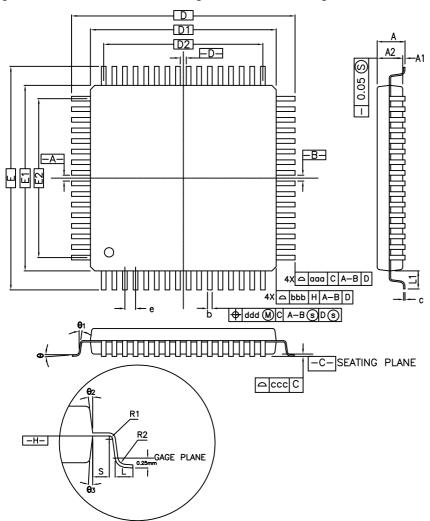


	SYMBOL	COMMON DIMENSIONS		
	SIMBUL	MIN.	NOM.	MAX.
Total Thickness	Α	0.440	0.494	0.533
Stand Off	A1	0.17	_	0.23
Wafer Thickness	A2	0.2	254 ±	0.025
Body Size	D		3.072	BSC
Body Size	E		3.072	BSC
Ball Diameter (Size)			0.25	
Ball/Bump Width	b	0.23	0.26	0.29
D-II /D Ditab	eD		0.4	
Ball/Bump Pitch	еE		0.4	
Ball/Bump Count	n	49		
Edna Ball Cantas to Cantas	D1		2.4	BSC
Edge Ball Center to Center	E1		2.4	BSC
Package Edge Tolerance	aaa		0.03	
Coplanarity (whole wafer)	ссс		0.075	
Ball/Bump Offset (Package)	ddd		0.05	
Ball/Bump Offset (Ball)	eee		0.015	



5.2 100-lead LQFP Package

Figure 5-2. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
SIMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α			1.60	_		0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.	551 BS	SC.
Ε	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08		0.20	0.003		0.008
R ₁	80.0			0.003	1	
Φ	0,	3.5*	7*	0,	3.5*	7*
θ1	ò			0.		
θг	11*	12 °	13°	11°	12*	13°
θз	11*	12*	13°	11*	12*	13°
O	0.09		0.20	0.004		0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 REF			0.039 REF		
S	0.20	_		0.008	_	_

	100L					
SYMBOL	MI	MILLIMETER		INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
е	0.50 BSC.			0.0	020 B	SC.
D2	12.00		0.472			
E2	12.00			0.472		
aaa	0.20		(800.0		
bbb	0.20			800.0		
CCC	0.08		0.08 0.003			
ddd	0.08		0.08 0.003			

6. Ordering Information

Table 6-1. SAM G54 Ordering Codes

Ordering Code	MRL	Flash (Kbytes)	Package	Carrier Type	Temperature Operating Range
ATSAMG54G19B-UUT	В	512	WLCSP49	Tape and Reel	Industrial -40°C to 85°C
ATSAMG54N19B-AU	В	512	LQFP100	Tape and Reel	Industrial -40°C to 85°C



7. Revision History

In the tables that follow, the most recent version of the document appears first.

Table 7-1. SAM G54 Datasheet Rev. 11266AS Revision History

Doc. Date	Changes
16-Dec-14	First issue.















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