

# **BOOSTXL-TPS65218 EVM User's Guide**

The BOOSTXL-TPS65218 is a BoosterPack evaluation module (EVM) for programming samples of the TPS65218D0 power management IC (PMIC) with user-defined values for output voltage, sequence timing, and other critical parameters. Modifying these parameters using the BOOSTXL-TPS65218 allows for rapid prototyping and quick time to market when using the TPS65218D0 PMIC to provide power to a variety of processors and FPGAs.

This document provides a description of how to setup the EVM and re-program the EEPROM memory of the TPS65218D0 devices using the BOOSTXL-TPS65218 BoosterPack, an MSP430F5529 LaunchPad, and the IPG-UI software. The steps in this document describe the procedure for programming samples of the TPS65218D0 installed in the socket of the BOOSTXL-TPS65218 printed circuit board (PCB).

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## Trademarks

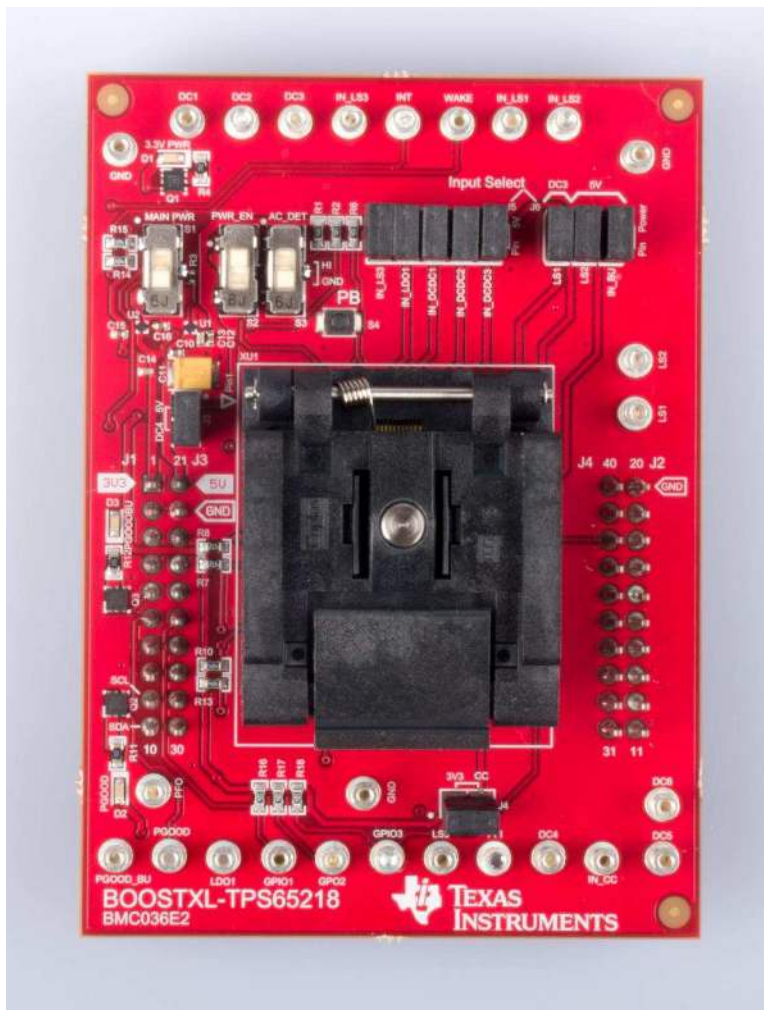
### 1 Introduction

The BOOSTXL-TPS65218 allows designers to program samples of the TPS65218D0 and verify the values in the EEPROM match the power-up and power-down sequence requirements of the targeted processor that will be powered by the PMIC in the final application. The BOOSTXL-TPS65218 BoosterPack EVM is simple to test, requiring only an MSP430F5529 LaunchPad and USB A-to-micro B cable. With no load or a light load on the BoosterPack EVM, the power provided by the LaunchPad is sufficient to power the TPS65218D0 device, re-program the EEPROM, and perform all of the measurements described in this document. The 5 V provided by the VBUS wire of the USB cable is the only power input to the LaunchPad.

The TPS65218D0 device consists of three step-down converters (DCDC1, DCDC2, DCDC3), one buck-boost converter (DCDC4), two low-quiescent current step-down converters (DCDC5, DCDC6), a general-purpose LDO regulator (LDO1), and three load switches (LS1, LS2, LS3) with varying input voltage ranges. The output voltage of all the DC/DC converters and the LDO regulator is programmable. The current limit of the load switches is programmable. The sequence order of all DC/DC converters, the LDO, and the load switches can also be programmed and assigned to integer values relative to each other. The sequence timing and supervisor tolerances are global parameters that can be programmed.

Modifying some or all of these register map values and re-programming the EEPROM of the TPS65218D0 device with the IPG-UI software creates new reset values for the PMIC, which allows the PMIC to power-on and power-off with the required timing for a variety of processors or FPGAs.

**Figure 1** shows the top-side of the BOOSTXL-TPS65218 PCB, on which a socket is placed to install TPS65218D0 samples and re-program the samples. The samples can then be removed from the socket and soldered down on a TPS65218EVM-100 or prototype PCB to evaluate the power delivery capabilities of the TPS65218D0 newly programmed for a specific processor or FPGA. If the output voltages or sequencing are not ideal for the processor or FPGA on the first attempt, the process can be repeated until the ideal programming of the TPS65218D0 device is determined.



**Figure 1. BOOSTXL-TPS65218 Printed Circuit Board (Top View)**

This procedure requires:

1. An MSP430F5529 LaunchPad development kit, [MSP-EXP430F5529LP](#)
2. A USB A to micro B cable (included with the LaunchPad development kit)
3. A BOOSTXL-TPS65218 BoosterPack plug-in module
4. TPS65218D0 devices (TPS65218D0RSL)
5. An internet connection

Specific instructions on how to program the TPS65218D0 using the BOOSTXL-TPS65218 with the IPG-UI software are provided in [Appendix A](#), while the EVM documentation related to the design of the BOOSTXL-TPS65218 hardware is provided in [Appendix B](#).

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**NOTE:** All re-programmed EEPROM settings must be validated during prototyping phase to ensure desired functionality because parts cannot be returned in case of incorrect programming. Any issues should be reported to the [e2e forum](#).

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## 1.1 Related Documentation

Texas Instruments,

[Integrated Power Management \(PMIC\) for ARM® Cortex™-A8/A9 SOCs and FPGAs data sheet](#)  
 Texas Instruments, [IPG-UI User's Guide](#)

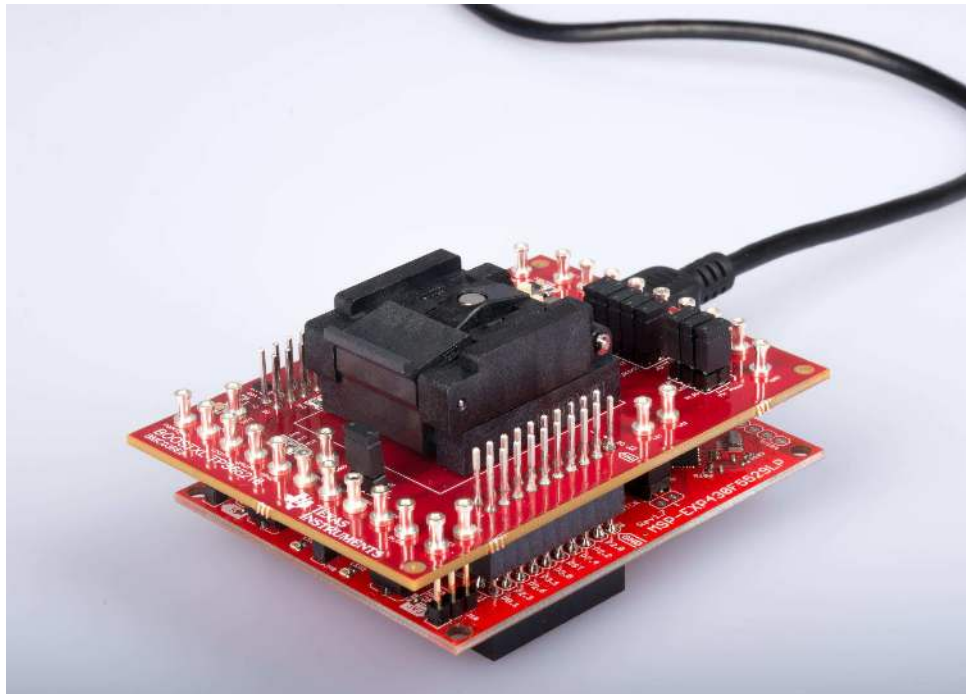
Texas Instruments, [TPS65218EVM User's Guide](#)

Texas Instruments, [MSP430F5529 LaunchPad Development Kit \(MSP-EXP430F5529LP\) User's Guide](#)

## 1.2 Required Hardware

### 1.2.1 MSP430F5529 LaunchPad

The MSP430F5529 LaunchPad will serve as a communication interface between the IPG-UI software and the TPS65218D0 device. The firmware on the MSP430F5529 needs to be updated before it can communicate with the TPS65218D0. [Figure 2](#) shows the BOOSTXL-TP65218 connected on top of the MSP430F5529 LaunchPad with a micro-USB cable inserted in the LaunchPad.



**Figure 2. BOOSTXL-TPS65218 and MSP430F5529 LaunchPad Connected**

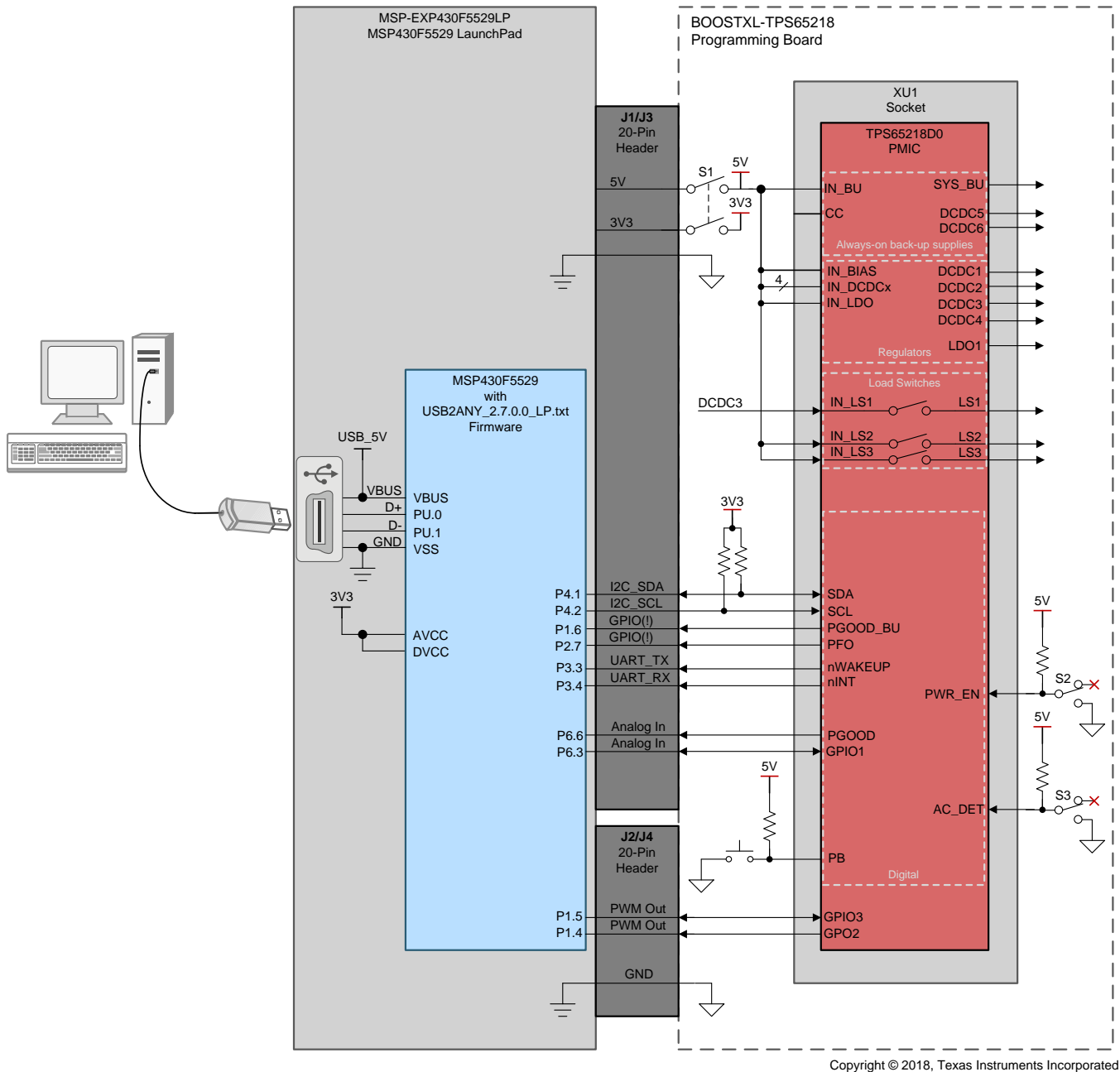
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**NOTE:** Do not plug the BOOSTXL-TPS65218 BoosterPack into the MSP430F5529 LaunchPad before the firmware is updated, as described in [Section 2.5](#).

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## 2 Getting Started

[Figure 3](#) shows the high-level block diagram of the BOOSTXL-TPS65218 as it is wired to the MSP430F5529 LaunchPad through the two 20-pin headers connecting the two PCBs. It also shows the LaunchPad connected to a computer through a USB cable, which is required for programming the TPS65218D0 device.



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Figure 3. BOOSTXL-TPS65218 BoosterPack and MSP430F5529 LaunchPad Block Diagram

## 2.1 Connecting Headers

This section describes the headers on the BOOSTXL-TPS65218 used to connect the BoosterPack EVM to the MSP430F5529 LaunchPad. There are two sets of headers numbered J1-J4, each set having two rows of 10 pins, for a total of 40 pins. The outside headers, closest to the board edge, are J1 (left) and J2 (right). The inside headers, closest to the socket on BOOSTXL-TPS65218 and closest to the MSP430F5529 device on the LaunchPad, are J3 (left) and J4 (right). When connected correctly, all 40 pins of the headers make a physical connection from board to board and the headers numbers line up (in other words, J1 connects to J1, J2 connects to J2, and so forth.). However, all 40 pins do not make an electrical connection from the LaunchPad to the BOOSTXL-TPS65218 design.

Table 1 lists all of the electrical connections made when the headers of the BOOSTXL-TPS65218 and MSP430F5529 LaunchPad are connected correctly.

**Table 1. Electrical Connections of Headers**

BOOSTXL-TPS65218		Connecting Headers			MSP430F5529 LaunchPad	
Device Pin	Net Name	Pin Number	Header Number	Pin Number	Header Pin Info	Net and/or Device Pin Name
I/O Power <sup>(1)</sup>	3V3LP	1	J1	1	+3V3	+3V3
45	nINT <sup>(2)</sup>	3	J1	3	UART RX	P3.4
40	nWAKEUP <sup>(2)</sup>	4	J1	4	UART TX	P3.3
19	PGOOD_BU <sup>(2)</sup>	5	J1	5	GPIO(!)	P1.6
8	PGOOD <sup>(2)</sup>	6	J1	6	Analog In	P6.6
10	nPFO <sup>(2)</sup>	8	J1	8	GPIO(!)	P2.7
3	SCL	9	J1	9	I2C SCL	P4.2
2	SDA	10	J1	10	I2C SDA	P4.1
PAD	GND	20	J2	20	GND	GND
Input Power <sup>(3)</sup>	5VLP	21	J3	21	+5V	+5V
PAD	GND	22	J3	22	GND	GND
11	GPIO1 <sup>(2)</sup>	26	J3	26	Analog In	P6.3
26	GPIO3 <sup>(2)</sup>	38	J4	38	PWM Out	P1.5
34	GPO2 <sup>(2)</sup>	37	J4	37	PWM Out	P1.4

<sup>(1)</sup> The net named 3V3LP is re-named 3V3 after the current-limiting switch controlled by S1 and provides a pull-up reference voltage for SCL, SDA, PGOOD, nPFO, nINT, nWAKEUP, GPIO1, GPO2, and GPIO3 pins of the TPS65218D0 device. It is also an optional power supply for the CC (coin cell) pin.

<sup>(2)</sup> Resistors R19-R26 on the BOOSTXL-TPS65218 board are not installed. As a result, this pin will not be electrically connected to the MSP430F5529 unless a 0-Ω resistor is added manually.

<sup>(3)</sup> The net named 5VLP is re-named 5V after the current-limiting switch controlled by S1 and provides power to IN\_BIAS directly. 5V also provides power to all IN\_DCDCx pins, IN\_LDO1, IN\_LS2, IN\_LS3, and IN\_BU when shunts are installed on headers J5 and J6. It is also the voltage compared at PFI and the pull-up reference voltage for PWR\_EN and AC\_DET.

## 2.2 Test Points

Table 2 lists the test points located on the BOOSTXL-TPS65218. The test points are required to measure the output voltage and sequence timing of the power rails generated by the TPS65218D0 device.

**Table 2. BOOSTXL-TPS65218 Test Point List**

PCB Reference Designator	Net Name	Type
TP1	PFI	Comparator input
TP2, TP3, TP4	PGND, AGND, thermal pad	Ground
TP5	LS1	Power output
TP6	LDO1	Power output
TP7	IN_LS1	Power input
TP8	LS2	Power output
TP9	LS3	Power output
TP10	PGOOD	Data output
TP11	PGOOD_BU	Data output
TP12	IN_LS2	Power input
TP13	IN_LS3	Power input
TP14	IN_nCC	Ground
TP15	nPFO	Data output
TP16	nINT	Data output
TP17	nWAKEUP	Data output

**Table 2. BOOSTXL-TPS65218 Test Point List (continued)**

PCB Reference Designator	Net Name	Type
TP18	GPIO1	Data input/output
TP19	GPO2	Data output
TP20	GPIO3	Data input/output
TP21	DC5	Power output
TP22	DC1	Power output
TP23	DC4	Power output
TP24	DC2	Power output
TP25	DC6	Power output
TP26	DC3	Power output

### 2.3 Jumpers

Table 3 lists and describes the jumper headers located on the BOOSTXL-TPS65218 for connecting or disconnecting nets of the PCB.

**Table 3. BOOSTXL-TPS65218 Jumper List**

PCB Reference Designator	Pin	Net Name	Default Shunt Connection <sup>(1)</sup>	Description
J3	1	5V	Installed	Required for 5V from LaunchPad to power DCDC4
	2	IN_DCDC4		
J4	1	3V3	Installed	Required for 3V3 from LaunchPad to power CC
	2	CC		
J5	1	5V	Installed	Required for 5V from LaunchPad to power DCDC3
	2	IN_DCDC3		
	3	5V	Installed	Required for 5V from LaunchPad to power DCDC2
	4	IN_DCDC2		
	5	5V	Installed	Required for 5V from LaunchPad to power DCDC1
	6	IN_DCDC1		
	7	5V	Installed	Required for 5V from LaunchPad to power LDO1
	8	IN_LDO1		
	9	5V	Installed	Required for 5V from LaunchPad to power LS3
	10	IN_LS3		
J6	1	5V	Installed	Required for 5V from LaunchPad to power IN_BU
	2	IN_BU		
	3	5V	Installed	Required for 5V from LaunchPad to power LS2
	4	IN_LS2		
	5	DC3	Installed	Required for DCDC3 to power LS1
	6	IN_LS1		

<sup>(1)</sup> Removing any of the shunts that are installed by default is an optional way to supply power to a DC/DC converter, the LDO regulator, or a load switch from an external supply.

### 2.4 Software

The software to be used with the BOOSTXL-TPS65218 EVM is the IPG-UI. Download the following files to ensure that all of the required software is available on the computer used for testing:

1. The latest revision of the [IPG-UI EVM GUI](#).
2. The latest revision of the TPS65218 IPG-UI device file (TPS65218-1.x.json) and script file (TPS65218-1.x.js) from [here](#).
3. The latest MSP430F5529 LaunchPad USB2ANY firmware (USB2ANY\_2.7.0.0\_LP.txt) from [here](#).

4. The MSP430\_USB\_Firmware\_Upgrade\_Example-1.3.1.1-Setup.exe from the [MSP430\\_USB\\_Developers\\_Package 5\\_20\\_06\\_02](#).

A detailed set of instructions for using the software, with examples, is provided in [Appendix A](#).

## 2.5 Update MSP430F5529 Firmware

Update the MSP430F5529 LaunchPad development to the USB2ANY\_2.7.0.0\_LP.txt file before putting the BOOSTXL-TPS650861 on the LaunchPad development kit.

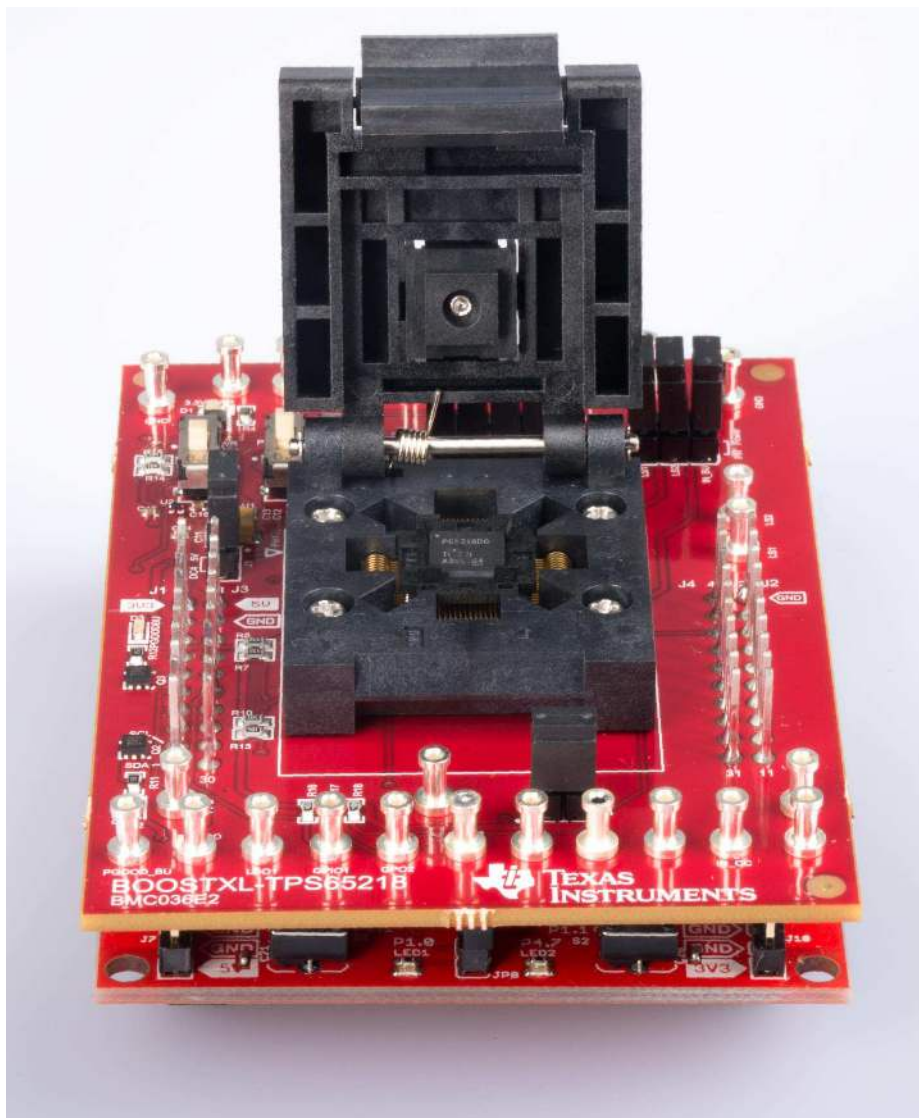
1. Press the S5 button while connecting the Micro USB cable.
2. Run the Firmware Upgrade Example.
3. Choose "Select Firmware".
4. Choose "Browse" and select the USB2ANY\_2.7.0.0\_LP.txt file downloaded previously.
5. Choose "Upgrade Firmware".
6. When complete, disconnect the USB cable.

## 3 EVM Operation

### 3.1 Power-On Procedure

[Figure 4](#) shows the BOOSTXL-TPS65218 board with socket XU1 open and a TPS65218D0 samples installed correctly. After the socket is closed, the S1 MAIN PWR switch can be moved from the GND (off) position to the HI (on) position.





**Figure 4. BOOSTXL-TPS65218 with Socket Open**

In order for all of the DCDCx converters, LDO1 regulator, LSx load switches, CC pin, and IN\_BU pin of the TPS65218D0 to receive power from the USB cable through the LaunchPad, shunts must be installed on all 2-pin headers as described in [Table 3](#).

## Software Instructions

### A.1 IPG-UI Software Installation

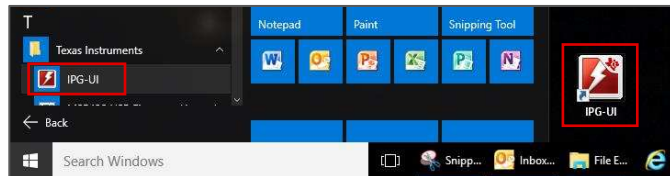
The following instructions explain how to install the IPG-UI software on a computer. If this software is already installed, this section may be skipped.

To install the IPG-UI software, first download the [IPG-UI](#) software installation package from [www.ti.com](http://www.ti.com). Then unzip and install the IPG-UI software tool onto the computer.

### A.2 IPG-UI Setup for BOOSTXL-TPS65218

The following instructions explain how to run, setup, and operate the IPG-UI software on a computer and connect it to the BOOSTXL-TPS65218.

- Install a shunt on header J20, shorting pin 1 (USB\_3P3V) and pin 2 (MSP\_3P3V).
- Run the IPG-UI software by using the Windows *Start Menu* and navigating to the Texas Instruments folder, or by double-clicking the desktop icon, as shown in [Figure 5](#).



**Figure 5. Run the IPG-UI Software**

- Wait for the program to load.
- Plug in the micro-USB cable to J21 and connect the other end of the USB cable to an open USB2/3 port on the computer.
- Verify that the software is connected to the USB2ANY as shown in [Figure 6](#).



**Figure 6. Successful Connection Between Computer and USB2ANY**

- Click the drop-down menu in the *Create New Project* section and select *TPS65218D0-spi-1.x* as shown in [Figure 7](#).

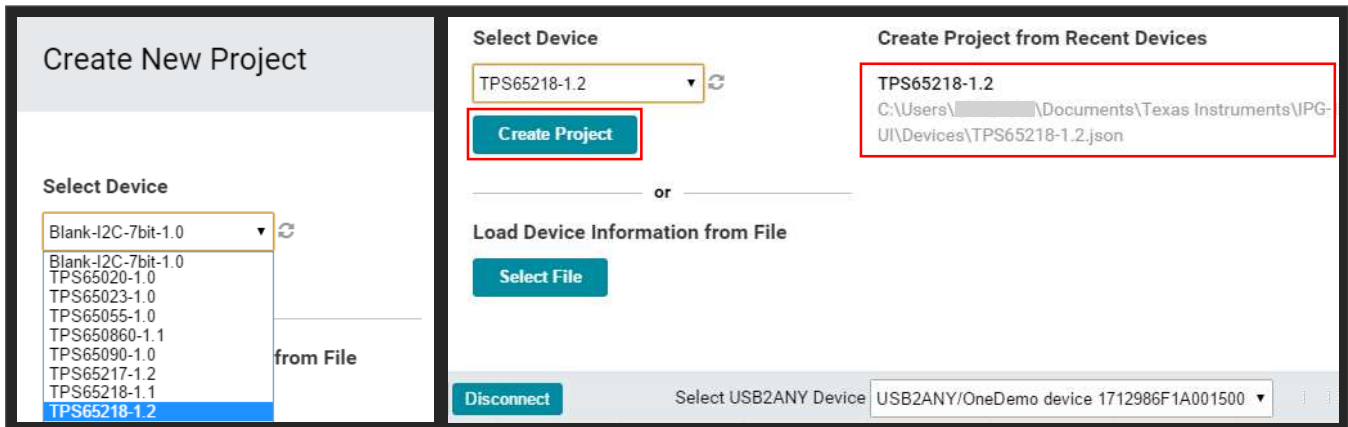


Figure 7. Creating New IPG-UI Project for the TPS65218D0

- Click the *Create Project* button.

**NOTE:** After a project is initially created, it is available in the *Create Projects from Recent Devices* menu. When a project is saved, it is available in the *Open Recent Projects* menu.

- The TPS65218 *Introduction* tab is now displayed, as shown in Figure 8. Click the *Get Started* button or the *Register Map* tab to begin communicating with TPS65218D0 device.

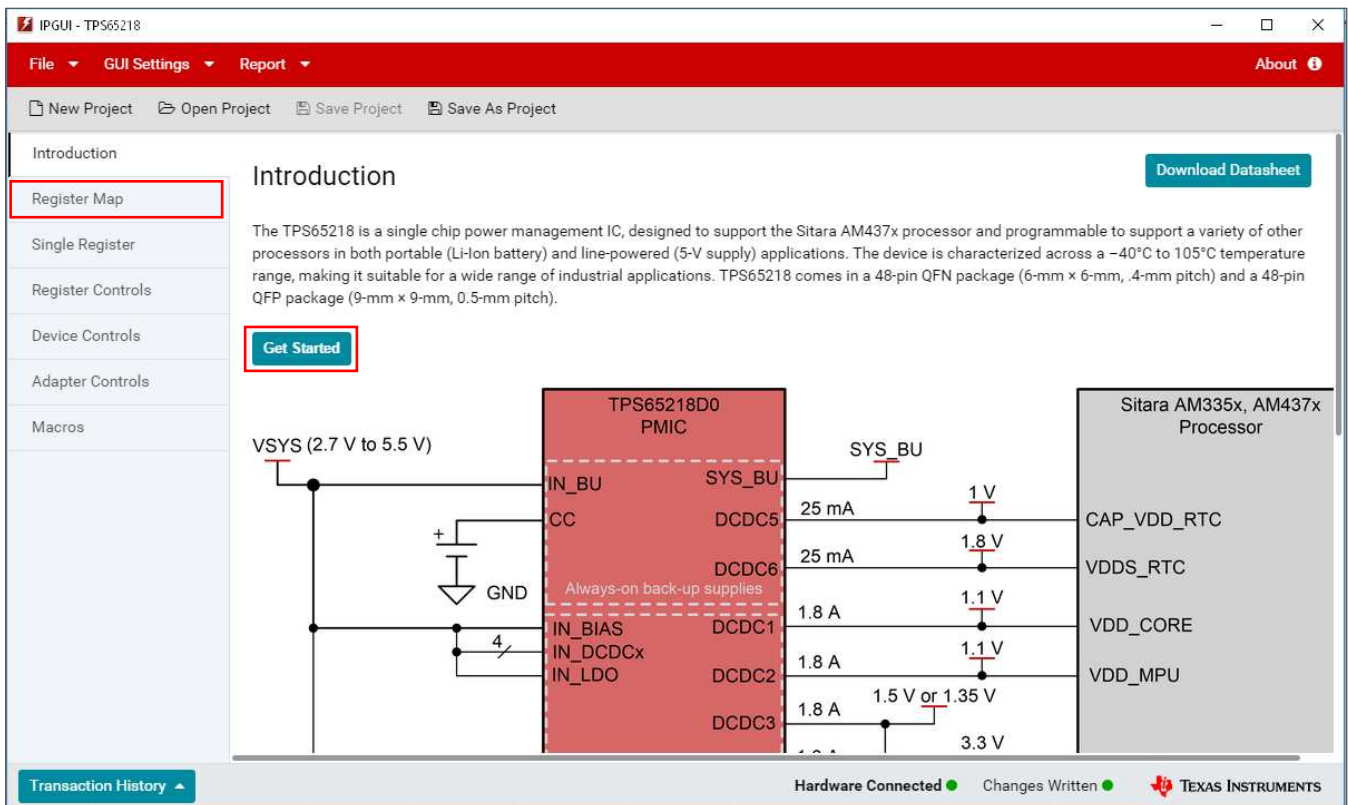
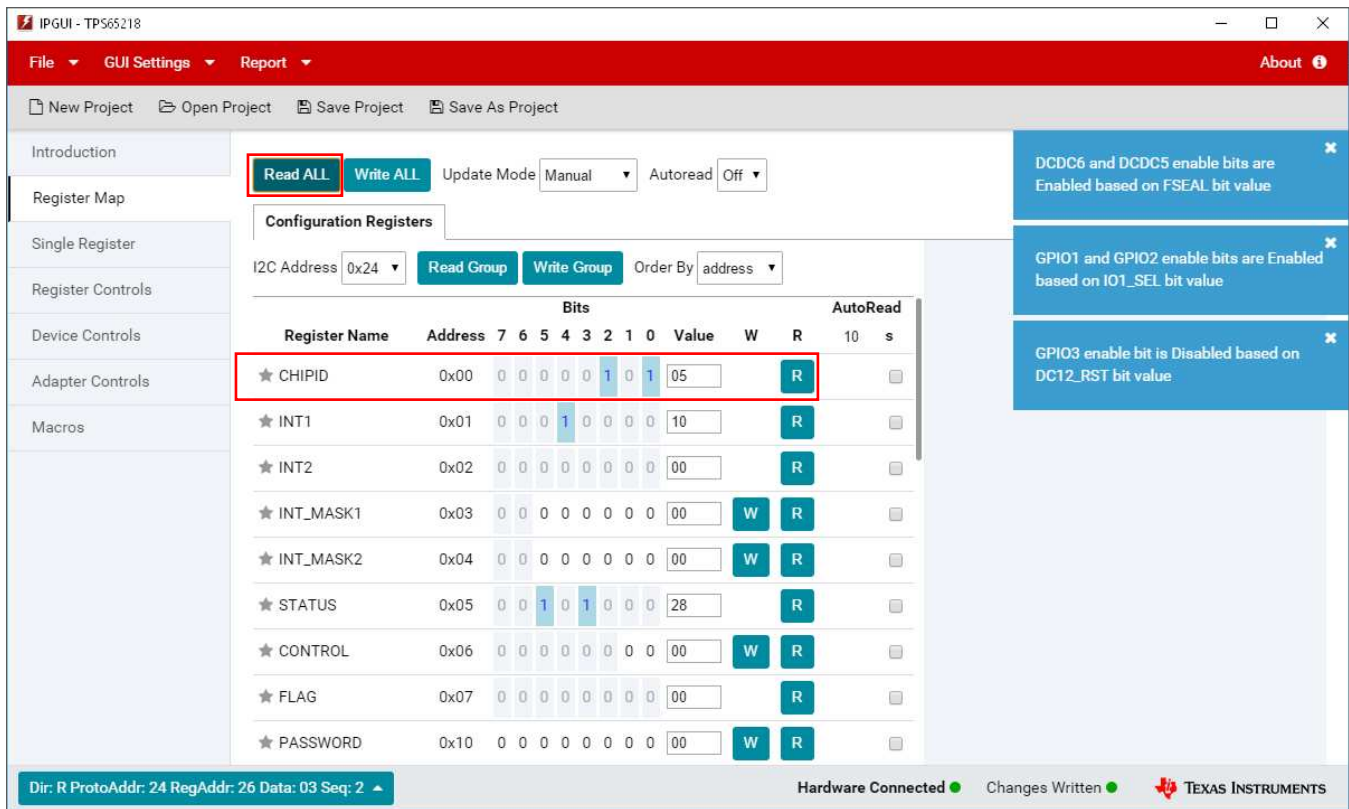


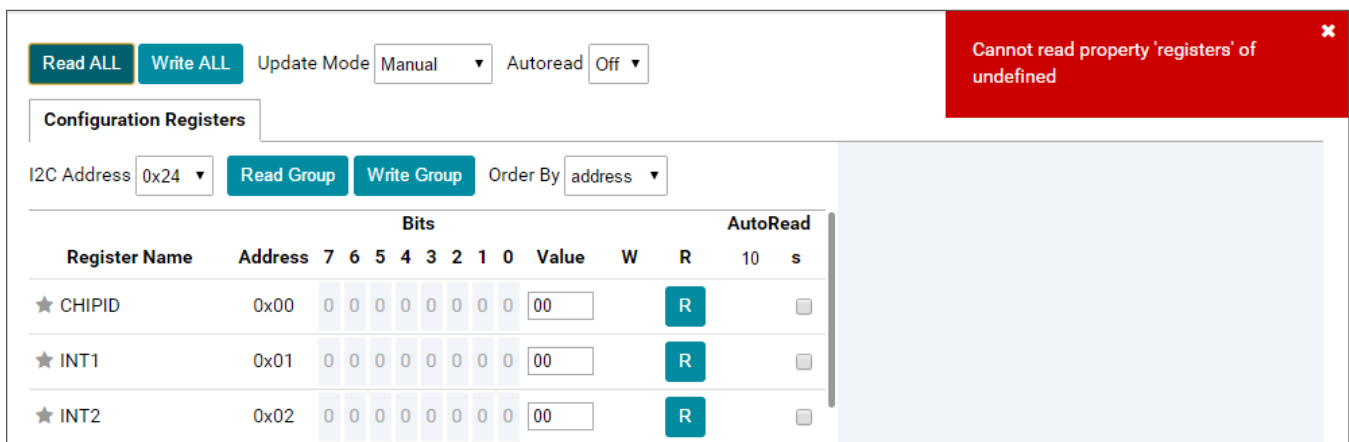
Figure 8. TPS65218D0 Project Introduction Tab in IPG-UI

- Click the *Read All* button and verify that data has changed in the **CHIPID** register from 0x00 to 0x05. Verify that only blue notifications appear. Blue notifications are informational only and do not indicate an error has occurred. Figure 9.



**Figure 9. Successful Write Access to TPS65218D0 Notification**

- If all register data remains 0x00 and a red notification appears (as in Figure 10), it indicates the computer can talk to the USB2ANY but cannot communicate with the TPS65218D0 device. The primary cause of this issue may be that the power switch for the BOOSTXL-TPS65218 is in the OFF position, the socket does not have a sample installed, or the USB cable is not plugged into the MSP430F5529 LaunchPad or the computer. In case of either issue, the test setup of the EVM must be debugged before continuing.



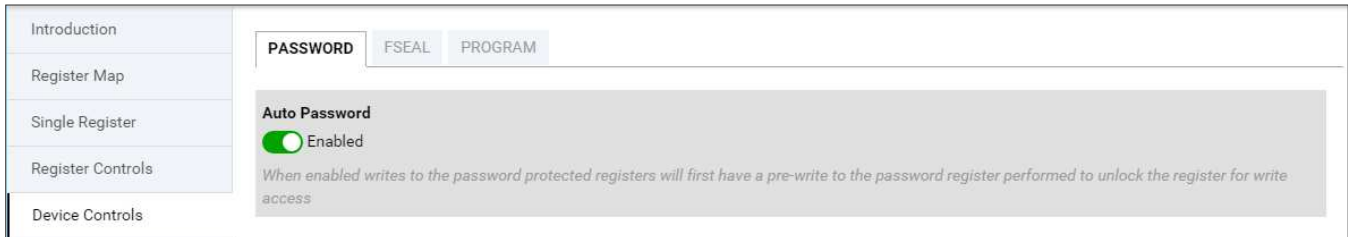
**Figure 10. Failed GUI Communication to TPS65218D0 Notification**

**NOTE:** At the time of writing this document, the IPG-UI software version is 2.5.0.4 and the TPS65218 file version is 1.2.

### A.3 Testing TPS65218D0 DCDC1 Voltage Change with IPG-UI

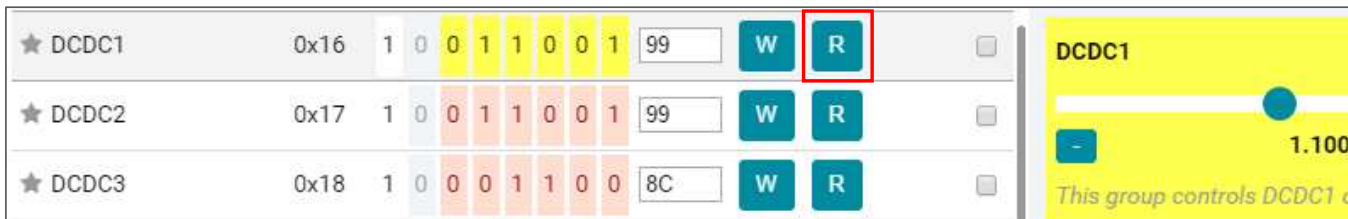
This section provides an example of how to use the IPG-UI software to read registers and modify the voltage of a single DC/DC converter of the TPS65218D0 device.

- Start by navigating to the *Device Controls* tab of the IPG-UI and verify that the Auto Password feature is Enabled, as shown in [Figure 11](#).



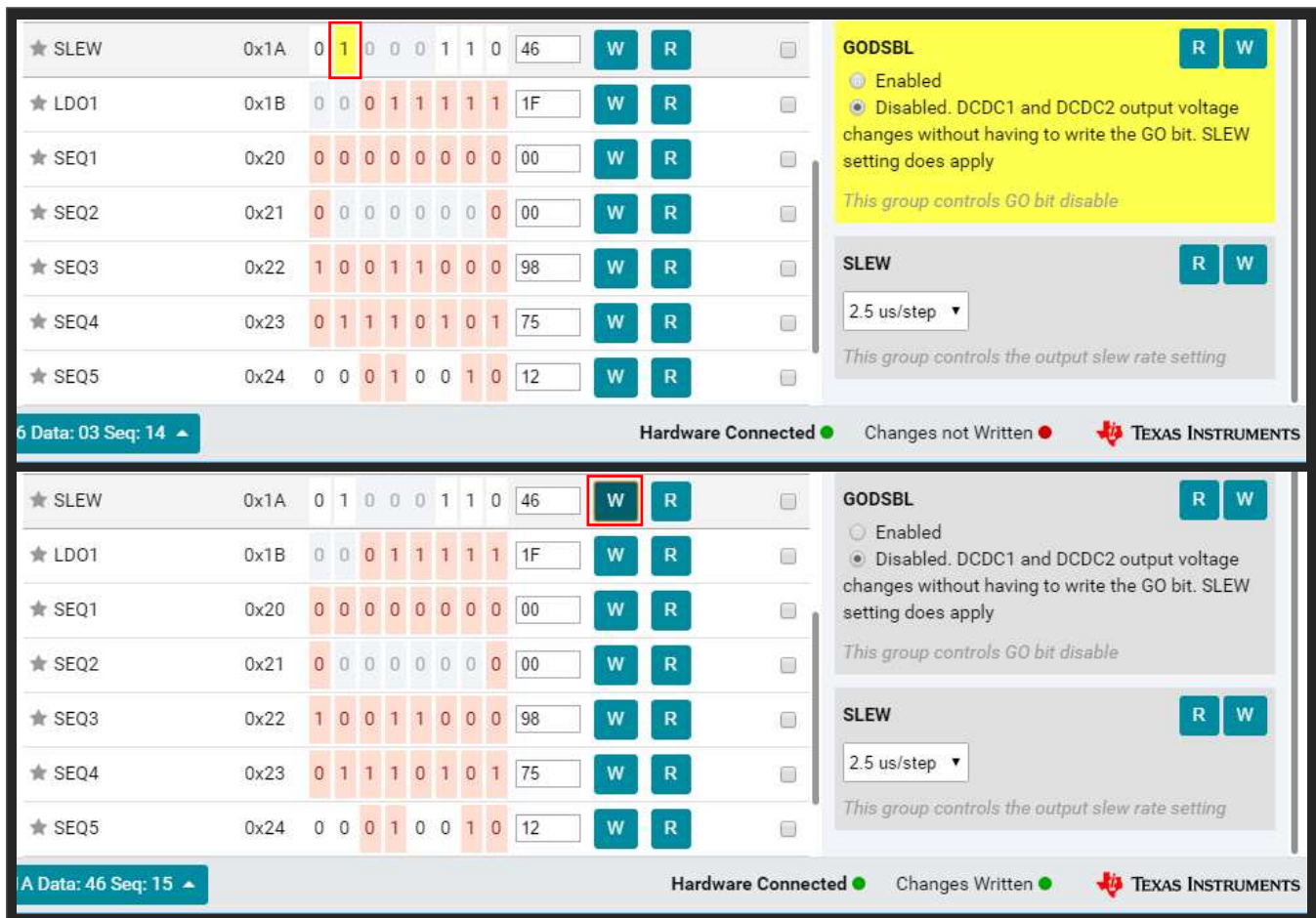
**Figure 11. Auto Password Write Enabled**

- Navigate back to the *Register Map* tab, click on the row for the **DCDC1** register (0x16), and read the value of this register by clicking the button labeled *R* in this row of the register map table, as shown in [Figure 12](#).



**Figure 12. DCDC1 Register, Default Value**

- Click on the row for the **SLEW** register (0x1A) and change the value of bit 6 in the from 0b to 1b by clicking the bit's cell in the table or clicking the radio button labeled *Disabled* on the right-hand side of the window. Write the new value of this register by clicking the button labeled *W* in this row of the register map table, as shown in [Figure 13](#).



The screenshot displays the IPG-UI interface for configuring the SLEW register (0x1A) and the DCDC1 register (0x16). The SLEW register configuration table is as follows:

Register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value	W	R
★ SLEW	0x1A	0	1	0	0	0	1	1	0	46	W	R
★ LDO1	0x1B	0	0	0	1	1	1	1	1	1F	W	R
★ SEQ1	0x20	0	0	0	0	0	0	0	0	00	W	R
★ SEQ2	0x21	0	0	0	0	0	0	0	0	00	W	R
★ SEQ3	0x22	1	0	0	1	1	0	0	0	98	W	R
★ SEQ4	0x23	0	1	1	1	0	1	0	1	75	W	R
★ SEQ5	0x24	0	0	0	1	0	0	1	0	12	W	R

The DCDC1 register (0x16) configuration table is as follows:

Register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value	W	R
★ DCDC1	0x16	0	0	0	0	0	0	0	0	00	W	R

The interface also shows the 'GODSBL' group controls, which are currently disabled. The 'SLEW' group controls show a value of 2.5 us/step. The status bar indicates 'Hardware Connected' and 'Changes Written'.

Figure 13. Disable GO Bit in SLEW Register

- Click on the row for the **DCDC1** register (0x16) again, and this time move the slider on the right-hand side of the window to change the output voltage of DCDC1 to a new value. Write the new value of this register by clicking the button labeled **W** in this row of the register map table, as shown in Figure 14. The value in the **PASSWORD** register (0x10) will also change because the IPG-UI is automatically writing the correct password to this register in advance so that the DCDC1 register will accept the new data.

The screenshot shows the 'Configuration Registers' interface. A table lists registers with their I2C addresses, bit patterns, and values. The 'DCDC1' register at address 0x16 is highlighted with a red box, and its 'W' button is also highlighted. The register value is 8F. To the right, the DCDC1 configuration panel shows the output voltage set to 1.000 V.

Register Name	I2C Address	Bit Pattern	Value	W	R
PASSWORD	0x10	0 1 1 0 1 0 1 1	6B	W	R
ENABLE1	0x11	0 0 1 1 1 1 1 1	3F	W	R
ENABLE2	0x12	0 0 0 1 0 0 1 1	13	W	R
CONFIG1	0x13	0 1 0 0 1 1 0 0	4C	W	R
CONFIG2	0x14	1 1 0 0 0 0 0 0	C0	W	R
CONFIG3	0x15	0 0 0 0 0 0 0 0	00	W	R
DCDC1	0x16	1 0 0 0 1 1 1 1	8F	W	R

Figure 14. Modifying DCDC1 Register Value

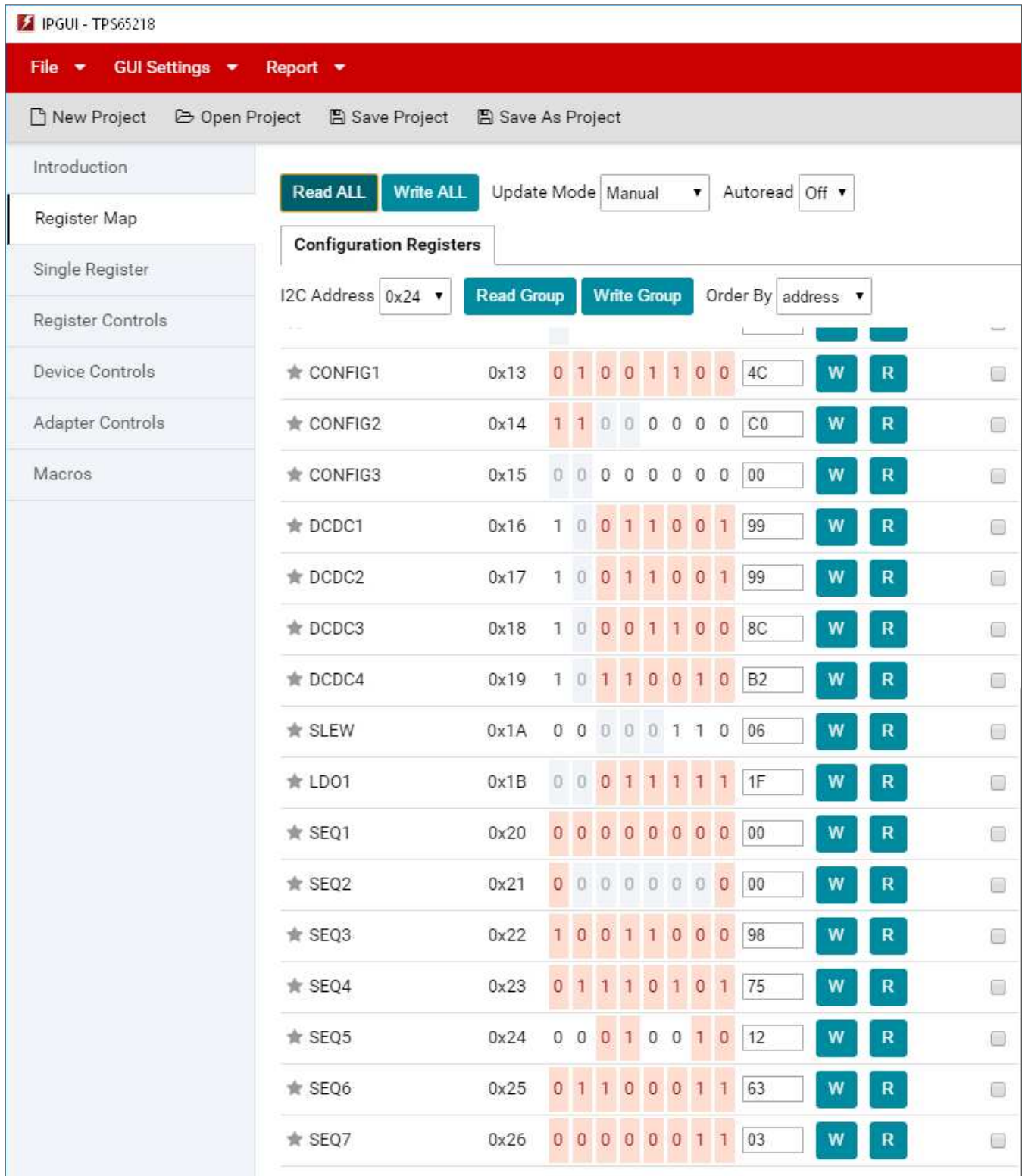
- Verify the new voltage setting by measuring TP22 on the BOOSTXL-TPS65218 board with a multi-meter.

#### A.4 Re-Programming the EEPROM of the TPS65218D0 Device

This section provides an example of how to re-write the EEPROM of the TPS65218D0 device using the IPG-UI and visually verify that the new values have been correctly programmed into the non-volatile EEPROM memory of the device. The most commonly programmed values, DC/DC converter output voltage and sequencing order, will be modified in this example.

**NOTE:** All of the bits that are backed by EEPROM and are programmable are highlighted in red in the Register Map section of the IPG-UI software for the TPS65218D0 device. Bits that are grayed out are Reserved and are Read-Only. The bits with no color-coding are Read-Write capable and can be edited in real-time, but this memory is volatile and the values will not be stored when the TPS65218D0 device is power-cycled.

- Figure 15 shows all of the available EEPROM-backed registers of the TPS65218D0 that may be programmed.



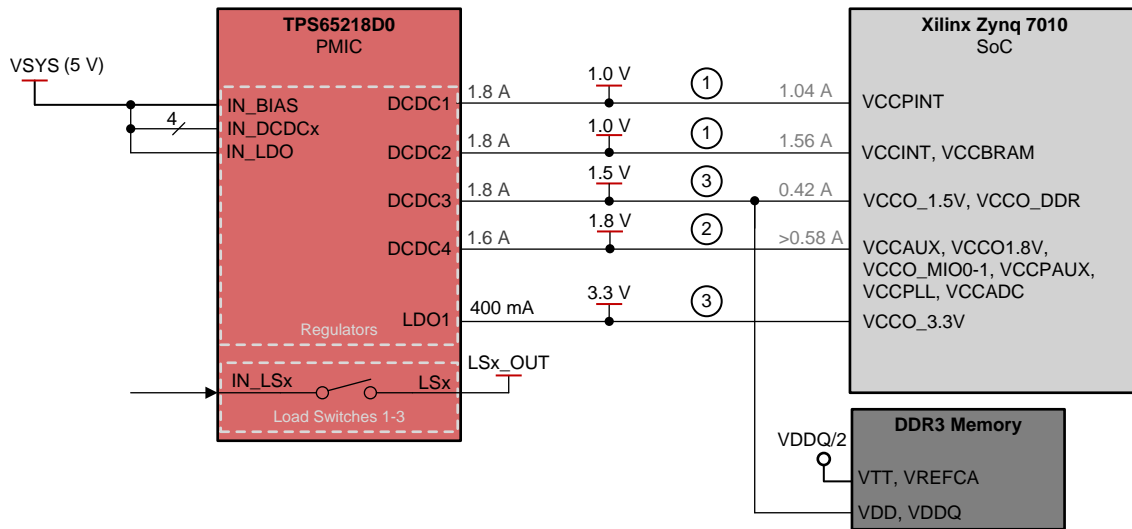
The screenshot shows the IPGUI - TPS65218 software interface. The top menu bar includes 'File', 'GUI Settings', and 'Report'. Below the menu bar are buttons for 'New Project', 'Open Project', 'Save Project', and 'Save As Project'. The left sidebar contains a navigation menu with items: 'Introduction', 'Register Map', 'Single Register', 'Register Controls', 'Device Controls', 'Adapter Controls', and 'Macros'. The main area displays the 'Configuration Registers' section. At the top of this section are buttons for 'Read ALL' and 'Write ALL', along with 'Update Mode' set to 'Manual' and 'Autoread' set to 'Off'. Below these are 'I2C Address' set to '0x24', 'Read Group', 'Write Group', and 'Order By' set to 'address'. The main part of the interface is a table of configuration registers, each with a star icon, name, I2C address, a bit pattern, a value field, and 'W' and 'R' buttons. The registers listed are CONFIG1 through SEQ7.

Register Name	I2C Address	Bit Pattern	Value	W	R
★ CONFIG1	0x13	0 1 0 0 1 1 0 0	4C	W	R
★ CONFIG2	0x14	1 1 0 0 0 0 0 0	C0	W	R
★ CONFIG3	0x15	0 0 0 0 0 0 0 0	00	W	R
★ DCDC1	0x16	1 0 0 1 1 0 0 1	99	W	R
★ DCDC2	0x17	1 0 0 1 1 0 0 1	99	W	R
★ DCDC3	0x18	1 0 0 0 1 1 0 0	8C	W	R
★ DCDC4	0x19	1 0 1 1 0 0 1 0	B2	W	R
★ SLEW	0x1A	0 0 0 0 0 1 1 0	06	W	R
★ LD01	0x1B	0 0 0 1 1 1 1 1	1F	W	R
★ SEQ1	0x20	0 0 0 0 0 0 0 0	00	W	R
★ SEQ2	0x21	0 0 0 0 0 0 0 0	00	W	R
★ SEQ3	0x22	1 0 0 1 1 0 0 0	98	W	R
★ SEQ4	0x23	0 1 1 1 0 1 0 1	75	W	R
★ SEQ5	0x24	0 0 0 1 0 0 1 0	12	W	R
★ SEQ6	0x25	0 1 1 0 0 0 1 1	63	W	R
★ SEQ7	0x26	0 0 0 0 0 0 1 1	03	W	R

**Figure 15. EEPROM-Backed Registers of the TPS65218D0**

- For this example, the TPS65218D0 will be re-programmed from its original settings to provide power to the SoC shown in [Figure 16](#).





(1) The power-on sequence order is listed for each rail, numbered 1-3.

**Figure 16. TPS65218D0 Re-Programming Example Block Diagram**

- When using a new TPS65218D0 sample IC, the EEPROM values will match a bank of one-time programmable (OTP) values also stored in the device. Figure 17 shows that when the EEPROM values have not yet been re-programmed, bit 6 of the **STATUS** register (0x05) will have a value of 0b.

Register Name	Address	7	6	5	4	3	2	1	0	Value	W	R	AutoRead
★ CHIPID	0x00	0	0	0	0	0	1	0	1	05		R	
★ INT1	0x01	0	0	0	0	0	0	0	0	00		R	
★ INT2	0x02	0	0	0	0	0	0	0	0	00		R	
★ INT_MASK1	0x03	0	0	0	0	0	0	0	0	00	W	R	
★ INT_MASK2	0x04	0	0	0	0	0	0	0	0	00	W	R	
★ STATUS	0x05	0	0	1	0	1	0	0	0	28		R	
★ CONTROL	0x06	0	0	0	0	0	0	0	0	00	W	R	
★ FLAG	0x07	0	0	0	0	0	0	0	0	00		R	
★ PASSWORD	0x10	0	0	0	0	0	0	0	0	00	W	R	

**Figure 17. EEPROM Not Changed (EE Bit = 0b) in Status Register**

- The original value of the **STRICT** bit in the **CONFIG1** register (0x13) is 1b. For this example, the tight supervisor tolerances are not required, so the **STRICT** bit is changed to 0b, as shown in Figure 18. Similarly, the dynamic voltage scaling of the TPS65218D0 device is not required. As a result, the value of the **DC12\_RST** bit in **CONFIG2** register (0x14) is set to 0b to disable the feature that allows GPIO3

to trigger a warm reset for the DCDC1 and DCDC2 converters.

★ CONFIG1	0x13	0	1	0	0	1	0	0	0	48	W	R		<b>STRICT</b> <span>R</span> <span>W</span> <input checked="" type="radio"/> Power good threshold has wider limits. Over-voltage is not monitored <input type="radio"/> Power good threshold has tight limits. Over-voltage is monitored <i>This group controls the supply voltage supervisor sensitivity selection</i>
★ CONFIG2	0x14	1	1	0	0	0	0	0	0	C0	W	R		
★ CONFIG3	0x15	0	0	0	0	0	0	0	0	00	W	R		
★ DCDC1	0x16	1	0	0	1	1	0	0	1	99	W	R		
★ CONFIG2	0x14	0	1	0	0	0	0	0	0	40	W	R		<b>DC12_RST</b> <span>R</span> <span>W</span> <input checked="" type="radio"/> GPIO3 is configured as general purpose output <input type="radio"/> GPIO3 is configured as warm-reset input to DCDC1 and DCDC2 <i>This group controls the DCDC1 and DCDC2 reset pin enable</i>
★ CONFIG3	0x15	0	0	0	0	0	0	0	0	00	W	R		
★ DCDC1	0x16	1	0	0	1	1	0	0	1	99	W	R		
★ DCDC2	0x17	1	0	0	1	1	0	0	1	99	W	R		

**Figure 18. Modifying CONFIG1 and CONFIG2 Register Values**

- The voltage setpoint of DCDC1 has already been modified, so only the remaining DC/DC converters and LDO1 regulator voltages need to be modified at this time. [Figure 19](#) shows the new output voltage setpoint configured in the **DCDC2**, **DCDC3**, **DCDC4**, and **LDO1** registers (0x17, 0x18, 0x19, and 0x1B) as well as the correct **PASSWORD** register (0x10) value written automatically by the IPG-UI.

The screenshot shows the TI Configurator interface for the TPS65218D0 device. It is divided into four sections, each corresponding to a different register being modified:

- Section 1:** The 'PASSWORD' register (0x10) is set to 6A. The 'DCDC2' register (0x17) is selected, with its value set to 8F. The right-hand view shows the DCDC2 output voltage slider set to 1.000 V.
- Section 2:** The 'PASSWORD' register (0x10) is set to 65. The 'DCDC3' register (0x18) is selected, with its value set to 98. The right-hand view shows the DCDC3 output voltage slider set to 1.500 V.
- Section 3:** The 'PASSWORD' register (0x10) is set to 64. The 'DCDC4' register (0x19) is selected, with its value set to 94. The right-hand view shows the DCDC4 output voltage slider set to 1.800 V.
- Section 4:** The 'PASSWORD' register (0x10) is set to 66. The 'LDO1' register (0x1B) is selected, with its value set to 3D. The right-hand view shows the LDO1 output voltage slider set to 3.300 V.

Figure 19. Modifying DCDC2-4 and LDO1 Register Values

**NOTE:** Extreme changes in output voltage settings for DCDC1-4 and LDO1 may not settle to the desired voltage before the TPS65218D0 supervisor circuitry recognizes the voltage as an overvoltage or undervoltage fault condition and performs a system reset. This will reset the DCDC1-4 and LDO1 registers to the value currently stored in EEPROM and is desirable in the end application, but it will prevent successful re-programming with new output voltage settings. If this issue is observed while modifying registers prior to re-programming the EEPROM, then a value of 0x00 must be written to the **ENABLE1** and **ENABLE2** registers (0x11 and 0x12) before re-starting this procedure.

- To match the example, the order in which the DC/DC converters and LDO turn on and turn off is must be changed. This order, or sequencing, is changed by modifying the **SEQ3**, **SEQ4**, and **SEQ6** registers (0x22, 0x23, and 0x25), as shown in Figure 20. GPIO3 is no longer used to trigger a warm-reset for DCDC1 and DCDC2, so the **SEQ7** register (0x26) has been modified to enable GPIO3 in the sequence to indicate all of the DC/DC converters and LDO1 have been enabled.

The screenshot displays the IPG-UI interface for configuring the TPS65218D0 device. At the top, there are controls for I2C Address (0x24), Read Group, Write Group, and Order By (address). A table lists registers SEQ1 through SEQ7 with their addresses and bit patterns. Below this, four detailed panels show the configuration for SEQ3, SEQ4, SEQ6, and SEQ7. Each panel includes a description of the register's function and specific settings for DC, LS, and GPO sequences.

Register	Address	Bit Pattern	Value
SEQ1	0x20	0 0 0 0 0 0 0 0	00
SEQ2	0x21	0 0 0 0 0 0 0 0	00
SEQ3	0x22	0 0 1 1 0 0 1 1	33
SEQ4	0x23	0 1 0 1 0 1 1 1	57
SEQ5	0x24	0 0 0 1 0 0 1 0	12
SEQ6	0x25	1 0 1 0 0 1 1 1	A7
SEQ7	0x26	1 0 0 0 0 0 1 1	83

Figure 20. Modifying Sequence (SEQ3-4, SEQ6) Registers

- To re-program the EEPROM of the TPS65218D0 device and make these changes permanent, a special sequence of three (3) bytes must be written to the **PASSWORD** register (0x10) without any other I2C commands in between the three Write commands. Figure 21 shows how to perform this sequence manually and Figure 22 shows how to use the IPG-UI to automatically write the correct sequence to the TPS65218D0 device.

The screenshot shows three consecutive write operations to the PASSWORD register (0x10). Each row shows the register name, address, bit pattern, value, and a 'W' button. The values are 50, 1A, and CE. The 'W' buttons are highlighted with red boxes, and the 'R' buttons are crossed out with red 'X' marks.

Register	Address	Bit Pattern	Value
PASSWORD	0x10	0 1 0 1 0 0 0 0	50
PASSWORD	0x10	0 0 0 1 1 0 1 0	1A
PASSWORD	0x10	1 1 0 0 1 1 1 0	CE

Figure 21. Manually Writing PASSWORD Sequence to Re-Program EEPROM

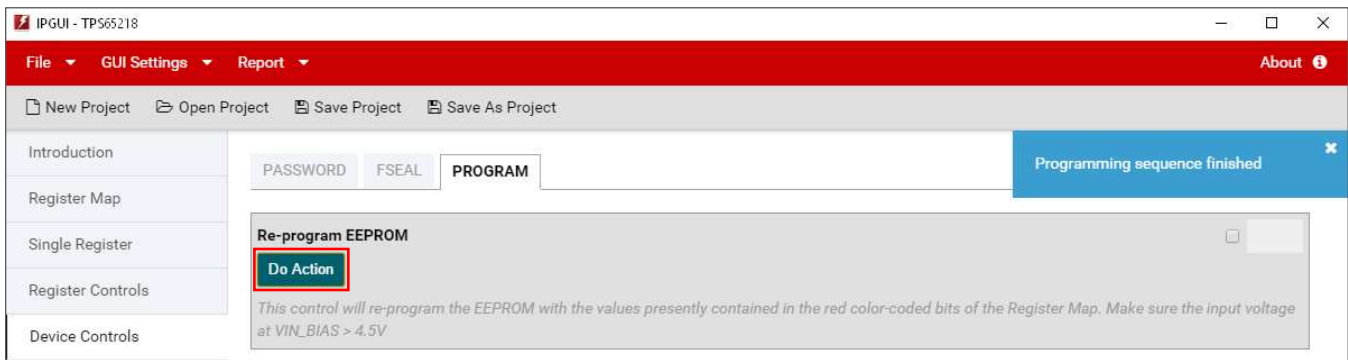


Figure 22. Automatically Writing PASSWORD Sequence to Re-Program EEPROM

- After the sequence is written to re-program the TPS65218D0 device EEPROM, there are a few indicators that the EEPROM has been re-programmed correctly. Figure 23 shows that the **PRGC** bit of the **INT1** interrupt register (0x01) is set to 1b, the **EE** bit of the **STATUS** register (0x05) is set to 1b, and the **PASSWORD** register (0x10) has retained the last byte (0xCE) of the special programming sequence.

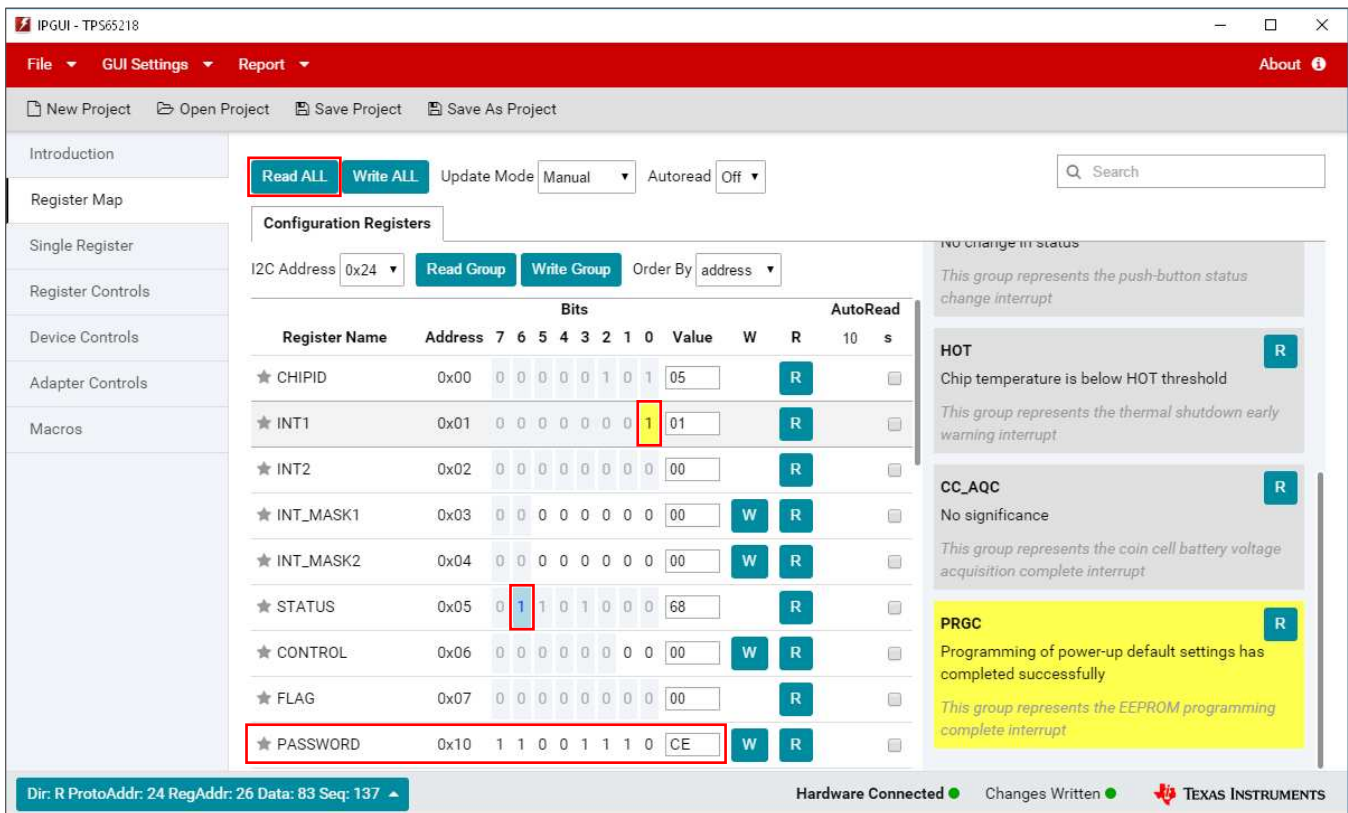


Figure 23. Interrupt for Successful Programming in INT1

**NOTE:** If the voltage on the VIN\_BIAS pin of the TPS65218D0 is less than or equal to 4.5V, this is too low for re-programming the EEPROM and bit 5 (**VPRG**) of the **INT1** register will be set to 1b instead to indicate the voltage is too low for programming.

- Now the BOOSTXL-TPS65218 board can be reset by moving S1 (labeled *MAIN PWR*) to the *GND* position and then moving it back to the *HI* position. Click *Read All* on the IPG-UI one more time to verify that the **EE** bit in the **STATUS** register (0x05) remains set to 1b, the **PASSWORD** register resets to

0x00, and all of the registers programmed into the EEPROM retain the new values. Figure 24 shows all of the registers that have been re-programmed in this example, as well as the volatile bits that have changed after power cycling the TPS65218D0 device.

Configuration Registers

I2C Address 0x24
Read Group
Write Group
Order By address

★ STATUS	0x05	0	1	1	0	1	0	0	0	68	R	☐	
★ CONTROL	0x06	0	0	0	0	0	0	0	0	00	W	R	☐
★ FLAG	0x07	0	0	0	0	0	0	0	0	00	R	☐	
★ PASSWORD	0x10	0	0	0	0	0	0	0	0	00	W	R	☐
★ ENABLE1	0x11	0	0	1	1	1	1	1	1	3F	W	R	☐
★ ENABLE2	0x12	0	1	0	1	0	0	1	1	53	W	R	☐
★ CONFIG1	0x13	0	1	0	0	1	0	0	0	48	W	R	☐
★ CONFIG2	0x14	0	1	0	0	0	0	0	0	40	W	R	☐
★ CONFIG3	0x15	0	0	0	0	0	0	0	0	00	W	R	☐
★ DCDC1	0x16	1	0	0	0	1	1	1	1	8F	W	R	☐
★ DCDC2	0x17	1	0	0	0	1	1	1	1	8F	W	R	☐
★ DCDC3	0x18	1	0	0	1	1	0	0	0	98	W	R	☐
★ DCDC4	0x19	1	0	0	1	0	1	0	0	94	W	R	☐
★ SLEW	0x1A	0	0	0	0	0	1	1	0	06	W	R	☐
★ LD01	0x1B	0	0	1	1	1	1	0	1	3D	W	R	☐
★ SEQ1	0x20	0	0	0	0	0	0	0	0	00	W	R	☐
★ SEQ2	0x21	0	0	0	0	0	0	0	0	00	W	R	☐
★ SEQ3	0x22	0	0	1	1	0	0	1	1	33	W	R	☐
★ SEQ4	0x23	0	1	0	1	0	1	1	1	57	W	R	☐
★ SEQ5	0x24	0	0	0	1	0	0	1	0	12	W	R	☐
★ SEQ6	0x25	1	0	1	0	0	1	1	1	A7	W	R	☐
★ SEQ7	0x26	1	0	0	0	0	0	1	1	83	W	R	☐

### STATUS

This register contains status settings

**FSEAL** R  
 FSEAL is in native state  
*This group represents the freshness seal status*

**EE** R  
 EEPROM values have been changed from factory default  
*This group represents the EEPROM status*

**AC\_STATE** R  
 AC\_DET input is active  
*This group represents the AC\_DET input status*

**PB\_STATE** R  
 Push button input is inactive  
*This group represents the push button status*

**STATE** R  
 PMIC is in ACTIVE state  
*This group represents the state machine STATE indication*

**CC\_STAT** R  
 Coin cell is not present or approaching end-of-life  
*This group represents the coin cell state of charge*

Figure 24. Registers 0x05-0x26 After Successful Re-Programming, EEPROM Changed (EE Bit = 1b) in Status Register

The EEPROM re-programming was successful because the IPG-UI remembers the previous value of bits before the *Read All* button is pressed and highlights changes in blue. There are some bits highlighted in blue in [Figure 24](#), but these differences do not indicate a failed EEPROM re-programming. The **PASSWORD** register (0x10) has reset to 0x00 because the power cycle has cleared this info that is not backed by EEPROM. Bit 6 of the **ENABLE2** register (0x12) is set to 1b now because GPIO3 is enabled after all of the DC/DC converters and LDO1 have been enabled. Bit 6 of the **SLEW** register (0x1A) has reset to 0b because the **GODSBL** bit is not backed by EEPROM. None of the EEPROM-backed bits (highlighted in red) that were changed in the example re-programming have been highlighted in blue.

The successful re-programming of the EEPROM can also be verified on the BOOSTXL-TPS65218 hardware by measuring the output voltages of DCDC1, DCDC2, DCDC3, DCDC4, and LDO1 with a multi-meter and by measuring the power-on sequence timing with an oscilloscope.

#### CAUTION

The BOOSTXL-TPS65218 board is intended for re-programming the EEPROM of the TPS65218D0 only. Significant loads should not be applied to the DC/DC converters, LDO1 regulator, or LS1-3 load switches using the BOOSTXL-TPS65218 test points. The newly re-programmed TPS65218D0 device must be removed from the socket and soldered down onto a TPS65218EVM-100 board or another board designed to carry the current for maximum loads to evaluate the full performance of the TPS65218D0 device.

## EVM Documentation

### B.1 Layout

Figure 25 through Figure 32 show the board layout for the BOOSTXL-TPS65218

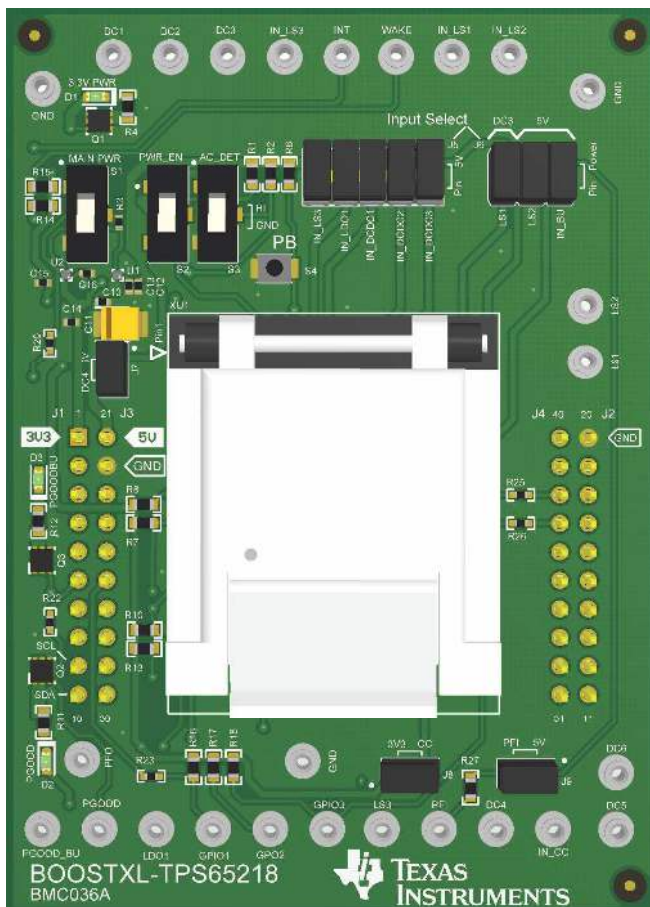


Figure 25. Component Placement—Top Assembly

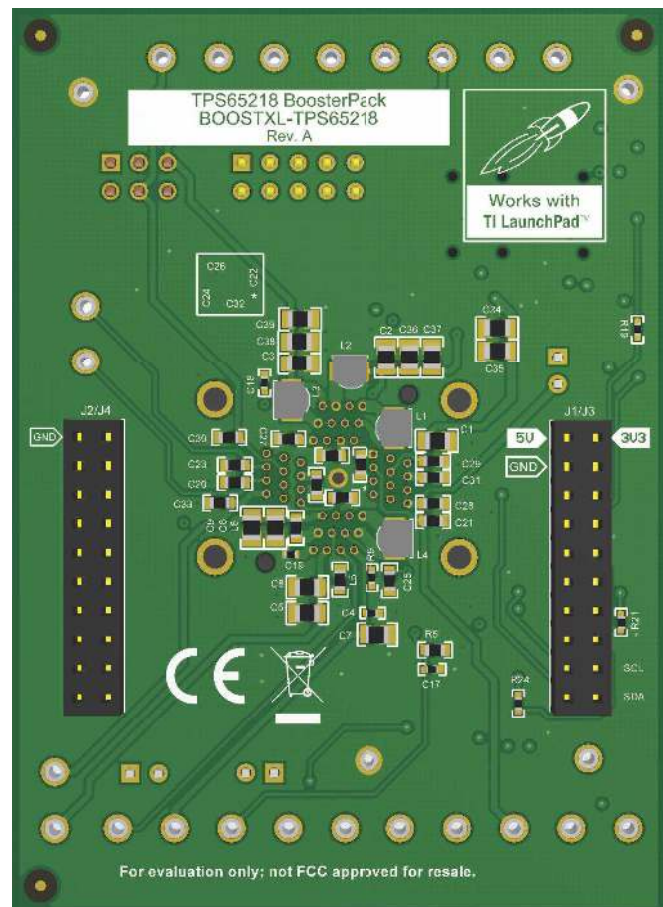


Figure 26. Component Placement—Bottom Assembly



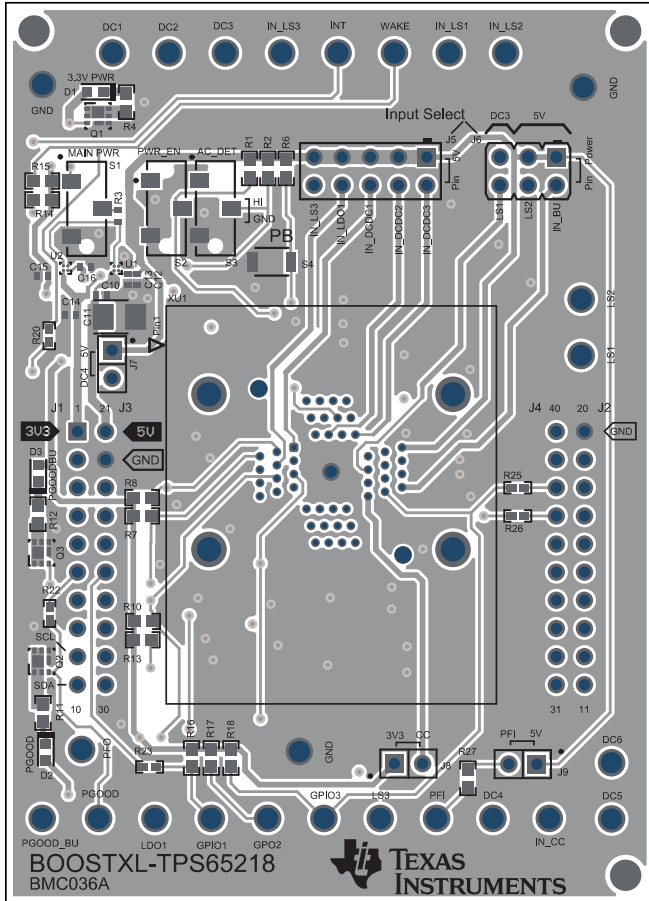


Figure 27. Layout—Top Composite

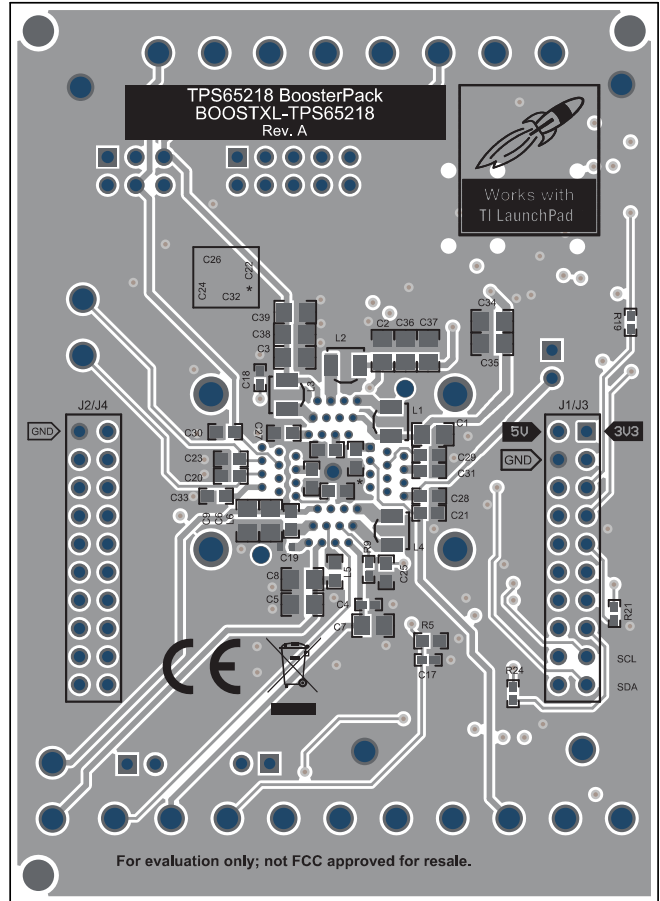


Figure 28. Layout—Bottom Composite

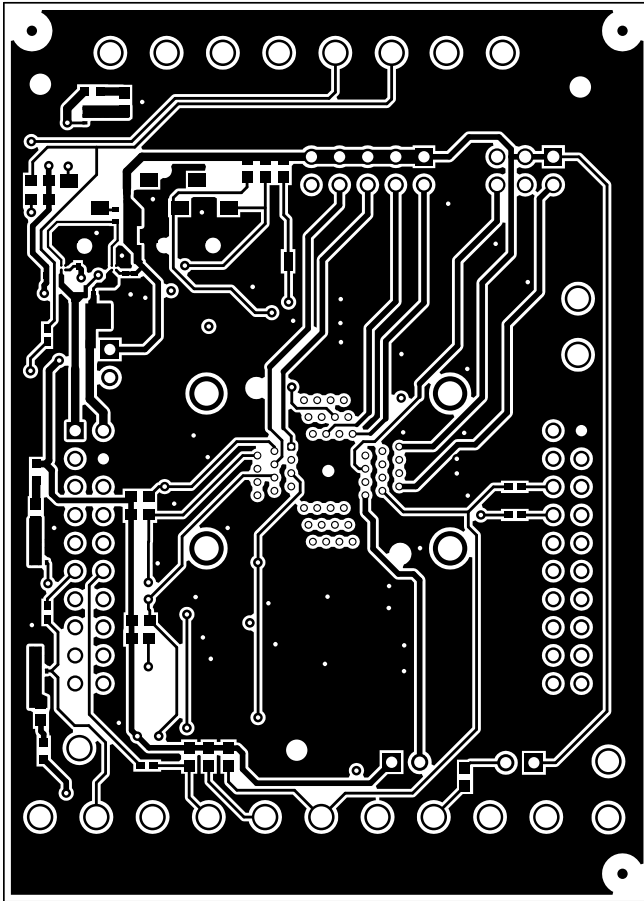


Figure 29. Top Layer

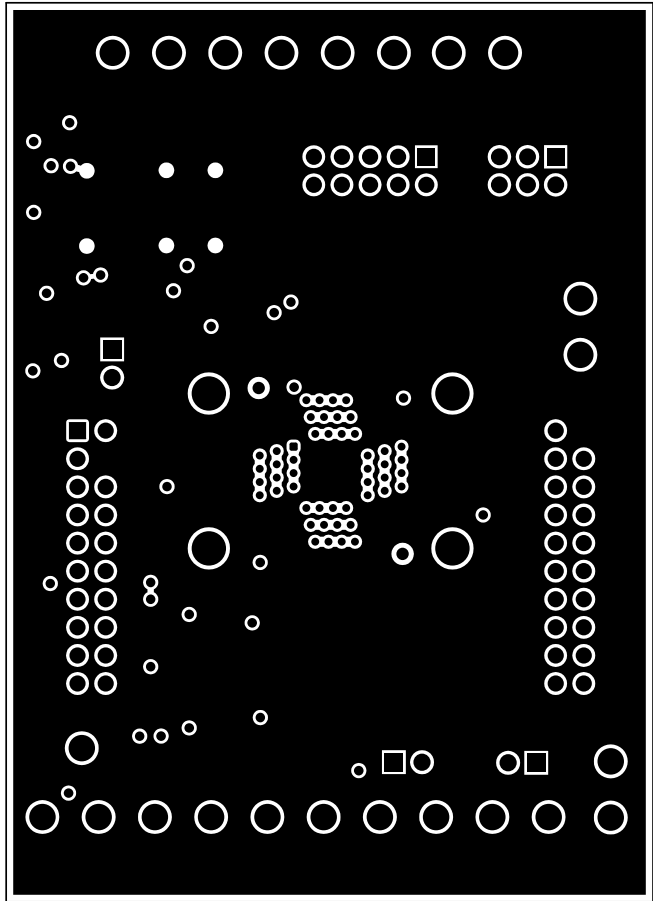


Figure 30. Inner Layer 1 (GND Plane)

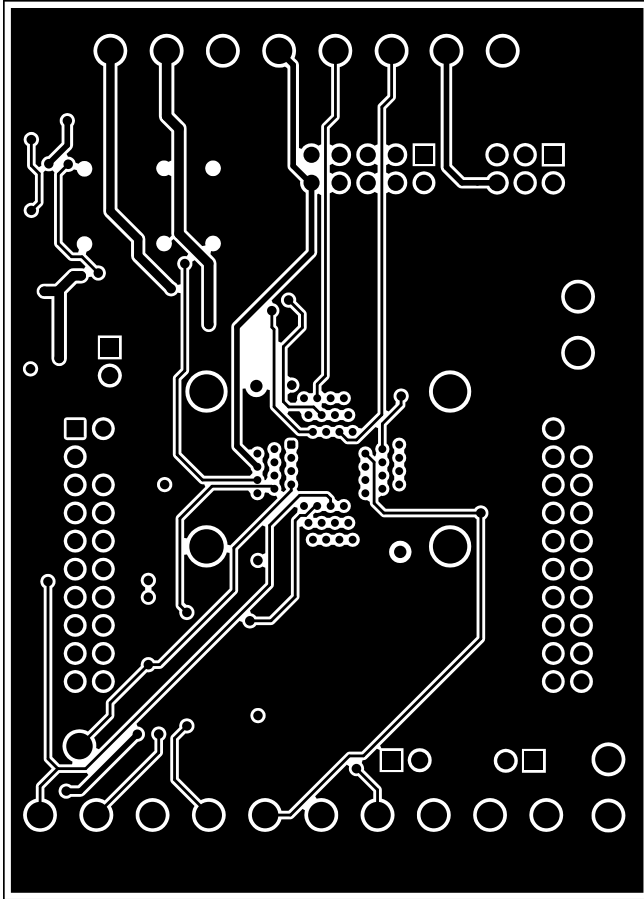


Figure 31. Inner Layer 2 (Signal)

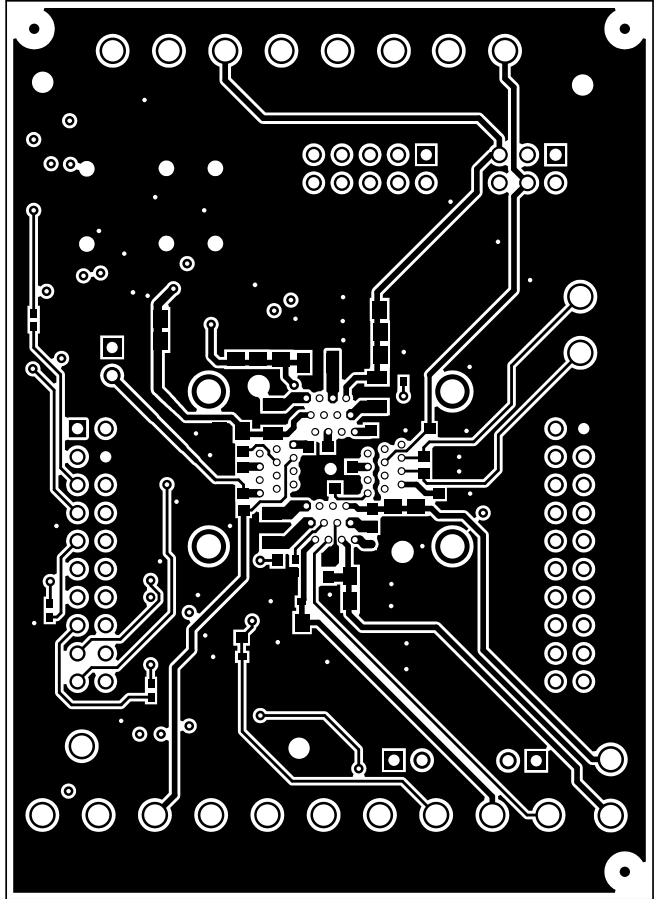
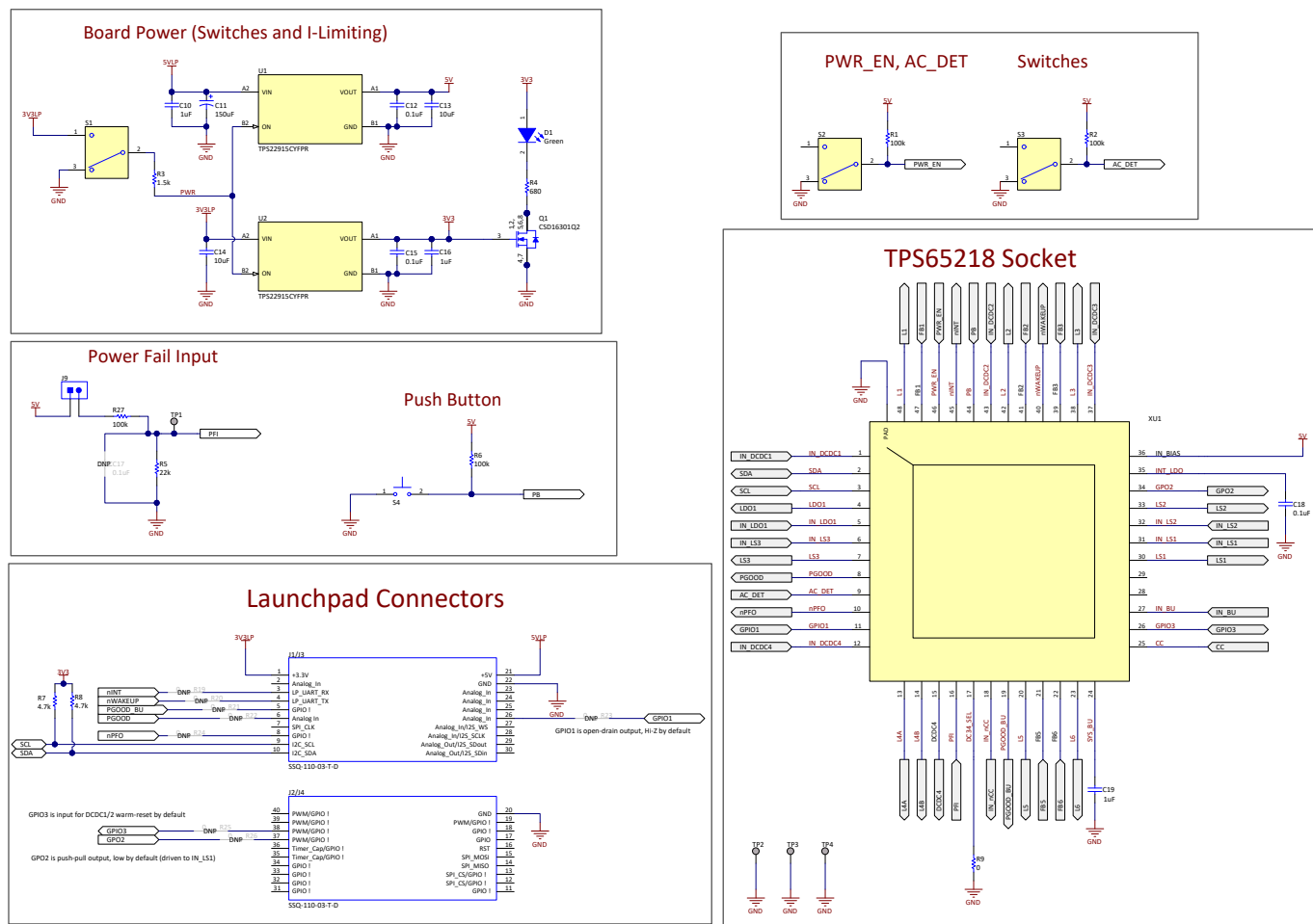


Figure 32. Bottom Layer (Top View)

## B.2 Schematic

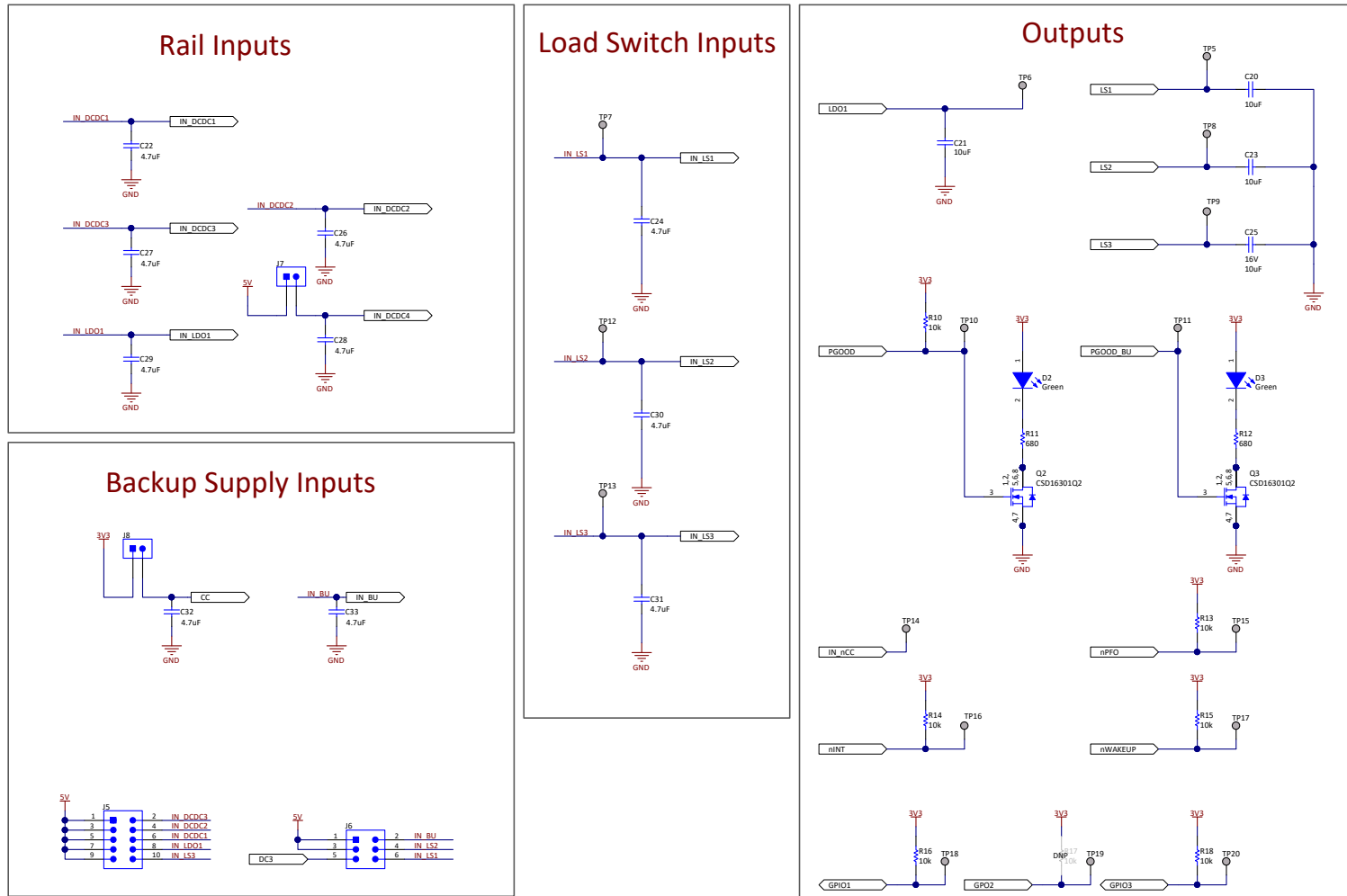
Figure 33 shows the 1st page of the schematic for BOOSTXL-TPS65218.



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Figure 33. BOOSTXL-TPS65218 Schematic, Page 1

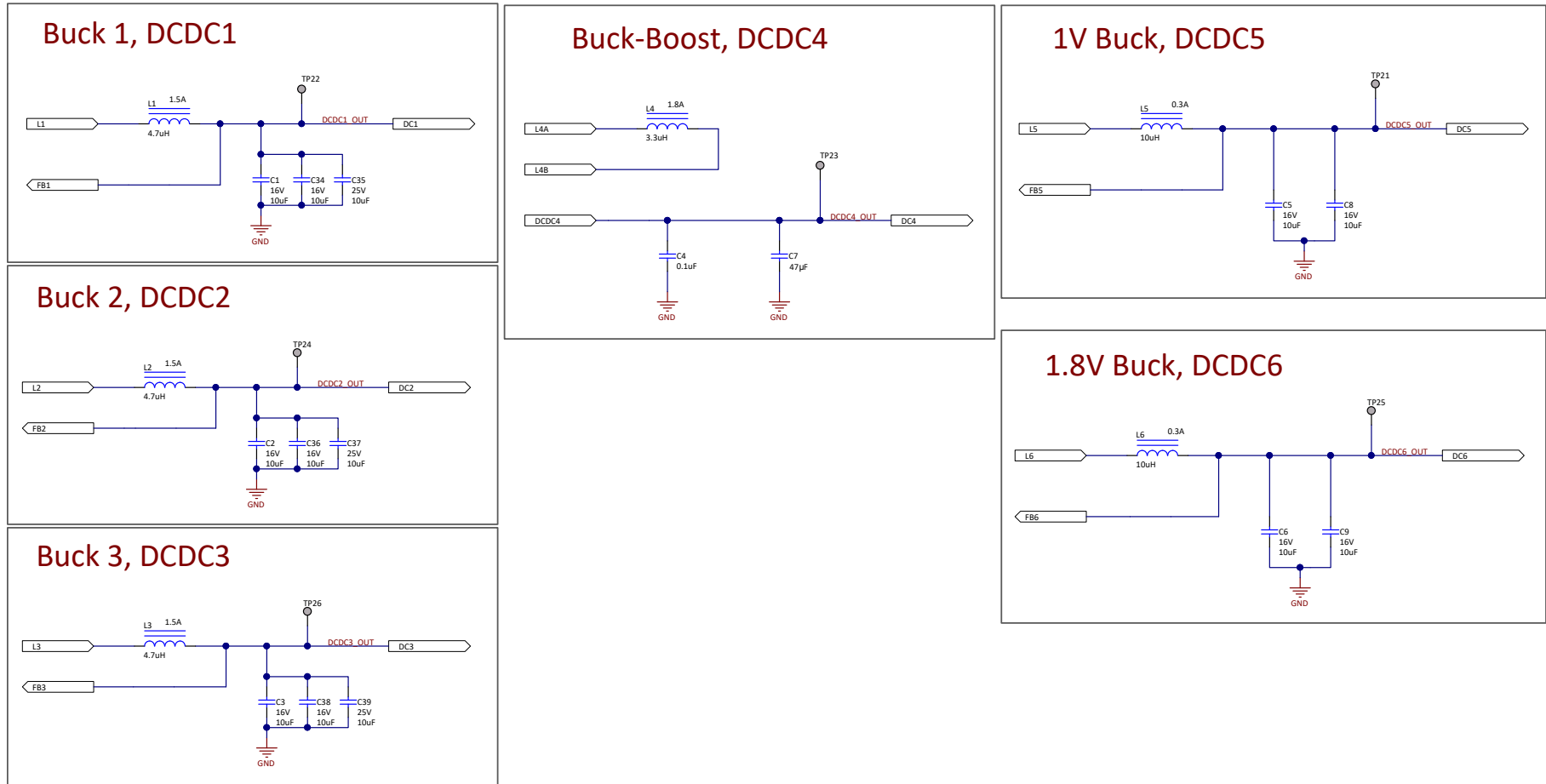
Figure 34 shows the 2nd page of the schematic for BOOSTXL-TPS65218.



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Figure 34. BOOSTXL-TPS65218 Schematic, Page 2

Figure 35 shows the 3rd page of the schematic for BOOSTXL-TPS65218.



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Figure 35. BOOSTXL-TPS65218 Schematic, Page 3

### B.3 Bill of Materials

Table 4 provides the bill of materials (BOM) for the BOOSTXL-TPS65218.

**Table 4. Bill of Materials**

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		BMC036	Any
C1, C2, C3, C5, C6, C8, C9, C34, C36, C38	10	10uF	CAP, CERM, 10 uF, 16 V, +/- 10%, X5R, 0805	0805	GRM21BR61C106KE15L	MuRata
C4, C18	2	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A104K050BA	TDK
C7	1	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A476ME15L	MuRata
C10, C16, C19	3	1uF	CAP, CERM, 1 uF, 35 V, +/- 20%, X5R, 0402	0402	GRM155R6YA105ME11D	MuRata
C11	1	150uF	CAP, TA, 150 uF, 6.3 V, +/- 20%, 0.025 ohm, SMD	3528-21	T520B157M006ATE025	Kemet
C12, C15	2	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	GRM155R61A104KA01D	MuRata
C13, C14	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402	0402	CL05A106MP5NUNC	Samsung Electro-Mechanics
C20, C21, C23	3	10uF	CAP, CERM, 10 uF, 10 V, +/- 10%, X6S, 0603	0603	C1608X6S1A106M080AC	TDK
C22, C24, C26, C27, C28, C29, C30, C32, C33	9	4.7uF	CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet
C25	1	10uF	CAP, CERM, 10 uF, 16 V, +/- 20%, X5R, 0603	0603	GRM188R61C106MAALD	MuRata
C31	1	4.7uF	CAP, CERM, 4.7 uF, 16 V, +/- 10%, X5R, 0603	0603	GRM188R61C475KAAJ	MuRata
C35, C37, C39	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	0805	TMK212BBJ106KG-T	Taiyo Yuden
D1, D2, D3	3	Green	LED, Green, SMD	0.8x1.6 mm	HSMG-C190	Avago
H1	1		IC to place in Socket XU1		TPS65218D0RS LR	Texas Instruments
J1/J3, J2/J4	2		Receptacle, 2.54 mm, 10x2, Tin, TH	10x2 Receptacle	SSQ-110-03-T-D	Samtec
J5	1		Header, 2.54 mm, 5x2, Gold, Black, TH	Header, 2.54mm, 5x2, TH	TSW-105-07-F-D	Samtec
J6	1		Header, 2.54mm, 3x2, Gold, TH	Header, 2.54mm, 3x2, TH	61300621121	Würth Elektronik
J7, J8, J9	3		Header, 100mil, 2x1, Tin, TH	Header 2x1	90120-0122	Molex

**Table 4. Bill of Materials (continued)**

L1, L2, L3	3	4.7uH	Inductor, Shielded, Ferrite, 4.7 uH, 1.5 A, 0.27 ohm, SMD	SMD, 2-Leads, Body 3.2x3 mm	SPM3012T-4R7M	TDK
L4	1	3.3uH	Inductor, Shielded, Ferrite, 3.3 uH, 1.8 A, 0.21 ohm, SMD	SMD, 2-Leads, Body 3.2x3 mm	SPM3012T-3R3M	TDK
L5, L6	2	10uH	Inductor, Multilayer, Ferrite, 10 uH, 0.3 A, 0.6 ohm, SMD	0603	MLZ1608N100LT000	TDK
Q1, Q2, Q3	3	25V	MOSFET, N-CH, 25 V, 5 A, DQK0006C (WSON-6)	DQK0006C	CSD16301Q2	Texas Instruments
R1, R2, R6, R27	4	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R3	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R4, R11, R12	3	680	RES, 680, 5%, 0.1 W, 0603	0603	RC0603JR-07680RL	Yageo
R5	1	22k	RES, 22 k, 5%, 0.1 W, 0603	0603	RC0603JR-0722KL	Yageo
R7, R8	2	4.7k	RES, 4.7 k, 5%, 0.1 W, 0603	0603	RC0603JR-074K7L	Yageo America
R9	1	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R10, R13, R14, R15, R16, R18	6	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
S1, S2, S3	3		Switch, Slide, SPDT, 0.2 A, J Lead, SMD	SMD, 3-Leads, Body 8.5x3.5 mm, Pitch 2.5 mm	CL-SB-12A-01T	Copal Electronics
S4	1		SWITCH TACTILE SPST-NO 0.05 A 12 V	3x1.6x2.5 mm	B3U-1000P	Omron Electronic Components
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11	11	1x2	Shunt, 100 mil, Flash Gold, Black	Closed Top 100 mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	26		PCB Pin, Swage Mount, TH	PCB Pin(2505-2)	2505-2-00-44-00-00-07-0	Mill-Max



**Table 4. Bill of Materials (continued)**

U1, U2	2		5.5 V, 2A, 38 mΩ Load Switch With Quick Output Discharge, YFP0004AAAA (DSBGA-4)	YFP0004AAAA	TPS22915CYFPR	Texas Instruments
XU1	1		Socket, QFN-48, 0.4 mm Pitch	Socket, QFN-48, 0.4 mm Pitch	QFN-48(52)BT-0.4-01	Enplas Tech Solutions
C17	0	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A104K050BA	TDK
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R17	0	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R19, R20, R21, R22, R23, R24, R25, R26	0	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
  - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductor products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
  - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
  - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
  - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
  - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
  - 3.1 *United States*
    - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
    - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

### CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### FCC Interference Statement for Class A EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

## FCC Interference Statement for Class B EVM devices

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

### Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

### Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。  
[http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page)

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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#### 3.4 *European Union*

##### 3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

#### 4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

##### 4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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- 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.
10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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