DS90LV031A 3-V LVDS Quad CMOS Differential Line Driver

1 Features

- >400-Mbps (200-MHz) Switching Rates
- 0.1-ns Typical Differential Skew
- 0.4-ns Maximum Differential Skew
- 2-ns Maximum Propagation Delay
- 3.3-V Power Supply Design
- ±350-mV Differential Signaling
- Low Power Dissipation (13-mW at 3.3-V Static)
- Interoperable With Existing 5-V LVDS Devices
- Compatible With IEEE 1596.3 SCI LVDS Standard
- Compatible With TIA/EIA-644 LVDS Standard
- Industrial Operating Temperature Range
- Available in SOIC and TSSOP Surface-Mount Packaging

2 Applications

- Building And Factory Automation
- Grid Infrastructure

3 Description

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) using Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage LVTTL or LVCMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

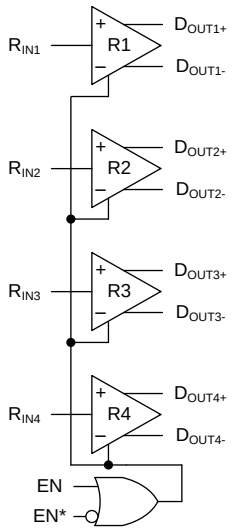
The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90LV031A	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

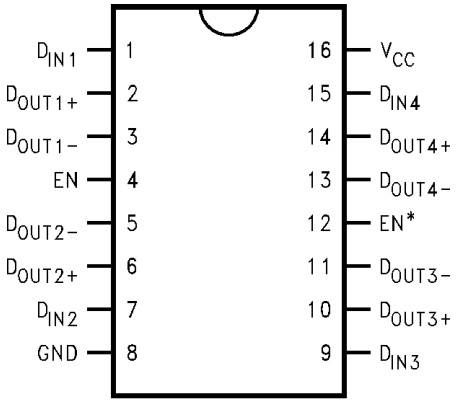
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

5 Pin Configuration and Functions

D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D_{IN}	1, 7, 9, 15	I	Driver input pin, TTL/CMOS compatible
D_{OUT+}	2, 6, 10, 14	O	Noninverting driver output pin, LVDS levels
$D_{OUT–}$	3, 5, 11, 13	O	Inverting driver output pin, LVDS levels
EN	4	I	Active high enable pin, OR-ed with $\overline{EN}$
$\overline{EN}$	12	I	Active low enable pin, OR-ed with EN
GND	8	—	Ground pin
V_{CC}	16	—	Power supply pin, 3.3 V ± 0.3 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.3	4	V
Input voltage, D_{IN}	–0.3	V_{CC} + 0.3	V
Enable input voltage, EN, EN*	–0.3	V_{CC} + 0.3	V
Output voltage, D_{OUT+}, $D_{OUT–}$	–0.3	3.9	V
Short circuit duration, D_{OUT+}, $D_{OUT–}$	Continuous		
Lead temperature, soldering (4 s)		260	°C
Maximum junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±6000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature, industrial	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		DS90LV031A		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114	75	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59	32	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58	31.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over supply voltage and operating temperature ranges (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD1}	Differential output voltage	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)	250	350	450	mV
ΔV_{OD1}	Change in magnitude of V_{OD1} for complementary output states	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)		4	35	|mV|
V_{OS}	Offset voltage	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)	1.125	1.25	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)		5	25	|mV|
V_{OH}	Output voltage high	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)		1.38	1.6	V
V_{OL}	Output voltage low	R_L = 100 Ω, D_{OUT-}, D_{OUT+} pins (see Figure 3)	0.90	1.03		V
V_{IH}	Input voltage high	D_{IN}, EN, EN* pins	2		V_{CC}	V
V_{IL}	Input voltage low	D_{IN}, EN, EN* pins	GND		0.8	V
I_{IH}	Input current high	V_{IN} = V_{CC} or 2.5 V, D_{IN}, EN, EN* pins	−10	±1	10	µA
I_{IL}	Input current low	V_{IN} = GND or 0.4 V, D_{IN}, EN, EN* pins	−10	±1	10	µA
V_{CL}	Input clamp voltage	I_{CL} = −18 mA, D_{IN}, EN, EN* pins	−1.5	−0.8		V
I_{OS}	Output short circuit current	Enabled, D_{OUT-}, D_{OUT+} pins(4), D_{IN} = V_{CC}, D_{OUT+} = 0 V, or D_{IN} = GND, D_{OUT-} = 0 V		−6	−9	mA
I_{OSD}	Differential output short circuit current	Enabled, V_{OD} = 0 V, D_{OUT-}, D_{OUT+} pins(4)		−6	−9	mA
I_{OFF}	Power-off leakage	V_{OUT} = 0 V or 3.6 V, V_{CC} = 0 V or open, D_{OUT-}, D_{OUT+} pins	−20	±1	20	µA
I_{OZ}	Output TRI-STATE current	EN = 0.8 V and EN* = 2 V, V_{OUT} = 0 V or V_{CC}, D_{OUT-}, D_{OUT+} pins	−10	±1	10	µA
I_{CC}	No load supply current drivers enabled	D_{IN} = V_{CC} or GND, V_{CC} pin		5	8	mA
I_{CCL}	Loaded supply current drivers enabled	R_L = 100 Ω (all channels), D_{IN} = V_{CC} or GND (all inputs), V_{CC} pin		23	30	mA
I_{CCZ}	No load supply current drivers disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}, V_{CC} pin		2.6	6	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = 3.3 V, T_A = 25°C.
(3) The DS90LV031A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90 Ω to 110 Ω)
(4) Output short-circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

6.6 Switching Characteristics – Industrial

V_{CC} = 3.3 V ±10% and T_A = –40°C to 85°C (unless otherwise noted)(1)(2)(3)

			MIN	NOM	MAX	UNIT
t_{PHLD}	Differential propagation delay high to low	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0.8	1.18	2	ns
t_{PLHD}	Differential propagation delay low to high	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0.8	1.25	2	ns
t_{SKD1}	Differential pulse skew(4) $\lvert t_{PHLD} - t_{PLHD} \rvert$	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0	0.07	0.4	ns
t_{SKD2}	Channel-to-channel skew(5)	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0	0.1	0.5	ns
t_{SKD3}	Differential part-to-part skew(6)	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0		1	ns
t_{SKD4}	Differential part-to-part skew(7)	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)	0		1.2	ns
t_{TLH}	Rise time	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)		0.38	1.5	ns
t_{THL}	Fall time	R_L = 100 Ω and C_L = 10 pF (see Figure 4 and Figure 5)		0.4	1.5	ns
t_{PHZ}	Disable time high to Z	R_L = 100 Ω and C_L = 10 pF (see Figure 6 and Figure 7)			5	ns
t_{PLZ}	Disable time low to Z	R_L = 100 Ω and C_L = 10 pF (see Figure 6 and Figure 7)			5	ns
t_{PZH}	Enable time Z to high	R_L = 100 Ω and C_L = 10 pF (see Figure 6 and Figure 7)			7	ns
t_{PZL}	Enable time Z to low	R_L = 100 Ω and C_L = 10 pF (see Figure 6 and Figure 7)			7	ns
f_{MAX}	Maximum operating frequency(8)		200	250		MHz

(1) All typicals are given for: V_{CC} = 3.3 V, T_A = 25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.
(3) C_L includes probe and jig capacitance.
(4) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2} is the differential channel-to-channel skew of any event on the same device.
(6) t_{SKD3}, differential part-to-part skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns, (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% / 55%, VOD > 250 mV, all channels switching.

6.7 Dissipation Ratings

	MAXIMUM PACKAGE POWER DISSIPATION AT 25°C
D package	1088 mW
PW package	866 mW
Derate D package	8.5 mW/°C above 25°C
Derate PW package	6.9 mW/°C above 25°C

6.8 Typical Characteristics

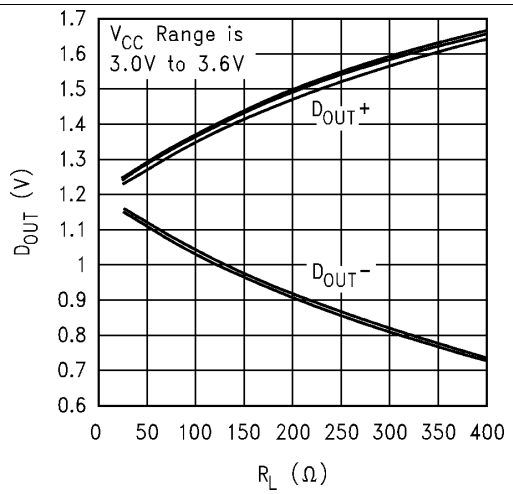


Figure 1. Typical DS90LV031A, D_{OUT} (Single-Ended) vs R_L, T_A = 25°C

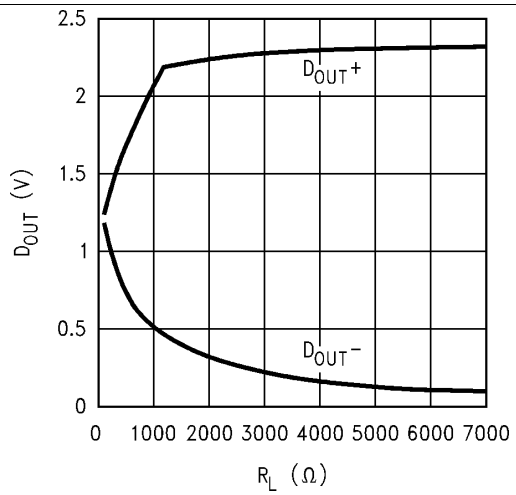


Figure 2. Typical DS90LV031A, D_{OUT} vs R_L, V_{CC} = 3.3 V, T_A = 25°C

7 Parameter Measurement Information

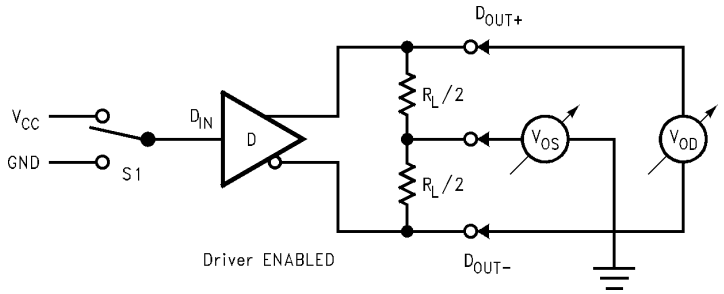


Figure 3. Driver V_{OD} and V_{OS} Test Circuit

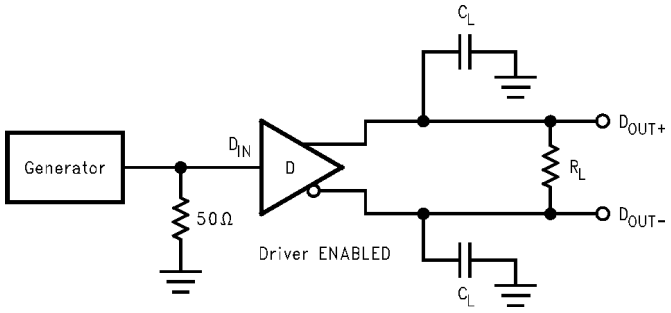


Figure 4. Driver Propagation Delay and Transition Time Test Circuit

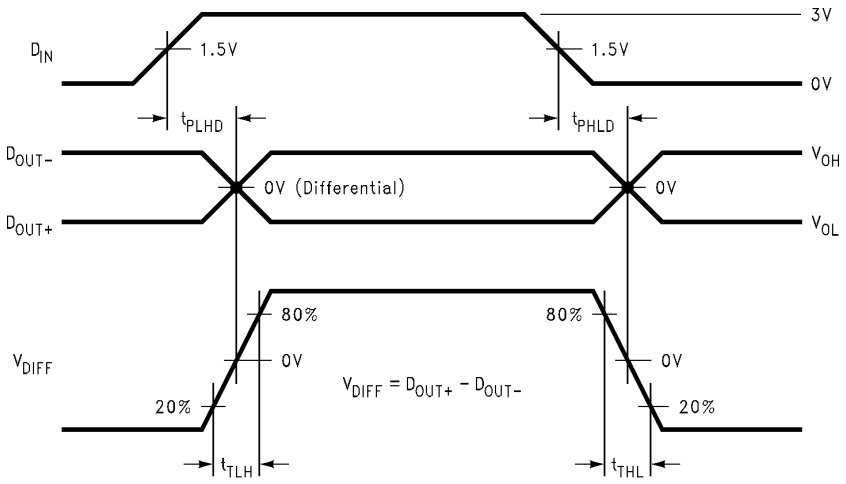


Figure 5. Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (continued)

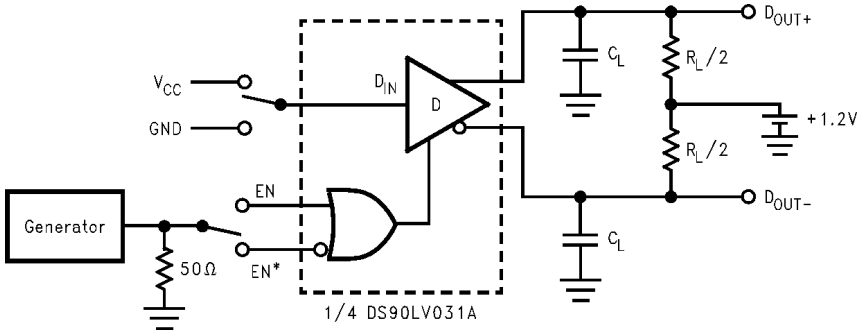


Figure 6. Driver TRI-STATE Delay Test Circuit

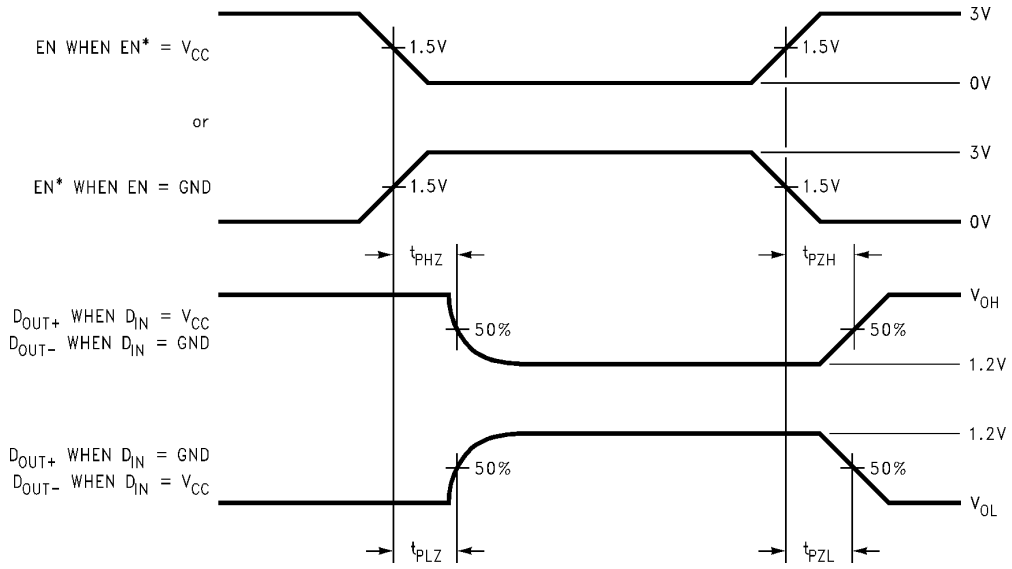


Figure 7. Driver TRI-STATE Delay Waveforms

8 Detailed Description

8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 9. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω must be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

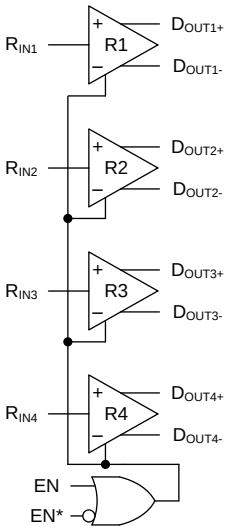
The DS90LV031A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 9. AC or unterminated configurations are not allowed. The 3.5-mA loop current develops a differential voltage of 350 mV across the 100-Ω termination resistor which the receiver detects with a 250-mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 100 mV = 250 mV)). The signal is centered around 1.2 V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 8. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz to 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL or PECL designs. LVDS requires >80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90LV031A is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver and is a step-down replacement for the 5-V DS90C031 Quad Driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fail-Safe LVDS Interface

If the LVDS link as shown in Figure 9 needs to support the case where the Line Driver is disabled, powered off, or removed (unplugged) and the Receiver device is powered on and enabled, the state of the LVDS bus is unknown and therefore the output state of the Receiver is also unknown. If this is of concern, consult the respective LVDS Receiver data sheet for guidance on Fail-safe Biasing options for the LVDS interface to set a known state on the inputs for these conditions.

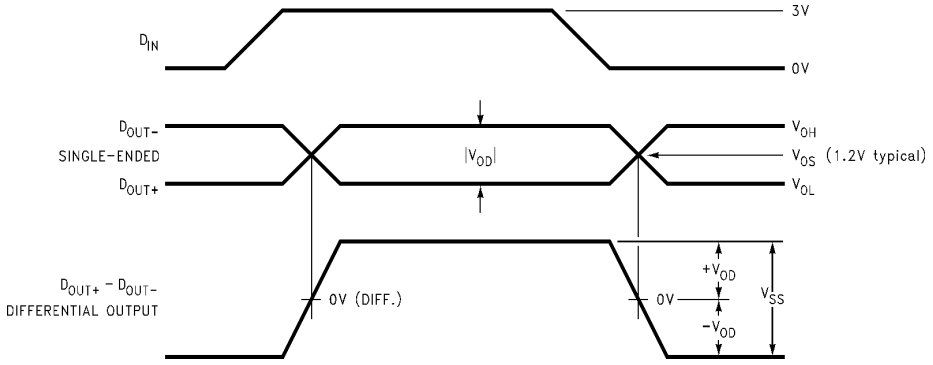


Figure 8. Driver Output Levels

8.4 Device Functional Modes

Table 1 lists the functional modes of DS90LV031A.

Table 1. Truth Table

ENABLES		INPUT	OUTPUTS	
EN	EN*	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90LV031A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

See *Related Documentation* for general application guidelines and hints for LVDS drivers and receivers.

9.2 Typical Application

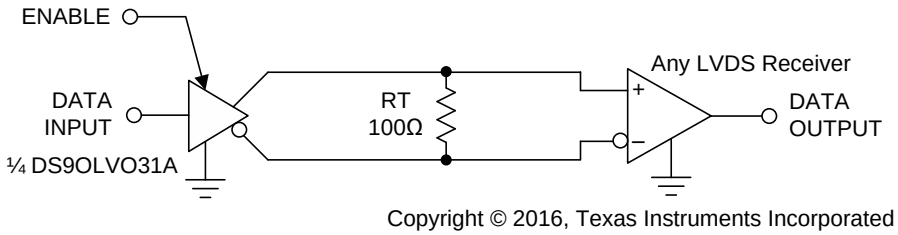


Figure 9. Point-to-Point Application

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

9.2.2 Detailed Design Procedure

9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (>100 kΩ), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.2.2.2 Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (such as ribbon cable or simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5 m, most cables can be made to work effectively. For distances 0.5 m ≤ d ≤ 10 m, Category 3 (CAT 3) twisted pair cable works well, is readily available, and relatively inexpensive.

Typical Application (continued)

9.2.3 Application Curves

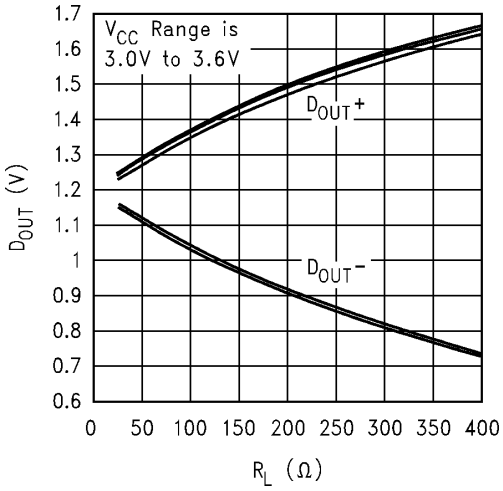


Figure 10. Typical DS90LV031A, D_{OUT} (Single-Ended) vs R_L, T_A = 25°C

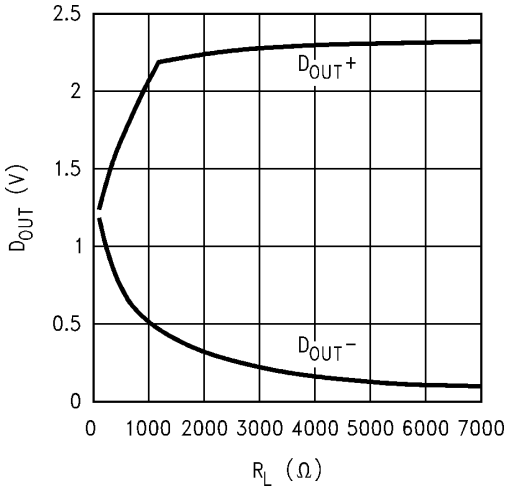


Figure 11. Typical DS90LV031A, D_{OUT} vs R_L, V_{CC} = 3.3 V, T_A = 25°C

10 Power Supply Recommendations

Although the DS90LV031A draws very little power, at higher switching frequencies there is a small dynamic current component which increases the overall power consumption. The DS90LV031A power supply design must include local decoupling capacitance to maintain optimal device performance at higher data rates.

11 Layout

11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom): LVDS signals, ground, power, and TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by power or ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High frequency ceramic (surface-mount recommended) 0.1-µF in parallel with 0.01-µF, in parallel with 0.001-µF at the power supply pin as well as scattered capacitors over the printed-circuit board. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board.

11.1.2 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be < 10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is greater with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and results in EMI. Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces must be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.3 Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface-mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be < 10 mm (12 mm maximum).

11.2 Layout Example

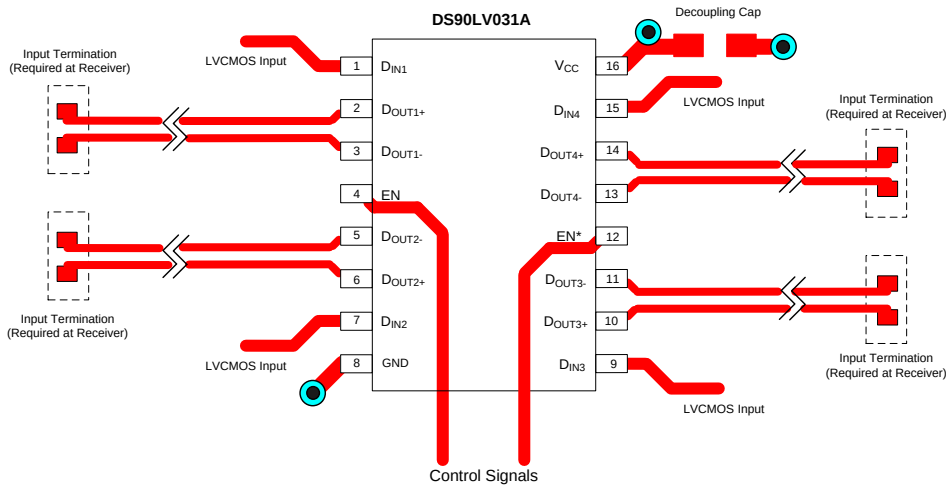


Figure 12. DS90LV031A Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *LVDS Owner's Manual*
- *AN-808 Long Transmission Lines and Data Signal Quality* (SNLA028)
- *AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report #1* (SNLA166)
- *AN-971 An Overview of LVDS Technology* (SNLA165)
- *AN-916 A Practical Guide to Cable Selection* (SNLA219)
- *AN-805 Calculating Power Dissipation for Differential Line Drivers* (SNOA233)
- *AN-903 A Comparison of Differential Termination Techniques* (SNLA034)
- *AN-1035 PCB Design Guidelines for LVDS Technology* (SNOA355)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
TRI-STATE is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV031ATM	NRND	SOIC	D	16	48	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	DS90LV031A TM	
DS90LV031ATM/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV031A TM	Samples
DS90LV031ATMTC	NRND	TSSOP	PW	16	92	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	DS90LV 031AT	
DS90LV031ATMTC/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 031AT	Samples
DS90LV031ATMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 031AT	Samples
DS90LV031ATMX	NRND	SOIC	D	16	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	DS90LV031A TM	
DS90LV031ATMX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 85	DS90LV031A TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

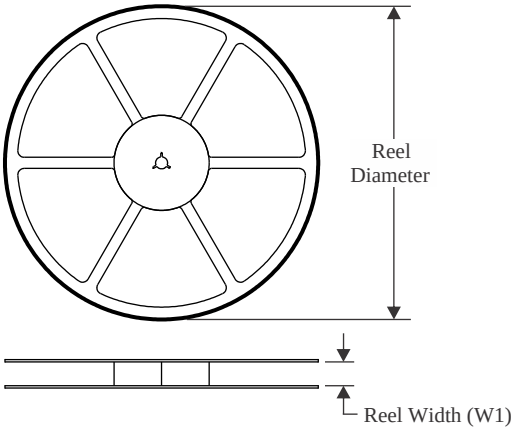
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

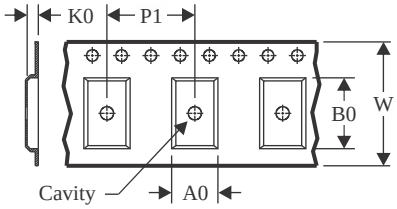
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

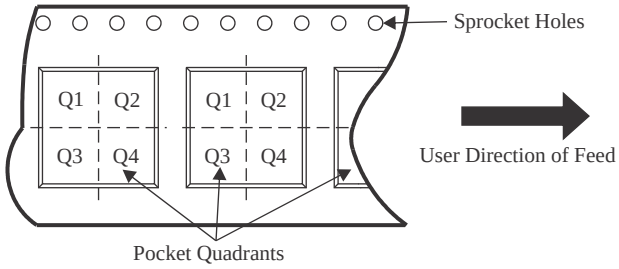


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

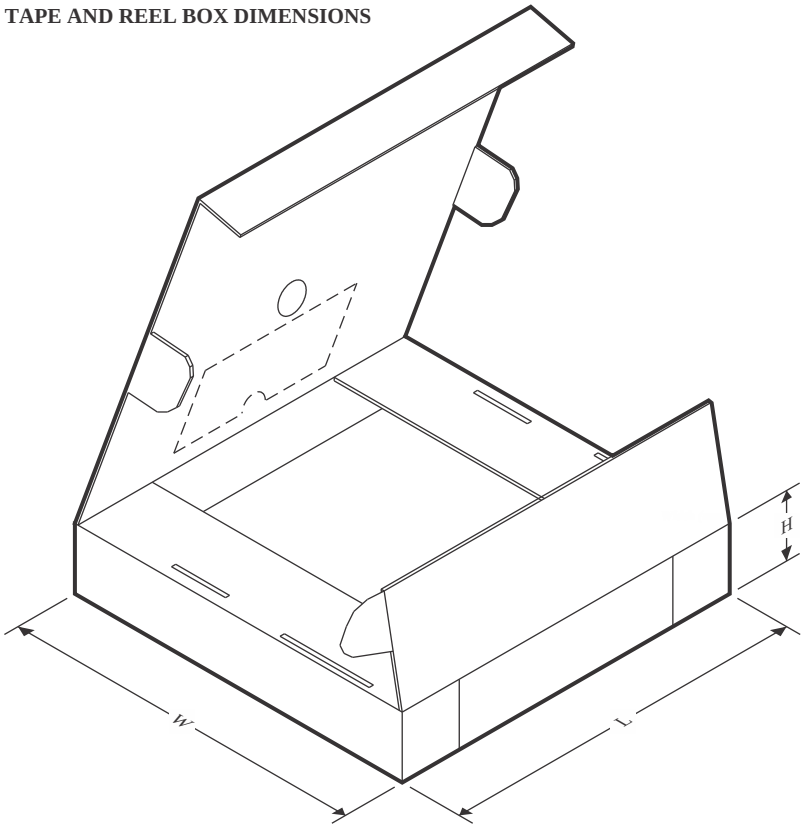
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV031ATMTCX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DS90LV031ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

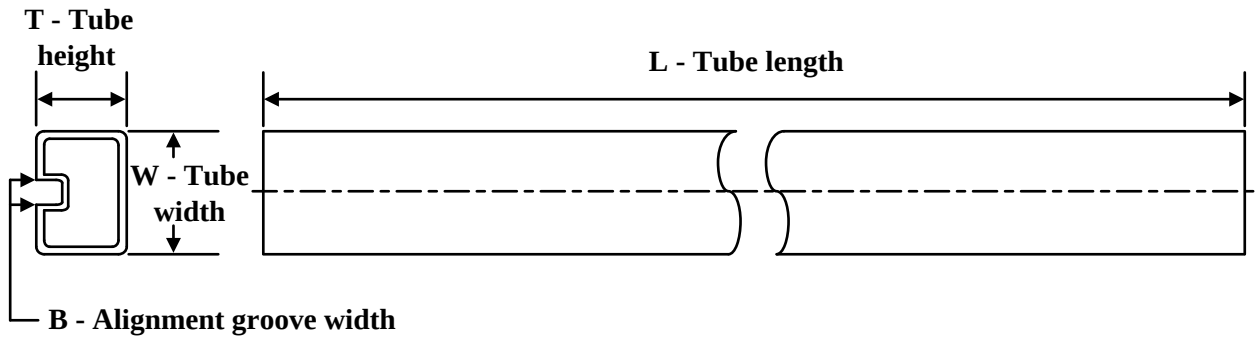
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV031ATMTCX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV031ATMX/NOPB	SOIC	D	16	2500	356.0	356.0	35.0

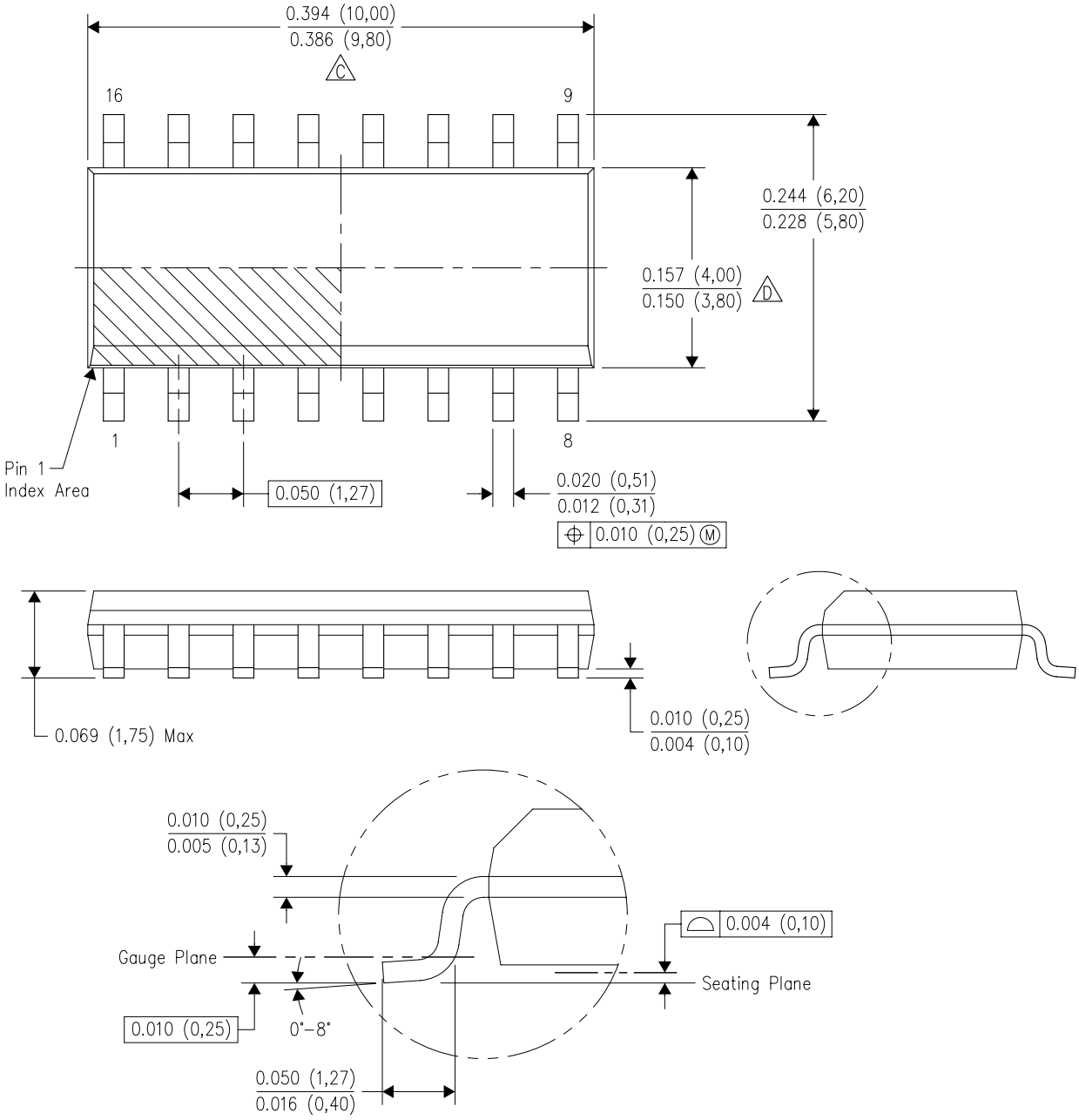
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV031ATM	D	SOIC	16	48	495	8	4064	3.05
DS90LV031ATM	D	SOIC	16	48	495	8	4064	3.05
DS90LV031ATM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DS90LV031ATMTC	PW	TSSOP	16	92	495	8	2514.6	4.06
DS90LV031ATMTC	PW	TSSOP	16	92	495	8	2514.6	4.06
DS90LV031ATMTC/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

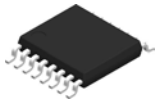
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

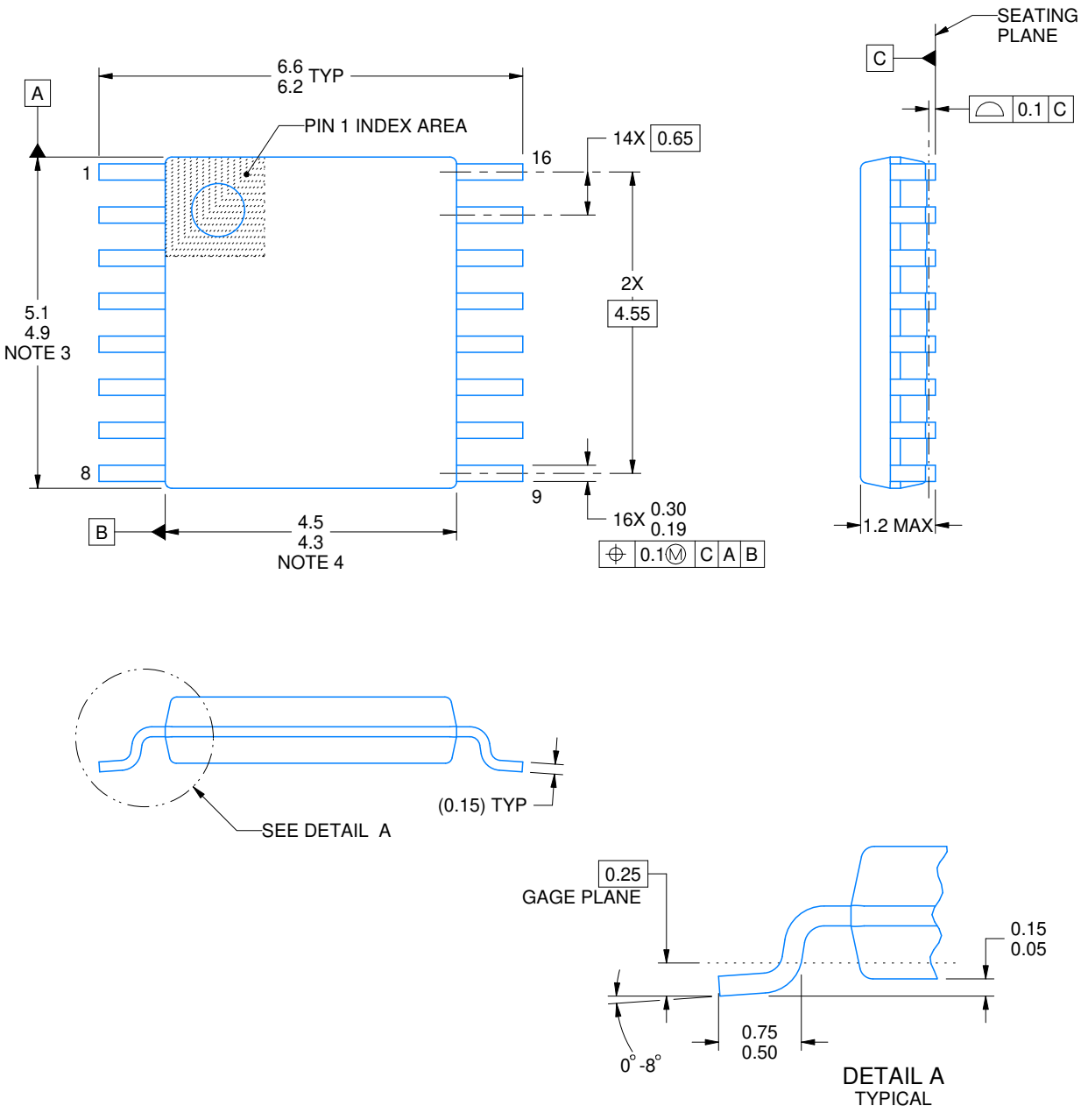
PACKAGE OUTLINE

PW0016A



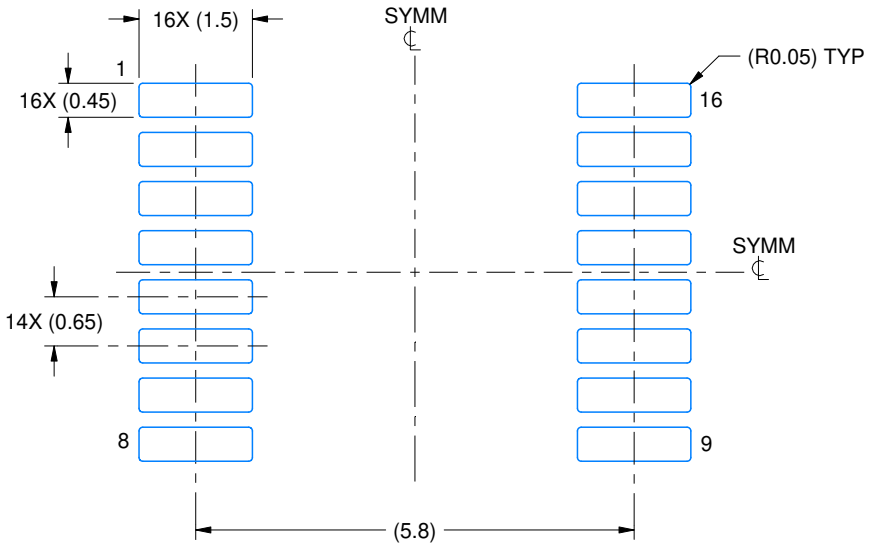
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

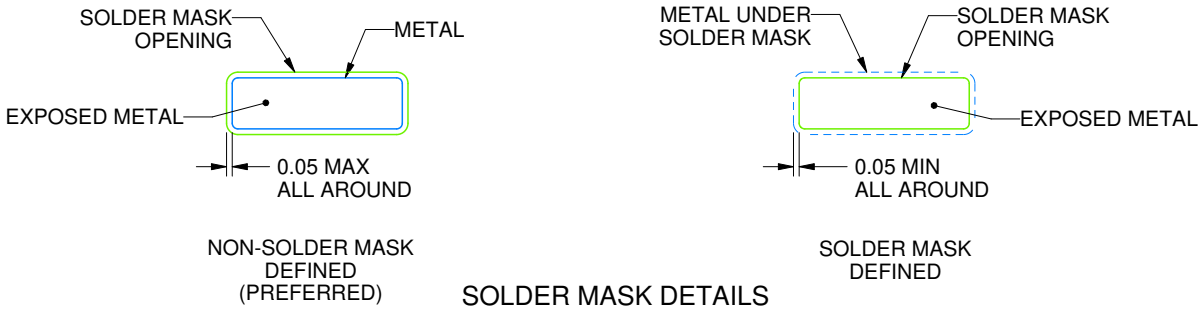


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

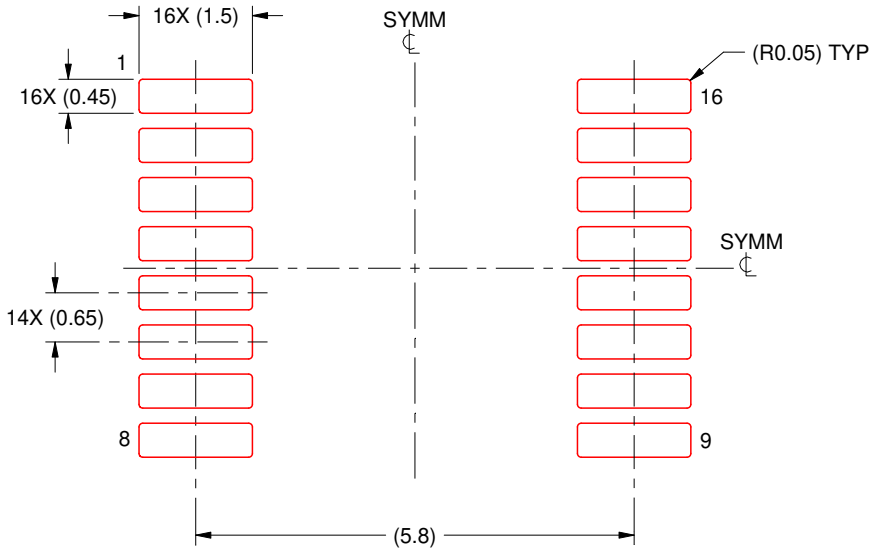


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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