GaAs MMIC LOW NOISE AMPLIFIER, 3.5 - 7.0 GHz

Typical Applications

The HMC392 is ideal for:

- Point-to-Point Radios
- VSAT
- LO Driver for HMC Mixers
- Military EW, ECM, C^3I
- Space

Features

Gain: 15.5 dB

Noise Figure: 2.4 dB

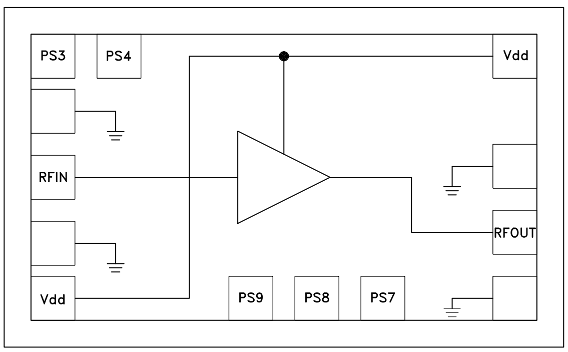
Single Supply Voltage: +5V

50 Ohm Matched Input/Output

No External Components Required

Small Size: 1.3 x 1.0 x 0.1 mm

Functional Diagram



General Description

The HMC392 is a GaAs MMIC Low Noise Amplifier die which operates between 3.5 and 7.0 GHz. The amplifier provides 15.5 dB of gain, 2.4 dB noise figure, and 28 dBm IP3 from a +5V supply voltage. The HMC392 has six bonding adjustment options which allow the user to select the bias point and output power of the device (+15 to +18 dBm). The HMC392 amplifier can easily be integrated into Multi-Chip-Modules (MCMs) due to its small (1.3 mm^2) size. All data is with the chip in a 50 Ohm test fixture connected via 0.025mm (1 mil) diameter wire bonds of minimal length 0.31mm (12 mils).

Electrical Specifications, T_A = +25° C, Vdd = 5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		4.0 - 6.0			3.5 - 7.0		GHz
Gain	13	15.5	19	11.5	14	19	dB
Gain Variation Over Temperature		0.018	0.025		0.018	0.025	dB/ °C
Noise Figure		2.4	3.0		2.8	3.4	dB
Input Return Loss		15			10		dB
Output Return Loss		15			10		dB
Output Power for 1 dB Compression (P1dB)	13	16		12	16		dBm
Saturated Output Power (Psat)		18			18		dBm
Output Third Order Intercept (IP3)	25	28		23	28		dBm
Supply Current (Idd)		50	66		50	66	mA

Note: Data taken with pads PS4 and PS8 bonded to ground (state 5) unless otherwise noted.

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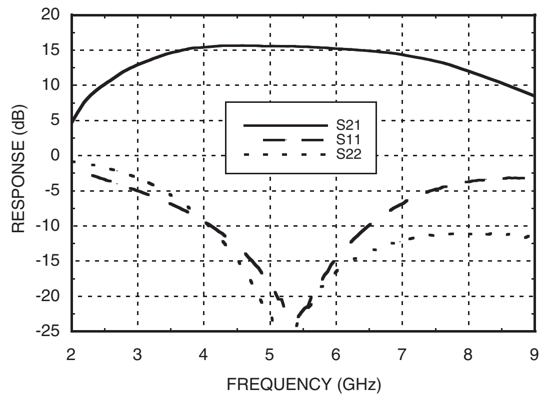
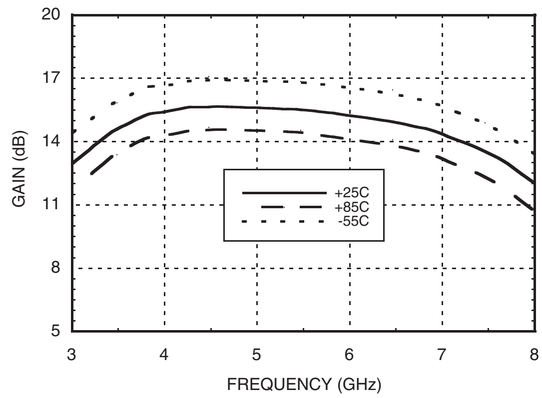
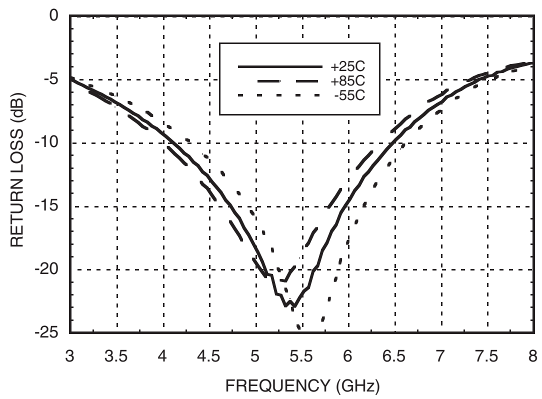
Broadband Gain & Return Loss



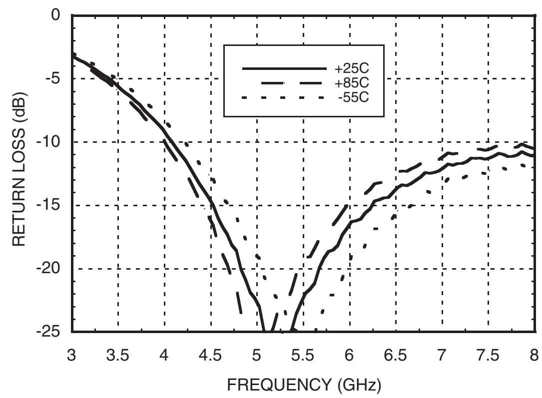
Gain vs. Temperature



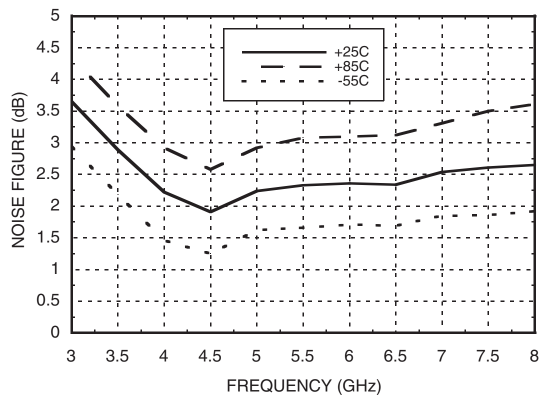
Input Return Loss vs. Temperature



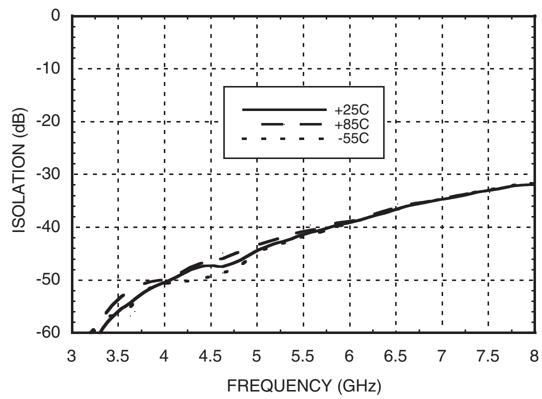
Output Return Loss vs. Temperature



Noise Figure vs. Temperature



Reverse Isolation vs. Temperature



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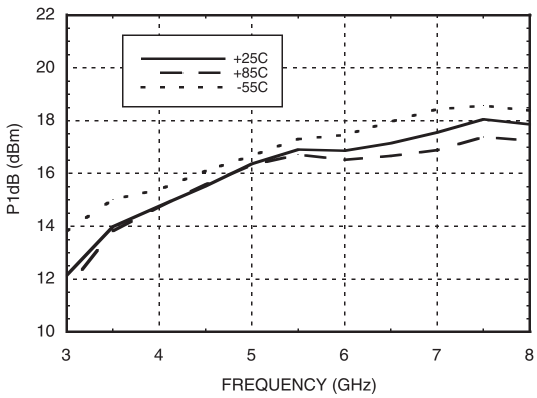
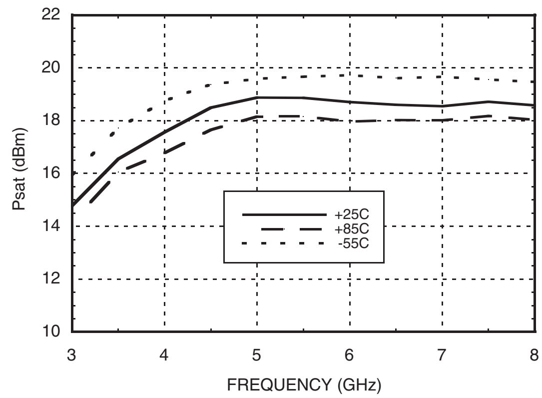
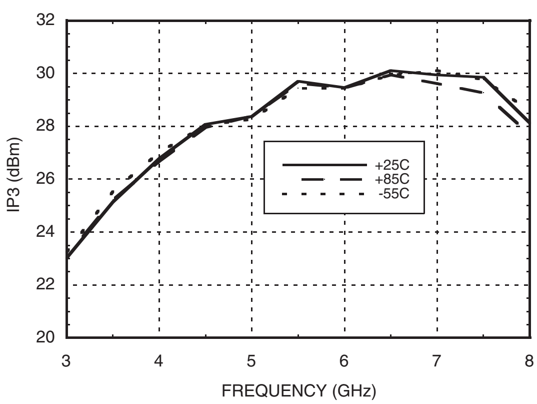
P1dB vs. Temperature



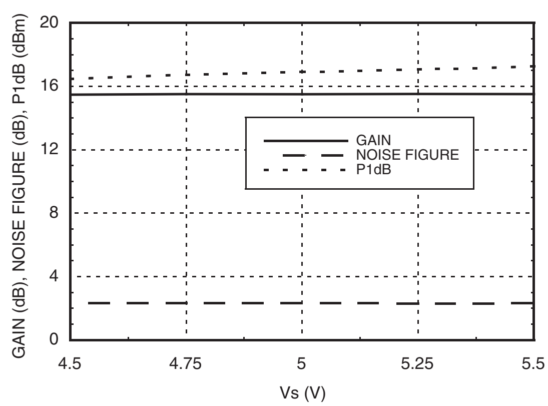
Psat vs. Temperature



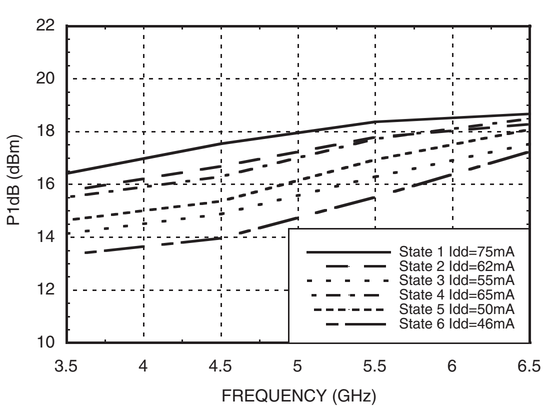
Output IP3 vs. Temperature



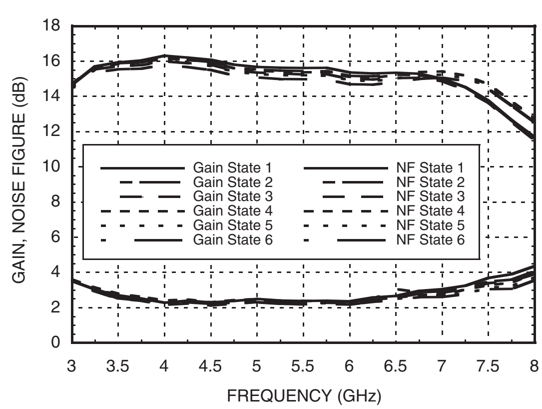
Gain, Noise Figure & Power vs. Supply Voltage @ 5.5 GHz



P1dB vs. Power Select State



Gain & Noise Figure vs. Power Select State



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Absolute Maximum Ratings

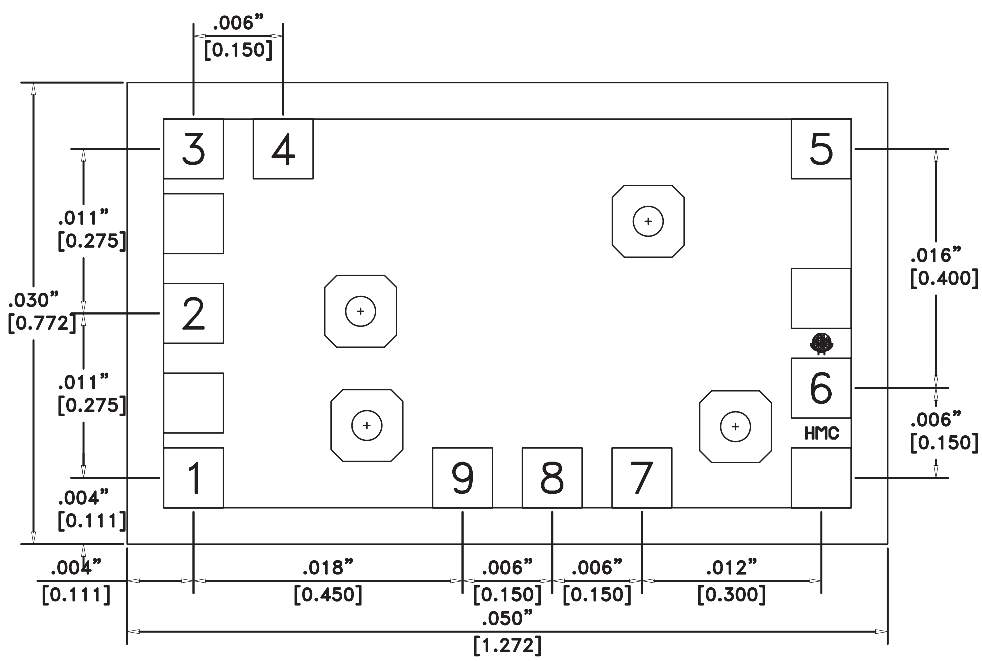
Drain Bias Voltage (Vdd)	7 Vdc
RF Input Power (RFIN)(Vdd = +5 Vdc)	+11 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 7.1 mW/°C above 85 °C)	0.64 W
Thermal Resistance (channel to die bottom)	140 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85° C

Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
+4.5	49
+5.0	50
+5.5	51
(State 5 Depicted)	

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Die Packaging Information [1]

Standard	Alternate
WP-16 (Waffle Pack)	[2]

[1] Refer to the “Packaging Information” section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. ALL TOLERANCES ARE ±0.001 (0.025)
3. DIE THICKNESS IS 0.004 (0.100) BACKSIDE IS GROUND
4. BOND PADS ARE 0.004 (0.100) SQUARE
5. BOND PAD SPACING, CTR-CTR: 0.006 (0.150)
6. BACKSIDE METALLIZATION: GOLD
7. BOND PAD METALLIZATION: GOLD

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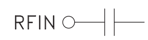
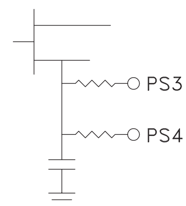
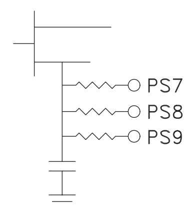
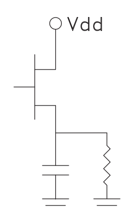
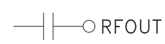
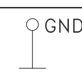
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
2	RFIN	This pad is AC coupled and matched to 50 Ohms	
3 4	Power Select PS3 PS4	One of these pads must be connected to ground. See Power Select Table for selection criteria.	
7 8 9	Power Select PS7 PS8 PS9	One of these pads must be connected to ground. See Power Select Table for selection criteria.	
1, 5	Vdd, Vdd (alt.)	Power supply voltage. Connect either pad1 or pad5 to +5V supply. No choke inductor or bypass capacitor is needed.	
6	RFOUT	This pad is AC coupled and matched to 50 Ohms	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Power Select Table

State	Pads Bonded to Ground	Typical Idd (mA)	Typical P1dB (dBm)
1	PS3 & PS7	75	18.4
2	PS3 & PS8	62	17.9
3	PS3 & PS9	55	16.4
4	PS4 & PS7	65	17.7
5	PS4 & PS8	50	16.9
6	PS4 & PS9	46	15.5

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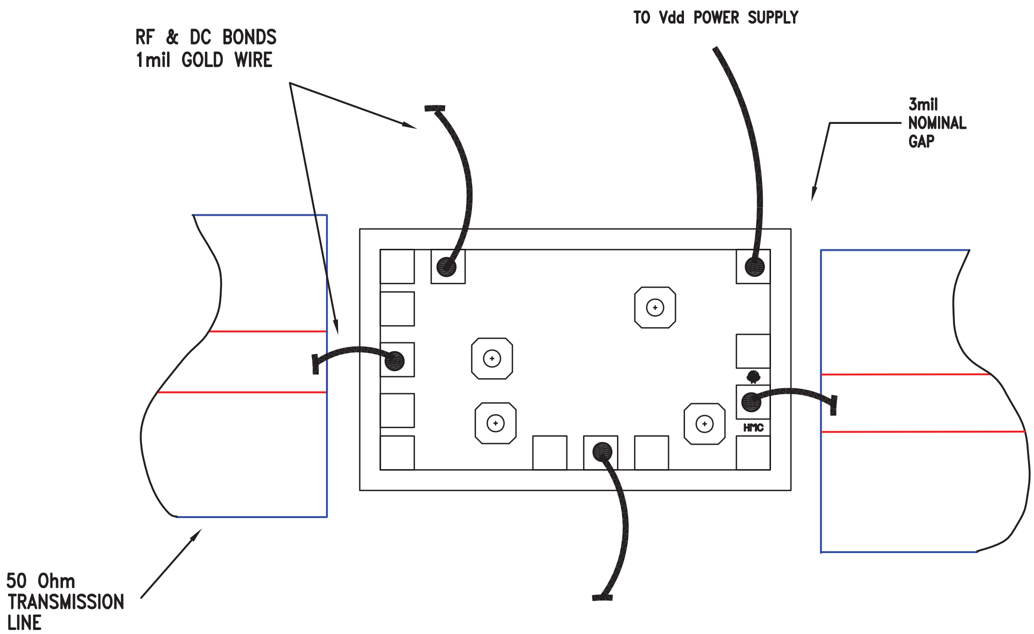
Assembly Diagram



Note: State 5 shown. PS4 and PS8 bonded to ground.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).

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