

# ACPL-M49U

Wide Operating Temperature R<sup>2</sup>Coupler™ 20kBd Digital Optocoupler  
Configurable as Low Power, Low Leakage Phototransistor



## Data Sheet



### Description

The ACPL-M49U is a single channel, high temperature, high CMR, 20kBd digital optocoupler, configurable as a low power, low leakage phototransistor, specifically for use in industrial applications. The SO-5 JEDEC registered (MO-155) package outline is surface mountable.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector in a 5-pin configuration increase the speed up to a hundred times over that of a conventional phototransistor by reducing the base-collector capacitance. Common connections with the supply and output pins shorted in a 4-pin configuration delivers low power, low leakage performance as a phototransistor. The ACPL-M49U has an increased common mode transient immunity of 15kV/μs minimum at  $V_{CM} = 1500V$  over extended temperature range.

Avago R<sup>2</sup>Coupler isolation products provide the reinforced insulation and reliability needed for critical in high temperature industrial applications.

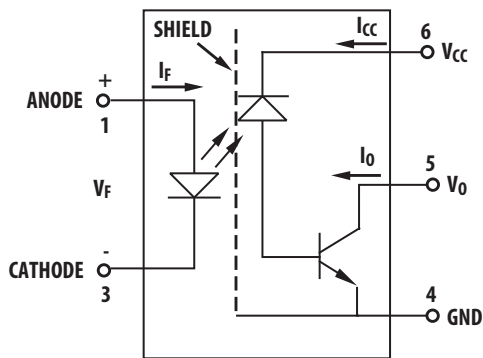
### Features

- High Temperature and Reliable low speed digital interface for Industrial Application.
- 30 kV/μs High Common-Mode Rejection at  $V_{CM} = 1500V$  (typ)
- Low Power, Low Leakage Phototransistor in a 4-Pin Configuration
- Compact, Auto-Insertable SO5 Packages
- Wide Temperature Range: -40°C ~ 125°C
- Low LED Drive Current: 4mA (typ)
- Propagation Delay: 20μs (max)
- Worldwide Safety Approval:
  - UL 1577, 3750  $V_{RMS}$  /1 min.
  - CSA File CA88324, Notice #5
  - IEC/EN/DIN EN 60747-5-5

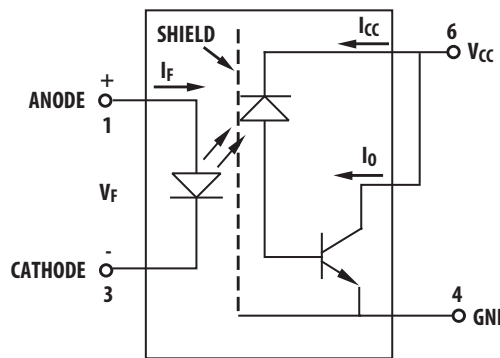
### Applications

- Low Speed Digital Signal isolation Interface
- Inverter fault feedback signal isolation
- Switching Power Supplies feedback circuit

### Functional Diagrams



Note: The connection of a 0.1 μF bypass capacitor between pins 4 and 6 is recommended for 5-pin configuration



Note: Pins 5 and 6 are externally shorted for 4-pin configuration.

LED	Vo
ON	LOW
OFF	HIGH

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Ordering Information

Part Number	Option	Package	Surface Mount	Tape & Reel	Quantity
	(RoHS) Compliant				
ACPL-M49U	-000E	SO-5	X		100 per tube
	-500E		X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

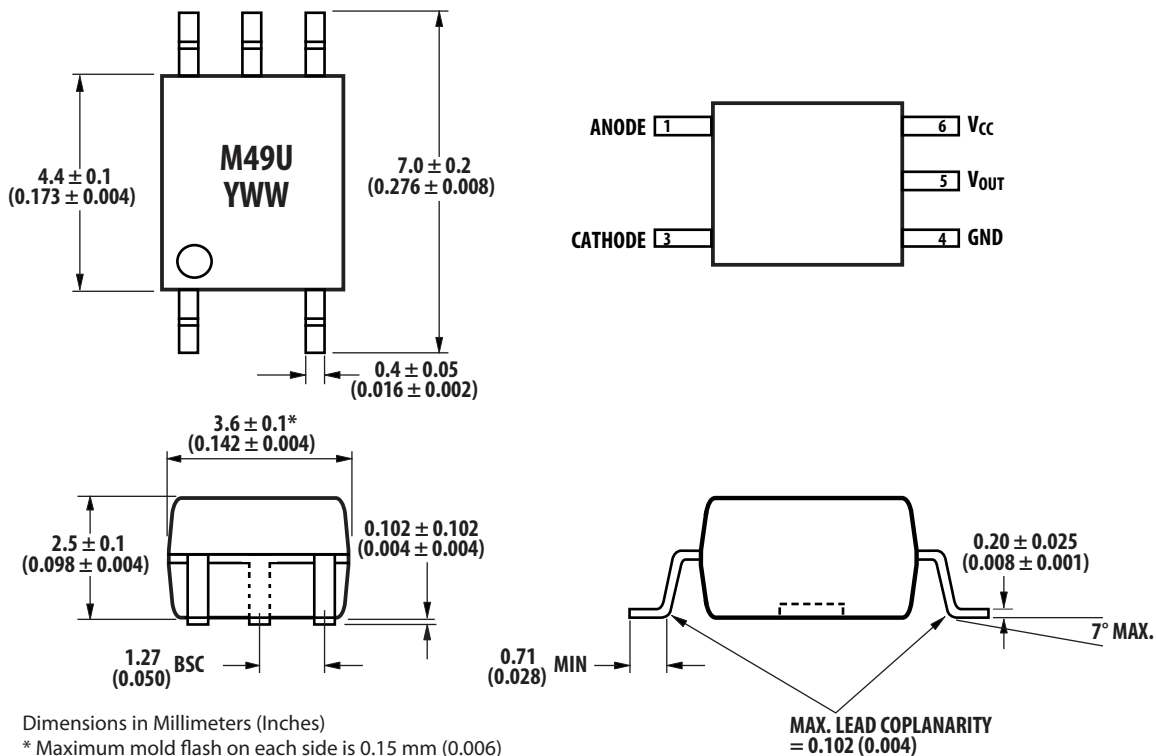
### Example:

ACPL-M49U-500E to order product of Mini-flat Surface Mount 5-pin package in Tape and Reel packaging with RoHS compliant.

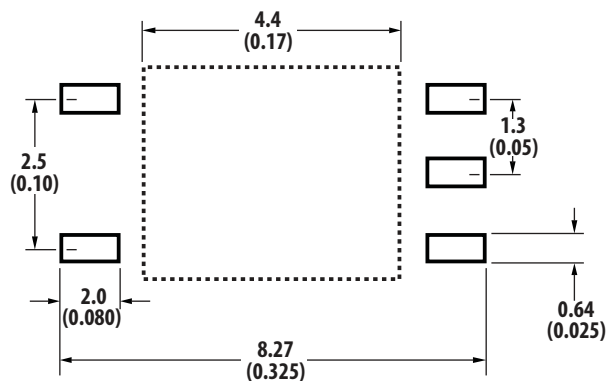
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

### ACPL-M49U Small Outline SO-5 Package (JEDEC MO-155)

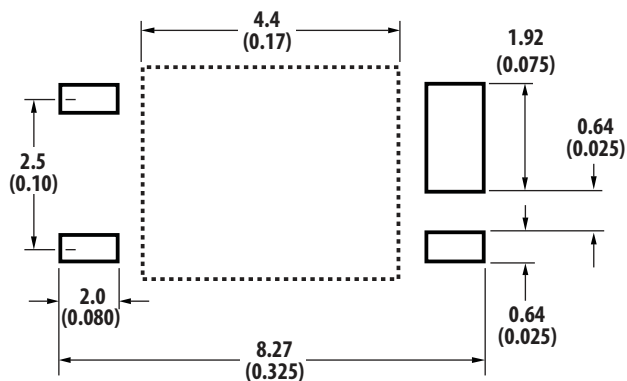


## Land Pattern Recommendation



Dimension in Millimeters (Inches)

## Land Pattern Recommendation (4-pin Configuration)



Dimension in Millimeters (Inches)

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used.

## Regulatory Information

The ACPL-M49U is approved by the following safety regulatory organizations:

### UL

Approved under UL 1577, component recognition program up to  $V_{ISO}=3750 V_{RMS}$

### CSA

Approved under CSA Component Acceptance Notice #5.

### IEC/EN/DIN EN 60747-5-5

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics\*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$		I – IV I – III I – II	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	567	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1063	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	907	$V_{peak}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	$V_{peak}$
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	$T_S$	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

## Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M49U	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	≥ 5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	≥ 5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T <sub>S</sub>	-55	150	°C	
Operating Temperature	T <sub>A</sub>	-40	125	°C	
Lead Soldering Cycle	Temperature		260	°C	
	Time		10	s	
Average Forward Input Current	I <sub>F(avg)</sub>		20	mA	1
Peak Forward Input Current (50% duty cycle, 1ms pulse width)	I <sub>F(peak)</sub>		40	mA	2
Peak Transient Input Current (<=1us pulse width, 300ps)	I <sub>F(trans)</sub>		100	mA	2
Reversed Input Voltage	V <sub>R</sub>		5	V	Pin 3 - 1
Input Power Dissipation	P <sub>IN</sub>		30	mW	3
Output Power Dissipation	P <sub>O</sub>		100	mW	4
Average Output Current	I <sub>O</sub>		8	mA	
Peak Output Current	I <sub>O(pk)</sub>		16	mA	
Supply Voltage (Pins 6-4)	V <sub>CC</sub>	-0.5	30	V	
Output Voltage (Pins 5-4)	V <sub>O</sub>	-0.5	20	V	
Solder Reflow Temperature Profile					See Reflow Temperature Profile

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V <sub>CC</sub>		20.0	V	
Operating Temperature	T <sub>A</sub>	-40	125	°C	

## Electrical Specifications (DC) for 5-Pin Configuration

Over recommended operating  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Current Transfer Ratio	CTR	32	45	80	%	$T_A=25^{\circ}\text{C}$ $V_O=0.4\text{V}$ $V_{CC}=4.5\text{V}$	1, 2	5
		20	45	$V_O=0.5\text{V}$ $I_F=10\text{mA}$				
			58			$T_A=25^{\circ}\text{C}$ $V_O=0.5\text{V}$ $V_{CC}=4.5\text{V}$	1, 2	
Logic Low Output Voltage	$V_{OL}$		0.1	0.4	V	$T_A=25^{\circ}\text{C}$ $I_O=3\text{mA}$ $V_{CC}=4.5\text{V}$	3	
				0.5		$I_O=2.4\text{mA}$ $I_F=10\text{mA}$		
Logic High Output Current	$I_{OH}$		0.003	0.5	$\mu\text{A}$	$T_A=25^{\circ}\text{C}$ $V_O=V_{CC}=5.5\text{V}$ $I_F=0\text{mA}$	7	
			0.01	1		$T_A=25^{\circ}\text{C}$ $V_O=V_{CC}=15\text{V}$		
				5				
Logic Low Supply Current	$I_{CCL}$		50	200		$I_F=10\text{mA}$ , $V_O=\text{open}$ , $V_{CC}=15\text{V}$		
Logic High Supply Current	$I_{CCH}$		0.02	1		$T_A=25^{\circ}\text{C}$ $I_F=0\text{mA}$ , $V_O=\text{open}$ , $V_{CC}=15\text{V}$		
Input Forward Voltage	$V_F$	1.45	1.5	1.75	V	$I_F=10\text{mA}$ , $T_A=25^{\circ}\text{C}$	5	
		1.25	1.5	1.85		$I_F=10\text{mA}$ , $T_A=\text{Across Temperature}$		
			1.5			$I_F=4\text{mA}$ , $T_A=25^{\circ}\text{C}$		
Input Reversed Breakdown Voltage	$BV_R$	5				$I_R=10\mu\text{A}$		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		$\text{mV}/^{\circ}\text{C}$	$I_F=10\text{mA}$		
Input Capacitance	$C_{IN}$		90		$\text{pF}$	$F=1\text{MHz}$ , $V_F=0$		

## Switching Specifications (AC) for 5-Pin Configuration

Over recommended operating ( $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{CC} = 5.0\text{V}$  unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	$t_{PHL}$	-	-	20	$\mu\text{s}$	Pulse: $f=10\text{kHz}$ , Duty cycle = 50%, $I_F=4\text{mA}$ , $V_{CC}=5.0\text{V}$ , $R_L=8.2\text{k}\Omega$ , $C_L=15\text{pF}$ $V_{THHL}=1.5\text{V}$	9	
Propagation Delay Time to Logic High at Output	$t_{PLH}$	-	-	20	$\mu\text{s}$	Pulse: $f=10\text{kHz}$ , Duty cycle = 50%, $I_F=4\text{mA}$ , $V_{CC}=5.0\text{V}$ , $R_L=8.2\text{k}\Omega$ , $C_L=15\text{pF}$ $V_{THLH}=2.0\text{V}$	9	
Common Mode Transient Immunity at Logic High Output	$ CM_H $	15	30		$\text{kV}/\mu\text{s}$	$I_F=0\text{mA}$ $V_{CM}=1500\text{V}_{p-p}$ $T_A=25^{\circ}\text{C}$ $R_L=8.2\text{k}\Omega$	10	9
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	15	30		$\text{kV}/\mu\text{s}$	$I_F=10\text{mA}$ $V_{CM}=1500\text{V}_{p-p}$ $T_A=25^{\circ}\text{C}$ $R_L=8.2\text{k}\Omega$		
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	-	15		$\text{kV}/\mu\text{s}$	$I_F=4\text{mA}$ $V_{CM}=1500\text{V}_{p-p}$ $T_A=25^{\circ}\text{C}$ $R_L=8.2\text{k}\Omega$		

## Electrical Specifications (DC) for 4-Pin Configuration

Applicable for  $V_{CC} = V_O$ . Over recommended operating  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Current Transfer Ratio	CTR		120		%	$T_A=25^\circ\text{C}$ , $I_F=5\text{mA}$ , $V_{CC}=V_O=5\text{V}$	4	5, 8
Current Transfer Ratio	CTR (Sat)	20	45		%	$I_F=10\text{mA}$ $V_{CC}=V_O=0.5\text{V}$	5	5, 8
			58			$I_F=4\text{mA}$		
Logic Low Output Voltage	$V_{OL}$		0.1	0.4	V	$T_A=25^\circ\text{C}$ $I_O=3\text{mA}$ $I_F=10\text{mA}$	5	8
				0.5		$I_O=2.4\text{mA}$		
Off-State Current	$I_{(CEO)}$		0.0001	5	$\mu\text{A}$	$V_O=V_{CC}=15\text{V}$ , $I_F=0\text{mA}$	8	8
Input Forward Voltage	$V_F$	1.45	1.5	1.75	V	$I_F=10\text{mA}$ , $T_A=25^\circ\text{C}$	6	
		1.25	1.5	1.85		$I_F=10\text{mA}$ , $T_A=$ Across Temperature		
			1.45			$I_F=4\text{mA}$ , $T_A=25^\circ\text{C}$		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		$\text{mV}/^\circ\text{C}$	$I_F=10\text{mA}$		
Input Reversed Breakdown Voltage	$BV_R$	5				$I_R=10\mu\text{A}$		
Input Capacitance	$C_{IN}$		90		pF	$F=1\text{MHz}$ , $V_F=0$		
Output Capacitance	$C_{CE}$		35		pF	$F=1\text{MHz}$ , $V_F=0$ , $V_O=V_{CC}=0\text{V}$		8

## Switching Specifications (AC) for 4-Pin Configuration

Over recommended operating ( $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{CC} = 5.0\text{V}$  unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	$t_{PHL}$	-	2	100	$\mu\text{s}$	Pulse: $f=1\text{kHz}$ , Duty cycle = 50%, $I_F=4\text{mA}$ , $V_{CC}=5.0\text{V}$ , $R_L=8.2\text{k}\Omega$ , $C_L=15\text{pF}$ $V_{THHL}=1.5\text{V}$	10	8
Propagation Delay Time to Logic High at Output	$t_{PLH}$	-	19	100	$\mu\text{s}$	Pulse: $f=1\text{kHz}$ , Duty cycle = 50%, $I_F=4\text{mA}$ , $V_{CC}=5.0\text{V}$ , $R_L=8.2\text{k}\Omega$ , $C_L=15\text{pF}$ $V_{THLH}=2.0\text{V}$	10	8
Common Mode Transient Immunity at Logic High Output	$ CM_H $	15	30		$\text{kV}/\mu\text{s}$	$I_F=0\text{mA}$ $V_{CM}=1500\text{V}_{p-p}$ $T_A=25^\circ\text{C}$ $R_L=8.2\text{k}\Omega$	12	8, 9
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	15	30		$\text{kV}/\mu\text{s}$	$I_F=4\text{mA}$ $V_{CM}=1500\text{V}_{p-p}$ $T_A=25^\circ\text{C}$ $R_L=8.2\text{k}\Omega$		

## Package Characteristics

\*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	3750			$V_{RMS}$	$RH \leq 50\%$ , $t = 1 \text{ min}$ ; $T_A = 25^\circ\text{C}$		6, 7
Input-Output Resistance	$R_{I-O}$		$10^{14}$		$\Omega$	$V_{I-O} = 500 V_{DC}$		6
Input-Output Capacitance	$C_{I-O}$		0.6		pF	$f = 1 \text{ MHz}$ ; $V_{I-O} = 0 V_{DC}$		6

Notes:

1. Derate linearly above 85°C free-air temperature at a rate of 0.25mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 0.30mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 0.375mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 1.875mW/°C.
5. Current Transfer Ratio in percent is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100.
6. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4,5, and 6 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 4800V_{RMS}$  for 1 second.
8. This is in a 4-pin configuration where the  $V_{CC}$  and  $V_O$  pin are shorted together.
9. Common transient immunity in a Logic High level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the rising edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 2.0V$ ). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the falling edge of the common mode pulse signal,  $V_{CM}$  to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 0.8V$ ).

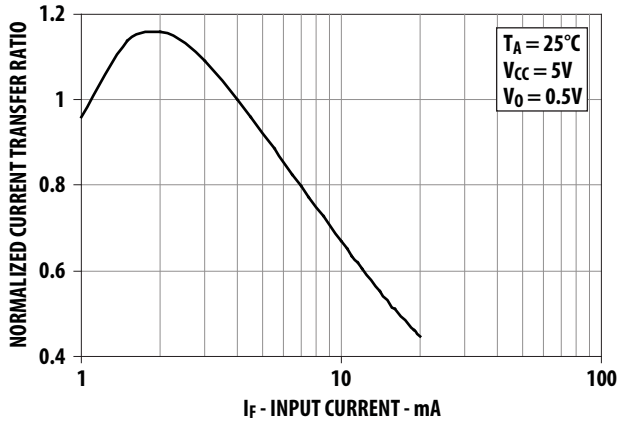


Figure 1. Normalized Current Transfer Ratio ( $I_F = 4\text{mA}$  as reference) vs Input Current

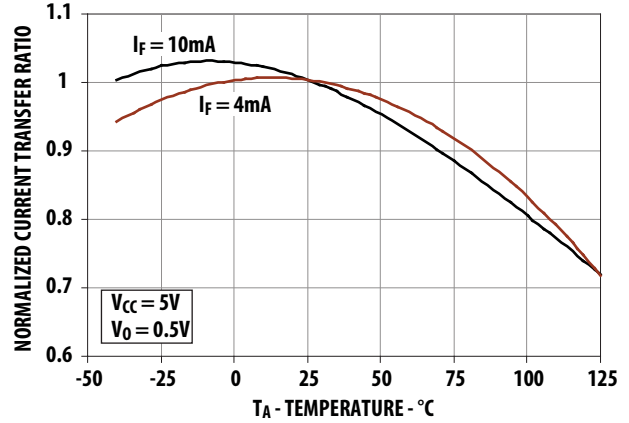


Figure 2. Normalized Current Transfer Ratio ( $T_A = 25^\circ\text{C}$  as reference) vs Temperature

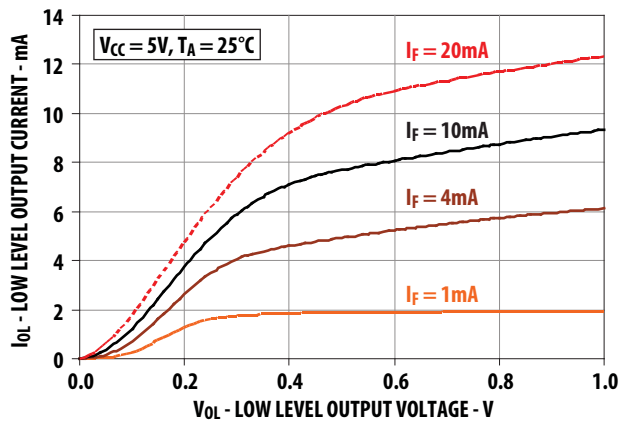


Figure 3. Typical Low Level Output Current vs Output Voltage

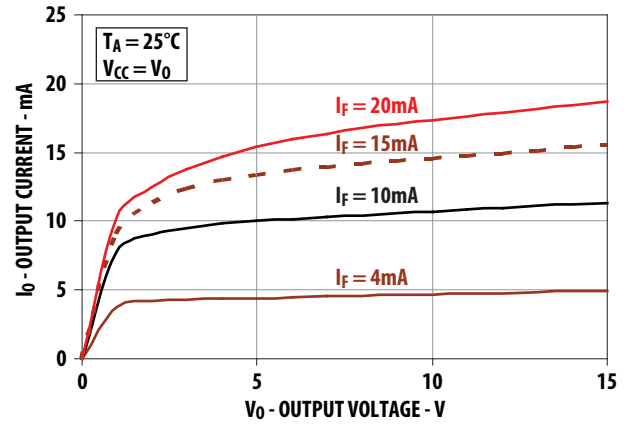


Figure 4. Output Current vs Output Voltage (4-Pin Configuration)

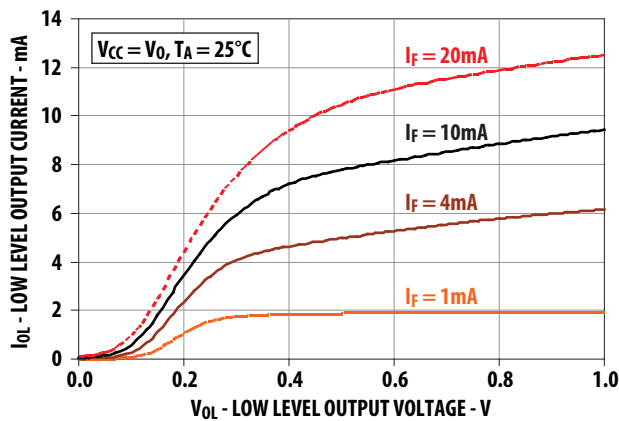


Figure 5. Typical Low Level Output Current vs Output Voltage (4-Pin Configuration)

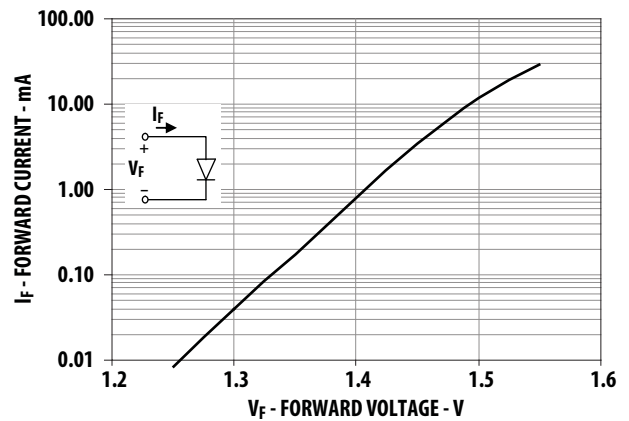


Figure 6. Typical Input Current vs Forward Voltage



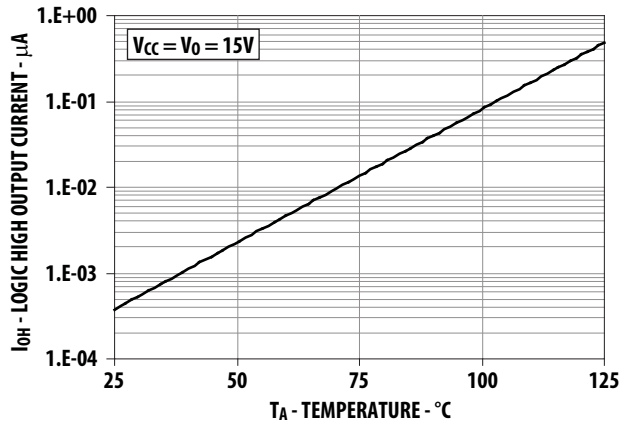


Figure 7. Typical High Level Output Current vs Temperature

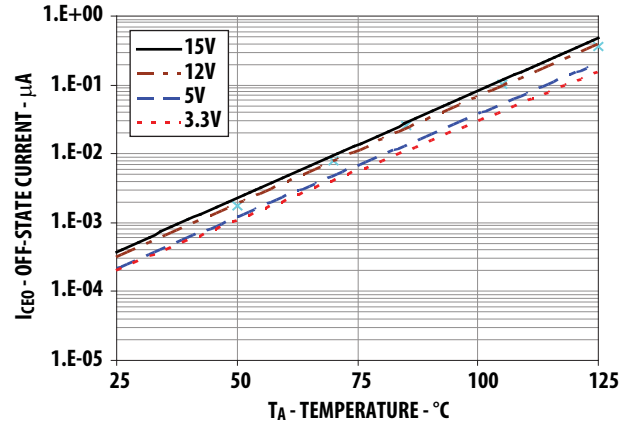


Figure 8. Typical Off-State Current vs Temperature (4-Pin Configuration)

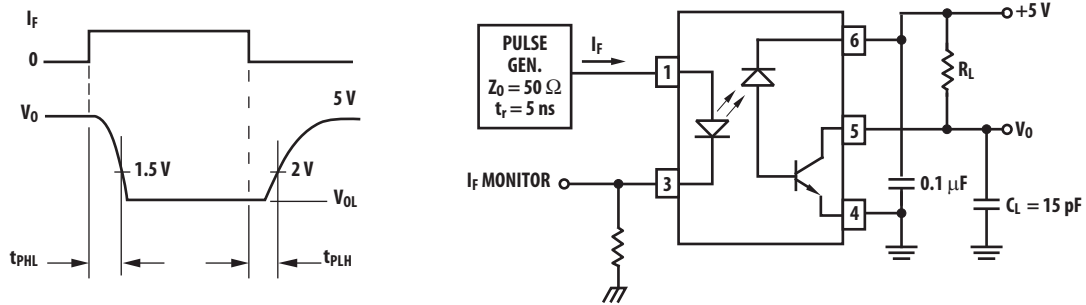


Figure 9. Switching Test Circuit

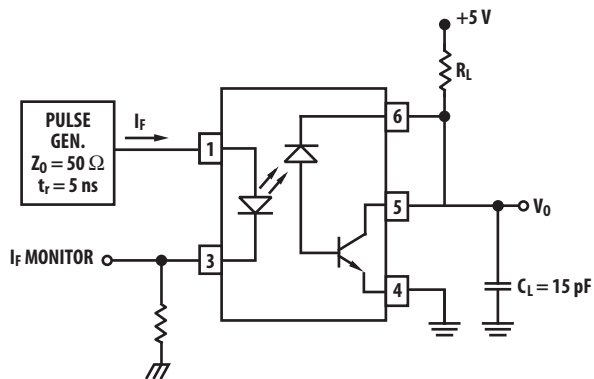


Figure 10. Switching Test Circuit (4-pin configuration)

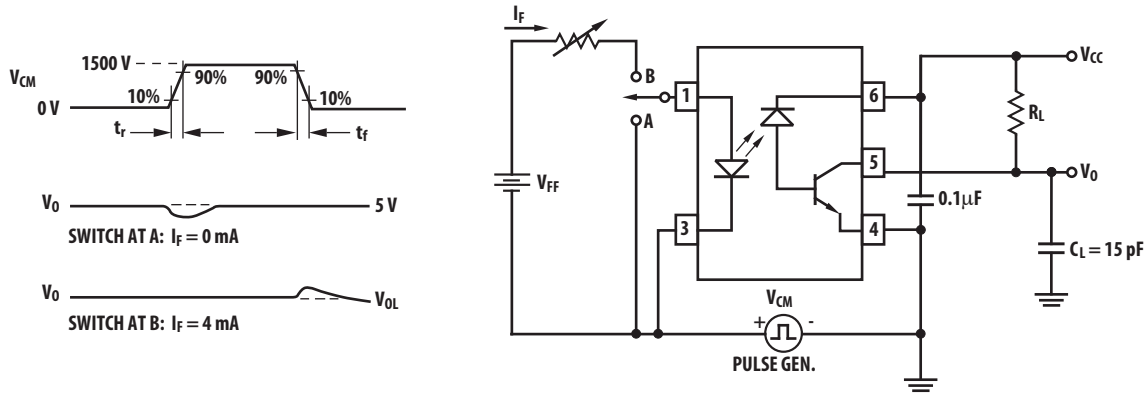


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms

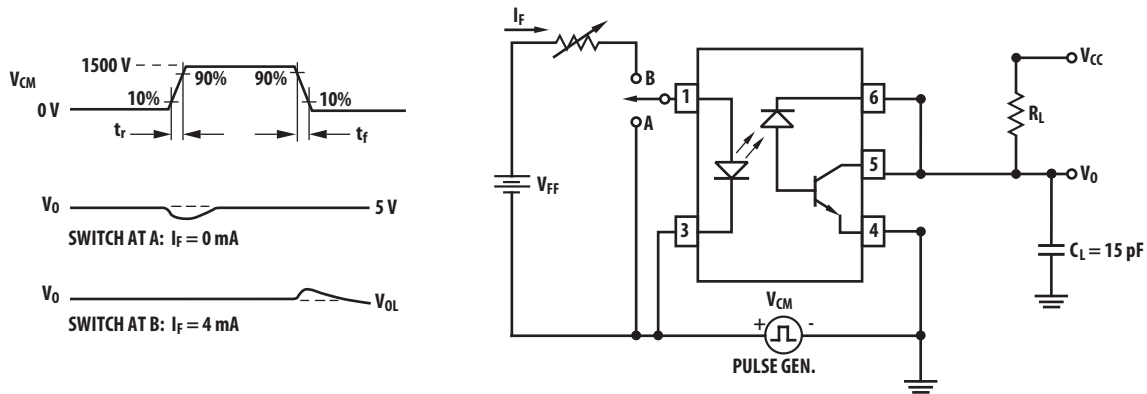


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms (4-Pin Configuration)

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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