MAX14653/MAX14654/ MAX14655/MAX14717

High-Current Overvoltage Protectors with Adjustable OVLO

General Description

The MAX14653/MAX14654/MAX14655/MAX14717 overvoltage protection devices feature a low 38mΩ (typ) R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +80V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the MAX14653/MAX14654/MAX14655/MAX14717 automatically choose the accurate internal trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 15.5V typical (MAX14653), 6.8V typical (MAX14654/MAX14717), or 5.825V typical (MAX14655). The devices feature an open-drain $\overline{ACOK}$ output indicating a stable supply between minimum supply voltage and V_{OVLO}. The MAX14653/MAX14654/MAX14655/MAX14717 are also protected against overcurrent events by an internal thermal shutdown.

The MAX14653/MAX14654/MAX14655/MAX14717 are offered in a small 12-bump WLP package and operate over the -40ºC to +85ºC extended temperature range.

Applications

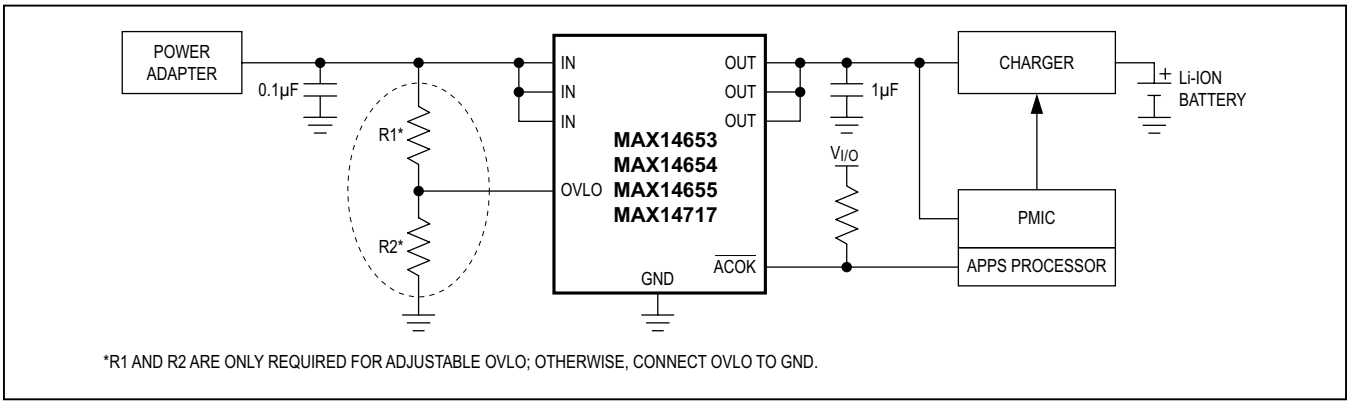
- Smartphones
- Tablet PCs
- Mobile Internet Devices

Benefits and Features

- Protect High-Power Portable Devices
  - Wide Operating Input Voltage Protection from +2.5V to +28V
  - Integrated 38mΩ (typ) n-Channel MOSFET Switch
- Flexible Overvoltage Protection Design
  - Adjustable Overvoltage Protection Trip Level
  - Wide Adjustable OVLO Threshold Range from +4V to +20V
  - Preset Internal Accurate OVLO Thresholds:
    - 15.5V ±3.3% (MAX14653)
    - 6.8V ±2.9% (MAX14654/MAX14717)
    - 5.825V ±3% (MAX14655)
- Additional Protection Features Increase System Reliability
  - Surge Immunity to +80V
  - Soft-Start to Minimize In-Rush Current
  - Internal 15ms Startup Debounce
  - Thermal-Shutdown Protection
- Minimize PCB Area
  - 12-Bump WLP (1.29mm x 1.83mm) Package
- -40ºC to +85ºC Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



*R1 AND R2 ARE ONLY REQUIRED FOR ADJUSTABLE OVLO; OTHERWISE, CONNECT OVLO TO GND.

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Absolute Maximum Ratings

(All voltages referenced to GND.)
IN (Note 1).....-0.3V to +29V
OUT.....-0.3V to V_{IN} + 0.3V
OVLO.....-0.3V to +24V
$\overline{ACOK}$.....-0.3V to +6V
Continuous IN, OUT Current.....4.5A
(**Note:** Continuous current limited by thermal design.)

Peak IN, OUT Current (10ms).....8A
Continuous Power Dissipation (T_A = +70ºC)
WLP (derate 13.7mW/ºC above +70ºC).....1096mW
Operating Temperature Range.....-40ºC to +85ºC
Junction Temperature.....+150ºC
Storage Temperature Range.....-65ºC to +150ºC
Soldering Temperature (reflow).....+260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....73°C/W

Note 1: Survives burst pulse up to 80V with 2Ω series resistance.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +2.5V to +28V, C_{IN} = 0.1µF, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{IN} = +5.0V, I_{IN} ≤ 3A, and T_A = +25ºC.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.5		28	V
Input Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 10mA, T_A = +25ºC			33		V
Input Supply Current	I_{IN}	V_{IN} = 5V			70	120	µA
OVLO Supply Current	I_{IN_Q}	V_{OVLO} = 3V, V_{IN} = 5V, V_{OUT} = 0V			63	120	µA
Internal Overvoltage Trip Level	V_{IN_OVLO}	V_{IN} rising	MAX14653	15	15.5	16	V
			MAX14654/ MAX14717	6.6	6.8	7.0	
			MAX14655	5.65	5.825	6.00	
		V_{IN} falling	MAX14653	14.5			
			MAX14654/ MAX14717	6.5			
			MAX14655	5.55			
OVLO Set Threshold	V_{OVLO_TH}	MAX14653		1.22	1.26	1.30	V
		MAX14654, MAX14655, MAX14717		1.18	1.22	1.26	
Adjustable OVLO Threshold Range				4		20	V
External OVLO Select Threshold	V_{OVLO_SELECT}			0.2		0.3	V
Switch On-Resistance	R_{ON}	V_{IN} = 5V, I_{OUT} = 1A, T_A = +25ºC			38	53	mΩ
OUT Load Capacitance	C_{OUT}	V_{IN} = 5V				1000	µF
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO} = V_{OVLO_TH}		-100		100	nA

Electrical Characteristics (continued)

(V_{IN} = +2.5V to +28V, C_{IN} = 0.1µF, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{IN} = +5.0V, I_{IN} ≤ 3A, and T_A = +25ºC.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Leakage Voltage by OVLO	V_{IN_LEAK}	V_{OVLO} = 20V, V_{IN} = unconnected, R_{OVLO} = 1MΩ			0.5	V
Thermal Shutdown				130		ºC
Thermal-Shutdown Hysteresis				20		ºC
DIGITAL SIGNALS ($\overline{ACOK}$)						
$\overline{ACOK}$ Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA, see the *Typical Application Circuit*			0.4	V
$\overline{ACOK}$ Leakage Current	V_{ACOK_LEAK}	$V_{I/O}$ = 3.3V, $\overline{ACOK}$ deasserted, see the *Typical Application Circuit*	-1		+1	µA
TIMING CHARACTERISTICS (Figure 1)						
Debounce Time MAX14653/ MAX14654/MAX14655	t_{DEB}	Time from 2.5V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 10% of V_{IN}		15		ms
Debounce Time MAX14717	t_{DEB}	Time from 2.5V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 10% of V_{IN}		150		ms
Soft-Start Time MAX14653/ MAX14654/MAX14655	t_{SS}	V_{OUT} = 10% of V_{IN} to soft-start off		30		ms
Soft-Start Time MAX14717	t_{SS}	V_{OUT} = 10% of V_{IN} to soft-start off		165		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, C_{LOAD} = 100µF, V_{OUT} from 10%, V_{IN} to 90% V_{IN}		2		ms
Switch Turn-Off Time	t_{OFF}	V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{IN}, R_L = 100Ω, V_{IN} rising at 2V/µs		2		µs
ESD PROTECTION						
Human Body Model		All pins		±2		kV
IEC 61000-4-2 Contact Discharge		IN pin		±8		kV
IEC 61000-4-2 Air Gap Discharge		IN pin		±15		kV

Note 3: All specifications are 100% production tested at T_A = +25ºC, unless otherwise noted. Specifications are over -40ºC to +85ºC and are guaranteed by design.

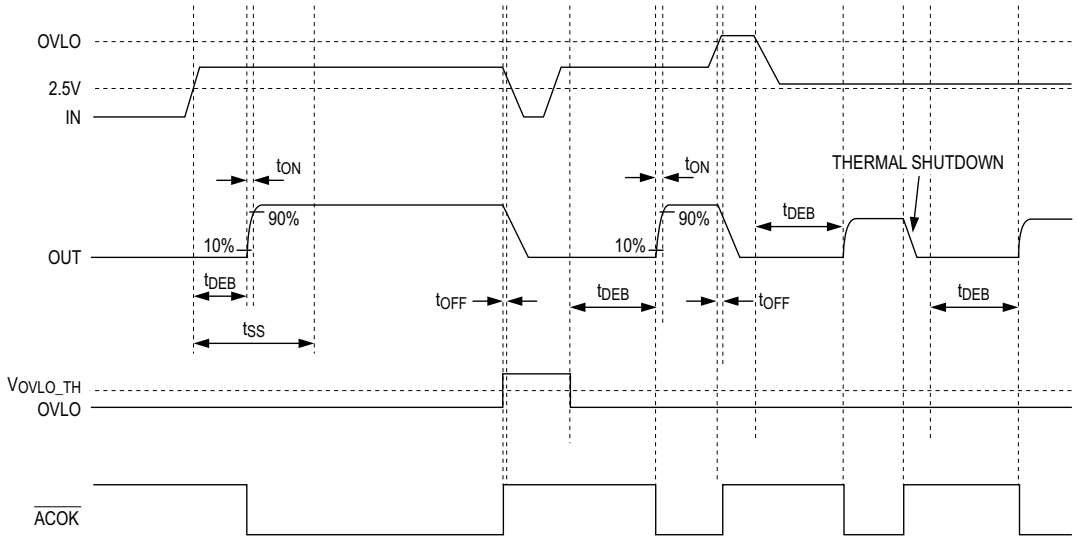
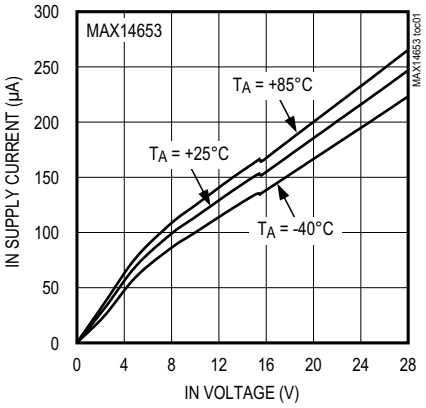


Figure 1. Timing Diagram

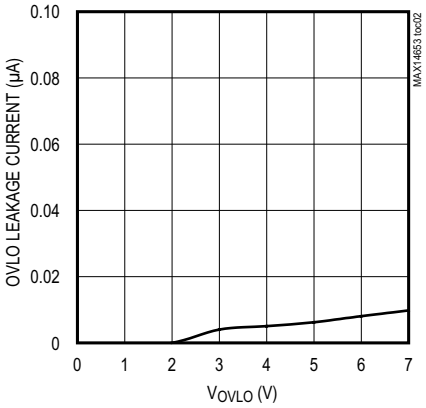
Typical Operating Characteristics

(V_{IN} = +5.0V, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25ºC, unless otherwise noted.)

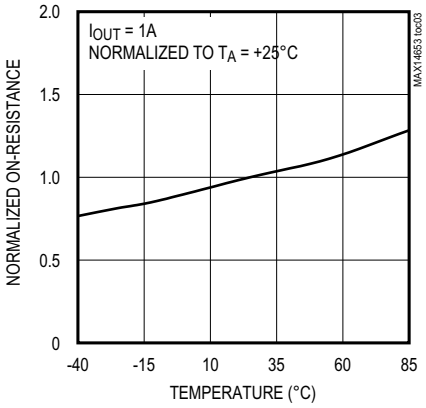
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



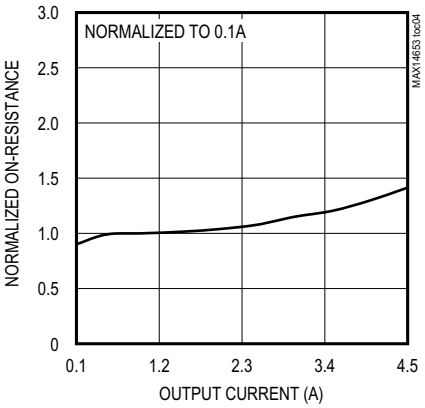
OVLO LEAKAGE CURRENT vs. V_{OVLO}



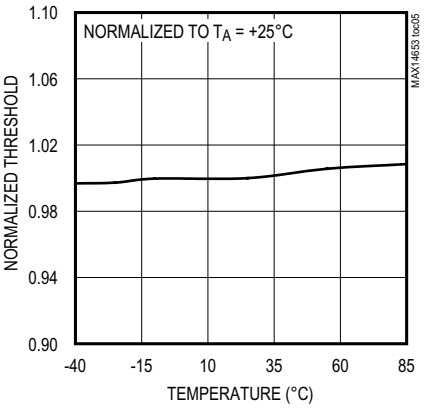
NORMALIZED R_{ON} vs. TEMPERATURE



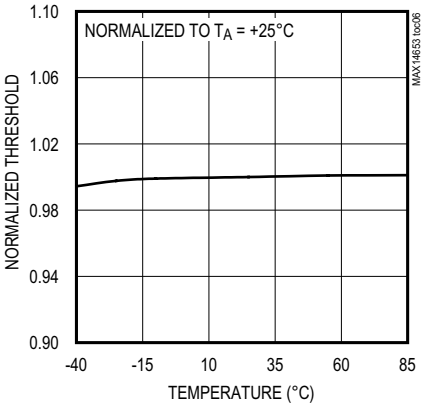
NORMALIZED R_{ON} vs. OUTPUT CURRENT



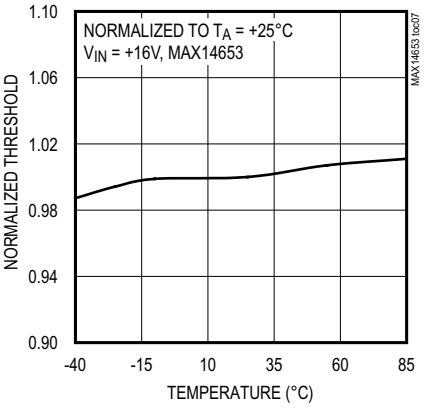
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



NORMALIZED EXTERNAL OVLO SET THRESHOLD vs. TEMPERATURE



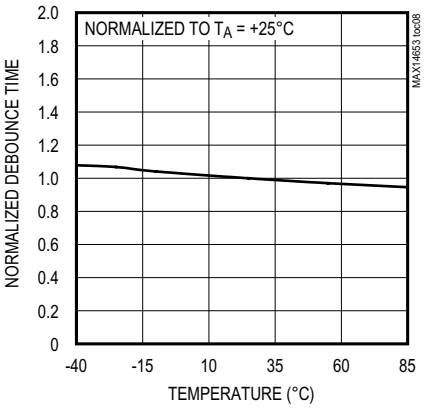
NORMALIZED EXTERNAL OVLO SELECT THRESHOLD vs. TEMPERATURE



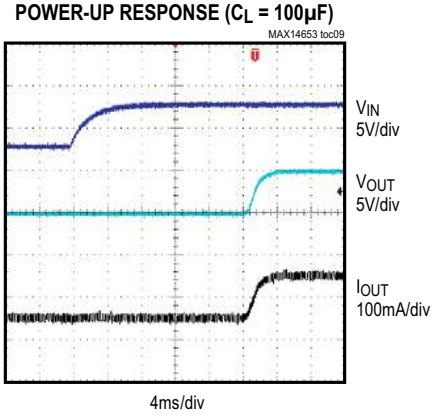
Typical Operating Characteristics (continued)

(V_{IN} = +5.0V, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25ºC, unless otherwise noted.)

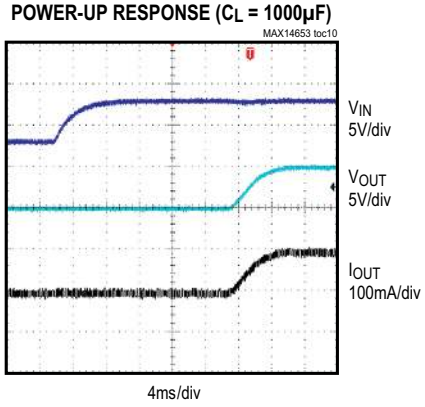
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



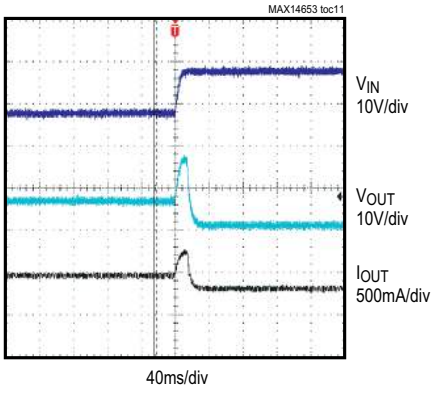
POWER-UP RESPONSE (C_L = 100µF)



POWER-UP RESPONSE (C_L = 1000µF)

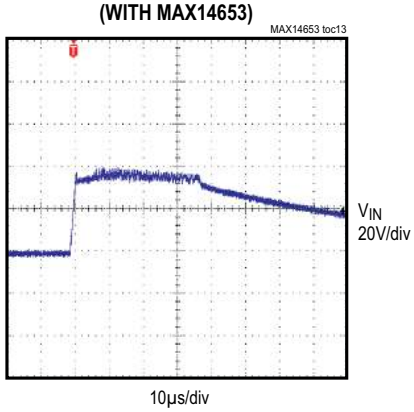


OVERVOLTAGE FAULT RESPONSE

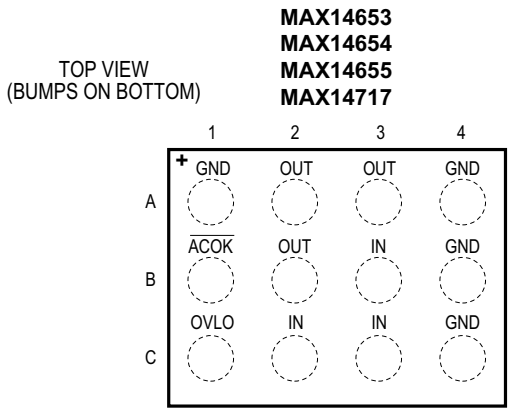


80V SURGE TEST WAVEFORM (WITHOUT MAX14653)

80V SURGE TEST WAVEFORM (WITH MAX14653)



Pin Configuration

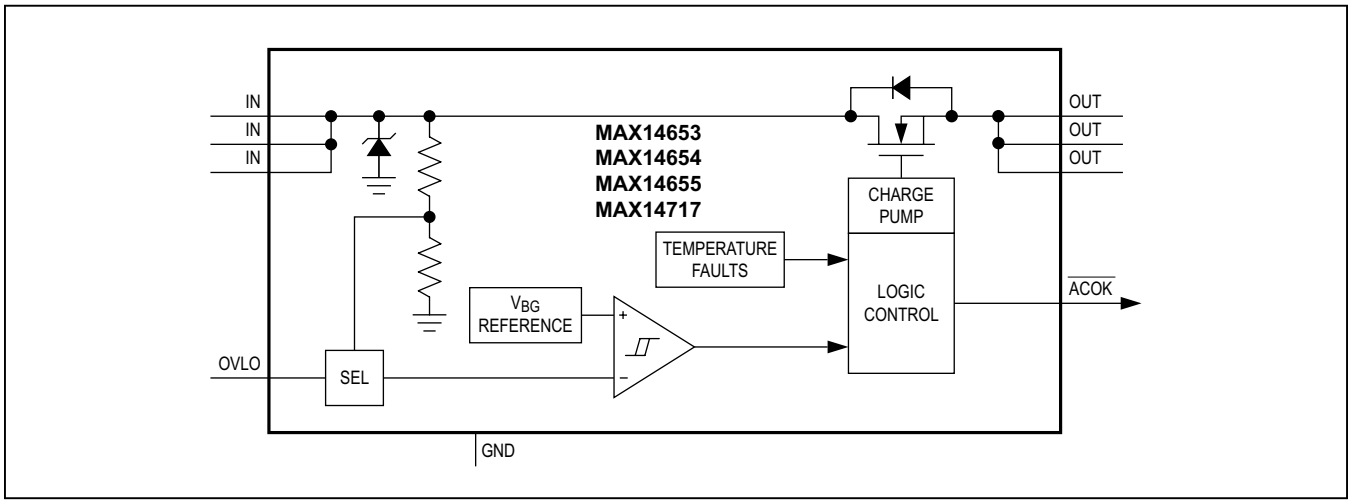


WLP
(1.3mm x 1.86mm)

Pin Description

PIN	NAME	FUNCTION
A1, A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.
A2, A3, B2,	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
B1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.
B3, C2, C3	IN	Voltage Input. Bypass IN with a 0.1µF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

Functional Diagram



Detailed Description

The MAX14653/MAX14654/MAX14655/MAX14717 overvoltage protection devices feature a low on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +80V. If the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The 15ms debounce time built into the device prevents false turn-on of the internal FET during startup.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when $V_{IN} < V_{IN\_OVLO}$ if internal trip thresholds are used or when $V_{IN} < V_{OVLO\_TH}$ if external trip thresholds are used. The charge-pump startup, which occurs after a 15ms debounce delay, turns the internal FET on (see the *Functional Diagram*). After the debounce time, soft-start limits the FET inrush current for 30ms (typ). At any time, if V_{IN} rises above V_{OVLO_THRESH}, OUT is disconnected from IN.

Internal Switch

The MAX14653/MAX14654/MAX14655/MAX14717 incorporate an internal FET with a 38mΩ (typ) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Overvoltage Lockout (OVLO)

The MAX14653 has a 15.5V (typ) overvoltage threshold (OVLO). The MAX14654/MAX14717 and MAX14655 have 6.8V and 5.825V (typ) OVLO thresholds, respectively.

Thermal Shutdown Protection

The MAX14653/MAX14654/MAX14655/MAX14717 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds +130ºC (typ). The device exits thermal shutdown once the junction temperature cools by 20ºC (typ).

$\overline{ACOK}$ Output

An open-drain $\overline{ACOK}$ output gives the MAX14653/MAX14654/MAX14655/MAX14717 the ability to communicate a stable power source to the host system. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.

Applications Information

IN Bypass Capacitor

For most applications, bypass IN to GND with a 0.1µF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

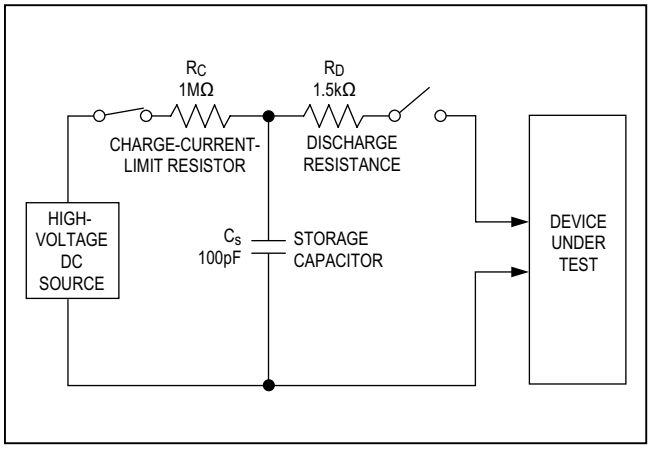


Figure 2a. Human Body ESD Test Model

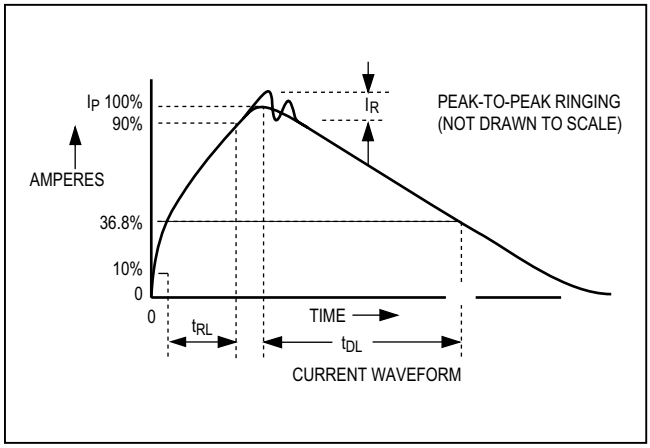


Figure 2b. Human Body Current Waveform

OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the MAX14653/MAX14654/MAX14655/MAX14717 to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition.

External OVLO Adjustment Functionality

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor divider. R_1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_THRESH}, and R_1 are known, R_2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left[1 + \frac{R_1}{R_2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX14653/MAX14654/MAX14655/MAX14717 are specified for ±2kV HBM typical ESD on all pins, Contact and Air-Gap Discharge on pin IN. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

HBM ESD Protection

Figure 2a shows the Human Body Model, while Figure 2b shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Ordering Information

PART	PIN-PACKAGE	TOP MARK	OVLO (V)
MAX14653EWC+T	12 WLP	ACS	15.5
MAX14654EWC+T	12 WLP	ACT	6.8
MAX14655EWC+T	12 WLP	ACU	5.825
MAX14717EWC+T	12 WLP	ADJ	6.8

Note: *All devices are specified over the -40ºC to +85ºC temperature range.*

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 WLP	W121G1+1	**21-0542**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	—
1	3/13	Removed future product asterisks for the MAX14653 and MAX14655	10
2	5/14	Added MAX14717	7