STANDARD MICROSYSTEMS CORPORATION

FDC 92C38/92C38B
FDC 92C38T/92C38BT

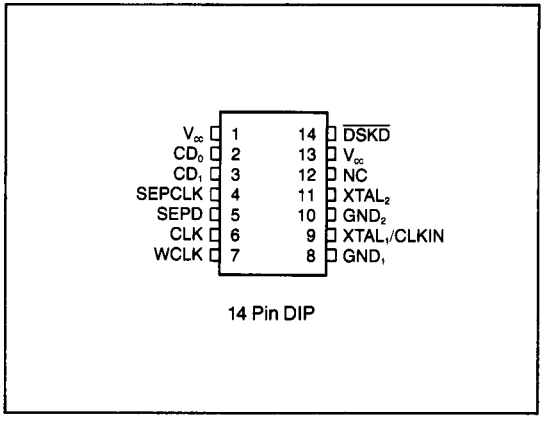
PRELIMINARY

CMOS Floppy Disk Data Separator and Clock Generator

FEATURES

- ☐ High Performance Digital Data Separator with Synthetic Oscillator and Phase Lock Loop for industry standard FDC 765A and FDC 7265
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Compatible with 3.5", 5.25" and 8" drives and data rates up to 500 KBs
- ☐ Internal Crystal Oscillator Circuit provides all clocks required by FDC 765A and FDC 7265
- ☐ Fabricated in power saving CMOS
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs
- ☐ Single +5 Volt supply
- ☐ Fully TTL compatible

PIN CONFIGURATION



14 Pin DIP

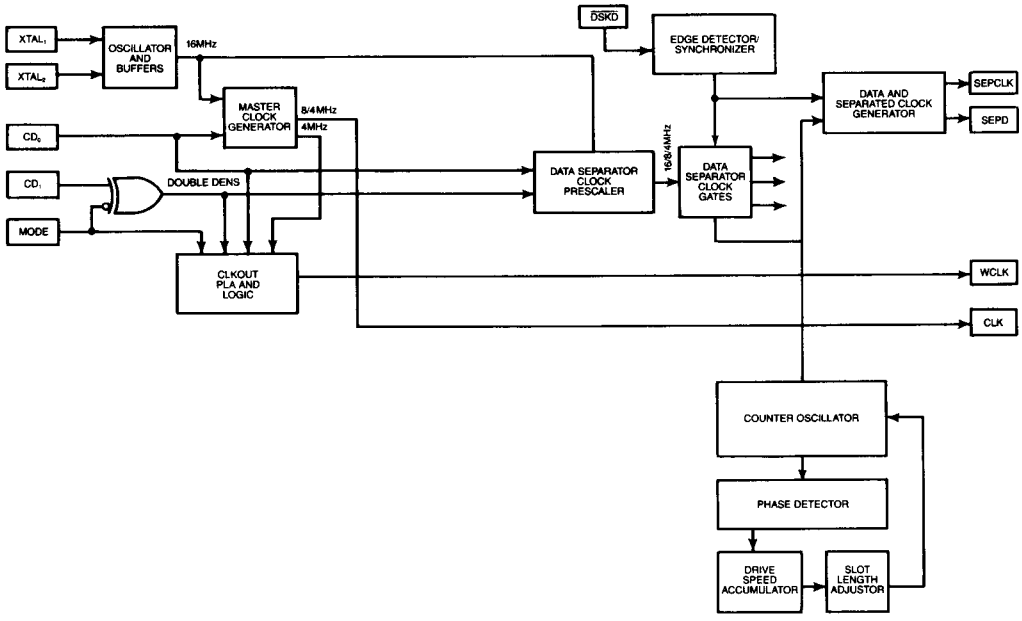
SECTION VI

FUNCTIONAL DESCRIPTION

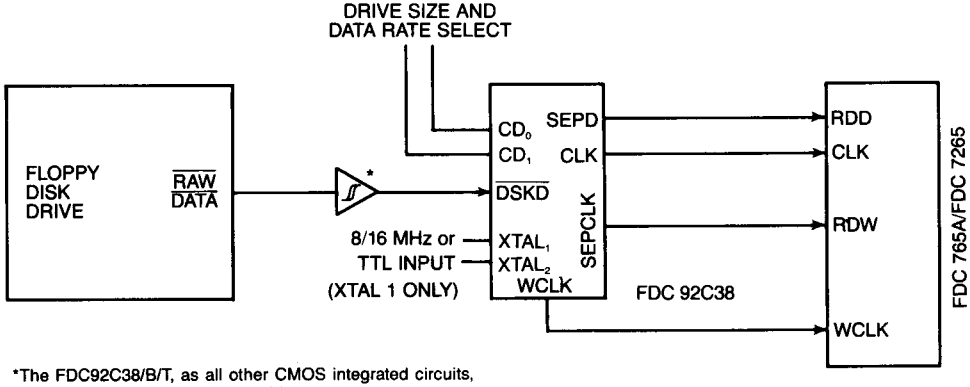
The FDC 92C38 is a CMOS integrated circuit designed to complement the FDC 765A (8272A) or the FDC 7265 floppy disk controller. It incorporates a high performance, synthetic phase locked loop digital data separator and clock generator in one 0.3 inch wide 14 pin package.

The use of a high performance synthetic phase locked loop data separator allows the system designer to replace (without sacrificing performance) a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC 92C38 is available in four versions: the FDC 92C38/T which is intended for disk transfer rates up to 250 kilobits per second and the FDC 92C38B/T is intended for disk transfer rates up to 500 kilobits per second.



FDC 92C38 BLOCK DIAGRAM



*The FDC92C38/B/T, as all other CMOS integrated circuits, presents a high impedance on all inputs

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{DSKD}$ input to the FDC92C38/B/T.

TYPICAL SYSTEM IMPLEMENTATION

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	V_{cc}	I	This pin MUST be tied to V_{cc}.
2,3	CD_0,CD_1	I	These inputs select the appropriate internal clock divisor for the data rate of the disk data, the CLK output to the FDC and the WCLK output to the FDC. Refer to Table 1.
4	SEPCLK	0	A Square wave window clock signal output derived from the $\overline{DSKD}$ input.
5	SEPD	0	This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). To insure complete compatibility with the FDC 765A and FDC 7265, this output is positive going.
6	CLK	0	This output provides the clock signal for the FDC 765A or FDC 7265.
7	WCLK	0	This output provides the write clock signal for the FDC 765A or FDC 7265.
8	GND_1		Ground
9	$XTAL_1$/CLKIN	I	This input is for direct connection to an 8 or 16 MHz single-phase TTL level clock, or one lead from an 8 or 16 MHz crystal.
10	GND_2	I	This pin must be tied to ground.
11	$XTAL_2$	I	In the FDC 92C38 and FDC 92C38B, the second lead from an 8 or 16 MHz crystal is connected to this pin. In the FDC 92C38T and FDC 92C38BT, this pin should be left floating.
12	NC		No connection should be made to this pin.
13	V_{cc}	I	+5 Volts
14	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)

SECTION VI

OPERATION

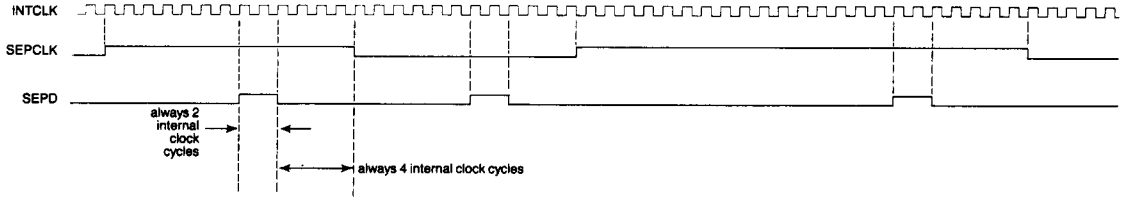
The high performance digital data separator incorporated in the FDC 92C38 will accept data from the floppy disk drive at 125 KHz, 250 KHz, or 500 KHz data rates and output the appropriate regenerated clock and data signals.

The heart of the digital floppy disk data separator section is a synthetic oscillator phase locked loop. One half-bit cell of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of 16 phase slices. The circuit, therefore, needs a phase slice clock with a frequency of 16 times the half-bit cell time.

Detection of an input pulse away from the center of its half-bit "slot" causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit slot closer to the pulse.

The end-of-cycle signal from the synthetic oscillator defines the derived clock waveform and the duration of each half-bit slot. If there is a flux transition during the half-bit slot, it is remembered and used to regenerate the data waveform pulses immediately following the end-of-cycle.

A short history of input pulse detections (which induce phase corrections by the FDC 92C38) is kept. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency, and helps compensate for drive speed variations. This, along with separate short term and long term correction algorithms, assures accurate floppy disk data separation.



MAXIMUM GUARANTEED RATINGS

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 300°C
Positive Voltage on any I/O Pin, with respect to ground	V_{CC} + 0.3V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Maximum V_{CC}	+ 7V
Power Dissipation	0.25W

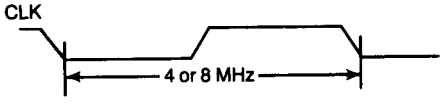
Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low (V_{IL})	−0.3		0.8	V	Except XTAL/CLKIN
High (V_{IH})	2.0		V_{cc}		
XTAL/CLKIN INPUT VOLTAGE					
Low (V_{IL})	−0.3		1.5	V	
High (V_{IH})	3.2		V_{cc}	V	
OUTPUT VOLTAGE					
Low (V_{OL})			0.4	V	L_{OL} = 1.6 ma, except CLK L_{OL} = 0.4 ma, CLK only
High (V_{OH})	2.4				L_{OH} = − 100µa, except CLK L_{OH} = − 400µa, CLK only
POWER SUPPLY CURRENT					
I_{cc}		TBD			
INPUT LEAKAGE CURRENT					
I_{IL}		TBD			
INPUT CAPACITANCE					
C_{IN}		TBD			
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
CLKIN Frequency	3.95	16	16.2	MHz	FDC 92C38B/BT
	3.95	8.0	8.1	MHz	FDC 92C38/T
CLKIN Duty Cycle	40		60	%	
T_{CLKOH}	90	125	140	ns	



XTAL	Inputs CD_1	Inputs CD_0	DISK DATA RATE	CLK	WCLK	ENCODING
16MHz	0	0	250KHz	8MHz	500KHz	FM
16MHz	1	0	500KHz	8MHz	1MHz	MFM
16MHz	0	1	125KHz	4MHz	250KHz	FM
16MHz	1	1	250KHz	4MHz	500KHz	MFM
8MHz	0	0	125KHz	4MHz	250KHz	FM
8MHz	1	0	250KHz	4MHz	500KHz	MFM
8MHz	0	1	Not Used			
8MHz	1	1	Not Used			

TABLE 1