Wintec Solid State Drive
1.8” SATA II
WxSSxxxG1TC-J2xx
(J2) Series

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Revision History

Revision	Month	Year	History
0.99	March	2012	Preliminary Release

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Wintec Solid State Drive

WxSSxxxG1TC-J2xx Series

Features:

GENERAL

- Density up to 256GB
- JMicron 612 controller with external SDRAM buffer
- SATA-II/I backwards compatible (3Gbps/1.5Gbps)
- High-Performance SLC or MLC NAND Flash memory

PERFORMANCE

- High Performance 190MB/s Seq. Read (SATA-II)*
- High Performance 110MB/s Seq. Write (SATA-II)*
- Random Read: 10,000 IOPS at 4KB transfer (SATA-II)

RELIABILITY

- Data Integrity under power cycling
- BCH ECC correction supports 16/24 bit ECC
- Enhanced endurance by dynamic/static wear leveling
- MTTF: 2,000,000 operating hours.

COMPATIBILITY

- Serial ATA Revision 2.6 Compliant
- ATA/ATAPI-7 Compliant
- Supports TRIM and S.M.A.R.T command

Wintec Solid State Drive

NOTE:
See Section 5.0 for Configuration & Ordering Guide

Description:

The Wintec Industries WxSSxxxG1TC-J2xx series of ROHS Compliant 1.8" uSATA Solid State drives are constructed with NAND-type flash memory devices paired to JMicron JMF612 SSD controller for virtual-to-physical address mapping and other sophisticated flash management functions. The Wintec Flash Solid State Disk (SSD) provides major advantages over the traditional magnetic hard disk drive (HDD). Faster access time and transfer rate, silent operation and low power consumption, better shock and vibration resistance, and lower total cost of ownership make the Wintec SSDs an attractive choice as the next generation mass storage device.

The Wintec 1.8" J2 series uSATA SSD provides high-speed data transfer and reliability utilizing SLC or MLC NAND flash in storage capacities ranging from 32GB to 256GB, in a small 1.8" hard drive form factor. Its robust design enables the SSD to achieve highest reliability and performance.

The JMF612 controller implements bad block management and dynamic/static wear-leveling techniques to ensure that the NAND flash memory is not worn out prematurely. The drive supports 24 bits/1K Byte sector BCH ECC algorithm for error correction. The drive supports basic S.M.A.R.T features to monitor the drive status and TRIM command to efficiently maintain the data.

The Wintec J2 series SSD drives are ideal for notebooks and embedded computing systems that need performance and reliability.

*Performance may vary based on drive configuration/NAND Flash type/capacity/test method used for testing.

1.0 General Product Specification

For all the following specifications, values are defined at ambient temperature unless otherwise stated.

Table 1: User Capacity Specifications

Model Number[1] (typ)[2,3]	NAND Flash Type	NAND Flash Total Capacity	Over-provison
W2SS032G1TC-J21xxx-yyy.zz	MLC	32 GB	**7%**
W2SS064G1TC-J21xxx-yyy.zz	MLC	64 GB	**7%**
W2SS128G1TC-J21xxx-yyy.zz	MLC	128 GB	**7%**

NOTE:
1. See Section 4.0 for Configuration & Ordering Guide
2. 1GB = 1,000,000,000 Bytes
3. Capacity available to end-user is less than "Total Capacity" due to flash controller overhead, and may vary with flash configuration.

Table 2: Typical Performance Specifications

Parameter	Typical Performance[4]
Sustained Sequential Read	up to 190 MB/sec (SATA-II)
Sustained Sequential Write	up to 110 MB/sec (2CE)/ 60MB/sec (1CE) (SATA-II)
Sustained IOPS Random Read	10,000 IOPS (SATA-II)

NOTE:
4. Bandwidth measured on high-performance desktop system. Note that performance may also vary depending on host system, drive capacity, and drive configuration. Measured at QD=32.

Table 3: Flash Endurance

Parameter	Spec
Program/Erase Cycles	up to 70,000 cycles for SLC up to 3,000 cycles for MLC
Data Retention	5 Years (Min.)
MTTF	2,000,000 Hours

Table 4: SSD Data Reliability

Parameter	Spec
Non-Recoverable Errors	< 1 in 10^{16} Bytes Read
Raw ECC Correctability	Up to 24 bits / 1K Bytes data

Table 5: Environmental Specifications

Parameters		Operating	Non-Operating
Temperature	**Commercial Temp.**	0°C to 70°C	-55°C to 95°C
	Industrial Temp.	-40°C to 85°C	-55°C to 95°C
Humidity (Non-Condensing)		5% to 95%	5% to 95%
Vibration		20 G RMS	N/A
Shock (Operating)		1,500 G (Max.)	
Noise		0 dB	0 dB

1.1 Block Diagram

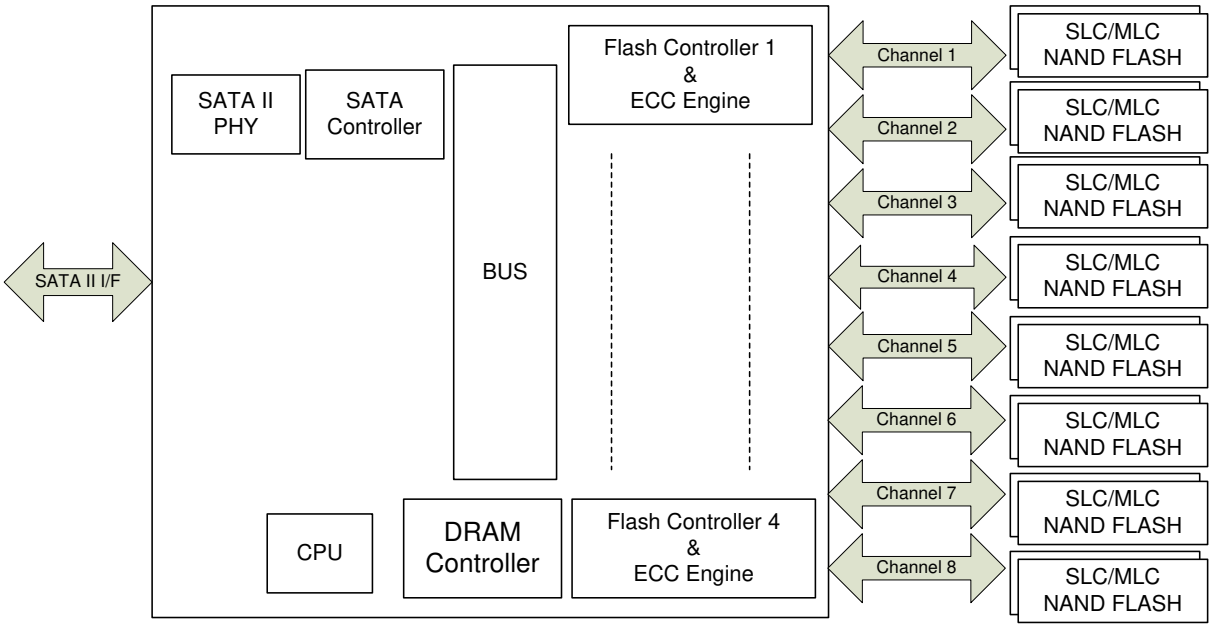

Figure 1. Block Diagram

1.2 Architecture

The Wintec 1.8" J2 series uSATA SSD utilizes a flash controller chip with 8 parallel channels of flash memory interface. The flash controller also simultaneously manages the file read and write interface with the host system via a single SATA-II interface. By utilizing 8 parallel channels of MLC flash memory, the Wintec SSD can provide both high performance and reliability, while maintaining a minimal unit cost.

1.3 Flash cell wear leveling

The SSD controller tracks the number of PE (program/erase) cycles that each block in the SSD goes through, and will dynamically remap logical sectors written from the host to different physical pages and blocks within the NAND flash. This including with static wear leveling ensures the flash cells wear evenly, and no premature wear out or data loss will occur in any portions of the drive.

1.4 Error correction and data integrity

The drive supports BCH error correction code; the controller can correct 16 bits or 24 bits per 1024 byte data.

1.5 TRIM support

The D4 series SSD supports the TRIM command. Data that has been deleted from the host can be marked as free space by the host issuing the TRIM command to the drive. This allows the drive to more efficiently reclaim free space and maintain performance.

2.0 Electrical Specification

2.1 General

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	V_{CC} With Respect to GND	-0.5	6.0	V

Table 7: Typical Operating Conditions (V_{CC}=5V ± 10%)

Symbol	Parameter	Min	Max	Units
V_{CC}	V_{CC} With Respect to GND	4.5	5.5	V
T_A	Operating Temperature **(Commercial Temp)**	0	70	°C
H	Humidity	5	95	%

Table 8: Power consumption

Symbol	Parameter	Value	Units
P_i	Idle Power consumption	0.95	Watts
P_T	Typical operating power consumption	1.50	Watts
P_{max}	Maximum operating power consumption	2.50	Watts

Power measurements were taken under IOMeter06 stress load with 4KB aligned reads and writes

2.2 SATA Pin Assignment and Description

The SATA connectors are compliant with standard SATA power specifications. As is standard, power may be supplied to all of the power pins. However, only the 5V power pins are utilized to provide power to the SSD. Therefore, where non-standard power supplies and connections are utilized, the power supply does not need to supply the SSD with power to the 3.3V power pins.

Table 9: SATA connector specification compliant

	No.	Plug Connector pin definition	
Signal	**S1**	**GND**	Ground
	S2	**A+**	Differential signal A
	S3	**A-**	
	S4	**GND**	Ground
	S5	**B-**	Differential signal B
	S6	**B+**	
	S7	**GND**	Ground
Key and spacing separate signal and power segments			
Power	**P1**	**V33**	3.3V power (Not Used)
	P2	**V33**	3.3V power (Not Used)
	P3	**GND**	Ground
	P4	**GND**	Ground

	P5	**V5**	5V power
	P6	**V5**	5V power
	P7	**Rev**	Not used
	P8	**Optional**	Not used
	P9	**Optional**	Not used

3.0 Software Interface

3.1 ATA Command Set

All mandatory, and many optional commands and features are supported. The following tables summarize the ATA feature set and commands.

Table 10: ATA Command

Command Name	Code	Parameters Used					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	O	X	X	O	X	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X

Note:
O = Valid, X = Don't care
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low/High Register
DR = Device Select Bit (Device/Head Register Bit 4)
HD = Head Select bit (Device/Head Register Bit 3-0)
FT = Features Register

3.2 SMART Command Support

3.2.1 SMART Function Set (B0h)

The J2 series express card performs different processing required for predicting device failures, according to the subcommand specified in the feature register. If the feature register contains an unsupported value, the aborted command error is returned. If the SMART function is disabled, any subcommand other than SMART enable operations results in the aborted command error.

Table 11: SMART Function Set (B0h)

Value	Command	Value	Command
D0h	Read Data attributes	**D1h**	Read attribute Threshold
D2h	Enable/Disable attribute auto save	**D3h**	Save attribute Values
D4h	Execute Off-line Immediate	**D5h**	Read log
D6h	Write log	**D8h**	Enable SMART operation
D9h	Disable SMART operation	**DAh**	Return Status
DBh	Enable/Disable Auto Off-line		

3.2.2 SMART Read Data (B0h/D0h)

This command returns 512-byte SMART data structure to the host with PIO data-in protocol. The register file has to contain D0h for features register, 4Fh for LBA mid register and C2h for the LBA high register.

Table 12: SMART Attribute Data Structure

Byte	Description
0-1	Data Structure revision number
2-13	1st attribute data
14-361	2^{nd}-30^{th} Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364-365	Total time in seconds to complete off-line data collection
366	Reserved
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability
371	Self-test failure checkpoint
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374-510	Reserved
511	Data structure checksum

Table 13: Byte 2-361 Individual attribute data

Byte	Description
0	Attribute ID
1-2	Status Flag
3	Attribute Value
4	Worst ever normalized attribute value
5-10	Raw attribute value
11	Reserved

3.2.3 SMART Attribute ID

The following table summarizes the SMART attribute ID information.

Table 13: SMART Attribute Menu Summary

ID	Hex	Attribute Name
1	01h	Read Error Rate
2	02h	Throughput Performance
3	03h	Spin up time
5	05h	Reallocated Sector Count
7	07h	Seek Error Rate
8	08h	Seek Time Performance
9	09h	Power-On hours Count
10	0Ah	Spin Retry Count
12	0Ch	Device Power Cycle Count
168	A8h	SATA PHY Error Count
170	AAh	Bad Block Count
173	ADh	Erase Count
175	AFh	Bad Cluster Table Count
192	C0h	Unexpected power Loss Count
194	C2h	Temperature
197	C5h	Current Pending Sector Count
240	F0h	Write Head

3.2.4 SMART Read Attribute Threshold (B0h/D1h)

This command transfers 512 bytes of drive failure threshold data to the host.

Byte	Description
0-1	Data structure revision number
2-361	1st- 30th individual attribute threshold data
362-510	Reserved
511	Data structure checksum

3.2.5 SMART Enable/Disable Attribute Auto save (B0h/D2h)

This command enables and disables the optional attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attributes to non-volatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature, either enabled or disabled, shall be preserved by the device during all power and reset events.

A value of zero written by the host into the devices count field before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to no-volatile memory during some other normal operation (e.g., during a power-on or power-off sequence or during an error recovery sequence).

A value of F1h written by the host into the device's count field before issuing this command shall cause this feature to be enabled. Any other non-zero value written by the host into this field before issuing this command is vendor specific. The meaning of any non-zero value written to this field at this time shall be preserved by the device during all power and reset events.

3.2.6 SMART Enable/Disable Attribute Auto save (B0h/D2h)

Saves any modified attribute values

3.2.7 SMART Execute Off-line Immediate (B0h/D4h)

This command of non-data input causes the controller to immediately initiate the set of activities that collect SMART data in off-line mode and then save data to the NAND flash memory, or execute a self-diagnostic test routine in either captive or off-line mode.

Byte	Description of subcommand to be executed
0	Execute SMART off-line routine immediately in off-line mode
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART extended self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART extended self-test routine immediately in off-line mode

3.2.8 SMART Read Log (B0h/D5h)

This command returns the indicated log sector contents to the host.
Sector count specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log, regardless of the sector count requested. Sector number indicates the log sector to be returned as described in the following Table.

Value	Content	R/W
0	Execute SMART off-line routine immediately in off-line mode	RO
1	Execute SMART Short self-test routine immediately in off-line mode	RO
2	Execute SMART extended self-test routine immediately in off-line mode	RO
3	Abort off-line mode self-test routine	RO

6	Execute SMART Short self-test routine immediately in captive mode	RO
7	Execute SMART extended self-test routine immediately in off-line mode	RO
128-159	Host vendor specific	R/W

3.2.9 SMART Write Log (B0h/D6h)

This command writes as indicated number of 512 byte data sectors to the indicated log (Host vendor specific).

3.2.10 SMART Enable Operations (B0h/D8h)

Enables the SMART function; this setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters.

3.2.11 SMART Disable Operations (B0h/D9h)

Disables the SMART function; upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.
Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the aborted Command error.
This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

3.2.12 SMART Return Status (B0h/DAh)

Reports the drive reliability status;

Values reported when a predicted defect has not been detected:

Cylinder Low register: 4Fh
Cylinder High register: C2h

Values reported when a predicted defect has been detected:

Cylinder Low register: F4h
Cylinder High register: 2Ch

3.2.13 SMART Enable/Disable Automatic Off-line (B0h/DBh)

Enables (when Sector Count register = "F8h") or disables (Sector Count register = "00h") the automatic off-line data collection function.
The automatic collection is disabled if a value of "00h" is set in the Sector Count register before a subcommand is issued. If automatic collection is disabled, the drive can still save attribute information during normal operation, such as during the power-on/off sequence or error correction sequence.
The automatic collection function is enabled if a value of "F8h" is set in the Sector Count register before the command is issued. Values other than "00h" and "F8h" are vendor-specific.

4.0 Physical Specifications

Table 15: Physical Specifications

Weight:	**3.0 oz typical**
Length:	**78.5 mm**
Width:	**54.0 mm**
Thickness:	**5.0 mm**

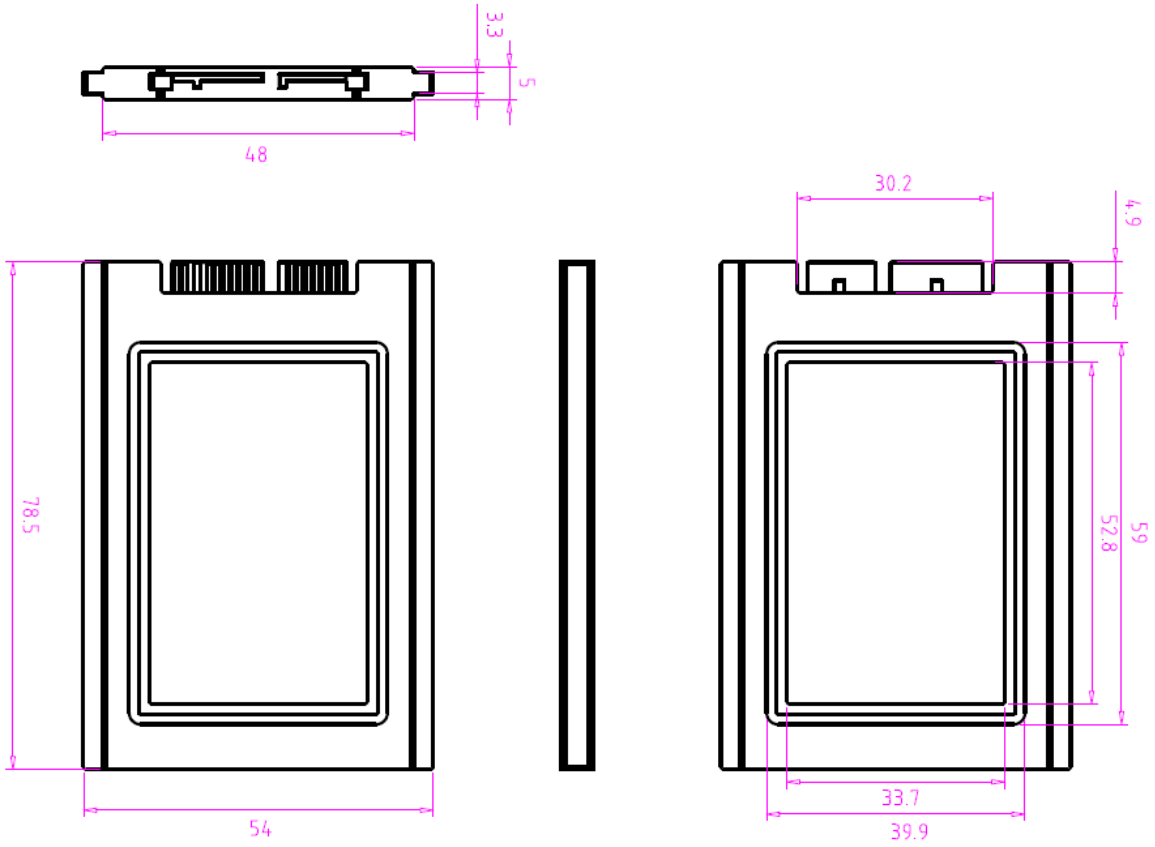

Figure 2: Physical Dimensions

5.0 Ordering Information

Table 16: Product Availability List & Naming

Model Number[1]	NAND Flash Type	Overprovision	User Capacity (typ)[2,3]
W2SS032G1TC-J21xxx-yyy.zz	MLC	7%	**30 GB**
W2SS064G1TC-J21xxx-yyy.zz	MLC	7%	**60 GB**
W2SS128G1TC-J21xxx-yyy.zz	MLC	7%	**120 GB**

(*u*) Flash Type
7: SLC Flash
2: MLC Flash

(*xxx*) Flash IC Manufacturer, Die Revision, Process

P: Samsung	M: M-die	3:3x nm
I: Intel	A: A-die	2:2x nm
M: Micron	B: B-die	
T: Toshiba	C: C-die	

(*yyy*) Component Flash Configuration
008: 8-Nand, Single Die Package, 1-CE
08D: 8-Nand, Dual Die Package, 1-CE
8D2: 8-Nand, Dual Die Package, 2-CE
8Q2: 8-Nand, Quad Die Package, 2-CE

(*zz*) Firmware Revision/Options
Please contact the factory for the latest firmware revisions and/or custom labeling and programming identification.

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About Wintec Industries, Inc.:
Wintec Industries, founded in 1988, is headquartered in Milpitas, California. Wintec, an ODM/OEM solution provider, specializes in product designs and manufacturing, including Flash modules (CF, SD, USB, embedded Flash, SSD, etc), DRAM modules (RDIMM, SODIMM, UDIMM), wireless products, modem products (embedded and USB), Advanced Digital Display products (ADD2 DVI, HDMI, digital signage), and so on. With experienced engineering team in Silicon Valley, Wintec provides a wide range of services and solutions for customers. Wintec is ISO9001-2000 certified.

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