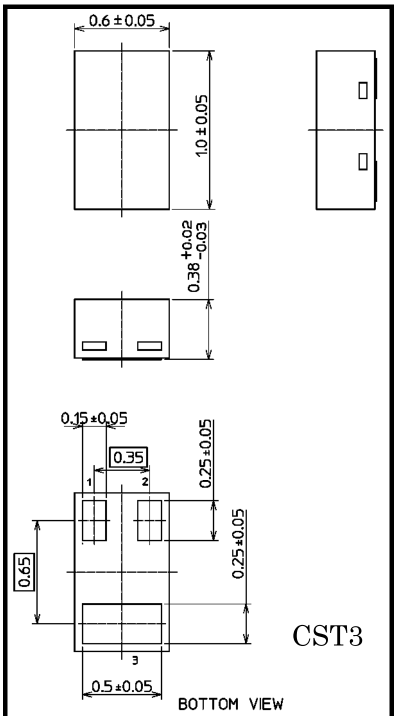
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K37CT

○ High Speed Switching Applications
○ Analog Switch Applications

- 1.5Vdrive
- Low ON-resistance $R_{DS(ON)}$ = 5.60 Ω (max) (@V_{GS} = 1.5 V)
  $R_{DS(ON)}$ = 4.05 Ω (max) (@V_{GS} = 1.8 V)
  $R_{DS(ON)}$ = 3.02 Ω (max) (@V_{GS} = 2.5 V)
  $R_{DS(ON)}$ = 2.20 Ω (max) (@V_{GS} = 4.5 V)

Unit : mm



JEDEC	―
JEITA	―
TOSHIBA	2-1J1B

Weight: 0.75mg(typ.)

Absolute Maximum Ratings (Ta = 25°C)

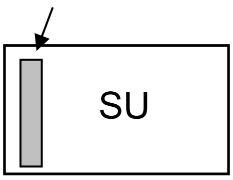
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	20	V
Gate-Source voltage		V_{GSS}	± 10	V
Drain current	DC	I_D	200	mA
	Pulse	I_{DP}	400	
Power dissipation		P_D(Note1)	100	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board
(10 mm × 10 mm × 1.0 mm, Cu Pad: 100 mm^2)

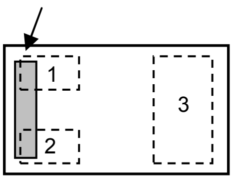
Marking(top view)

Polarity mark



Pin Condition (top view)

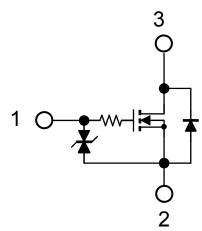
Polarity mark (on the top)



1. Gate
2. Source
3. Drain

*Electrodes: On the bottom

Equivalent Circuit



Start of commercial production
2010-11

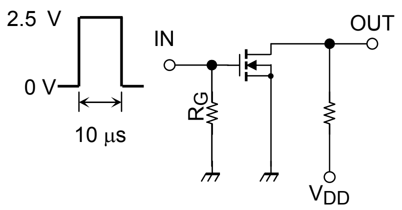
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\,DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
		$V_{(BR)\,DSX}$	I_D = 1 mA, V_{GS} = -10 V	12	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.35	—	1.0	V
Forward transfer admittance		$\lvert Y_{fs} \rvert$	V_{DS} = 3 V, I_D = 100 mA (Note2)	0.14	0.28	—	S
Drain-source ON-resistance		$R_{DS\,(ON)}$	I_D = 100 mA, V_{GS} = 4.5 V (Note2)	—	1.65	2.20	Ω
			I_D = 50 mA, V_{GS} = 2.5 V (Note2)	—	2.16	3.02	
			I_D = 20 mA, V_{GS} = 1.8 V (Note2)	—	2.66	4.05	
			I_D = 10 mA, V_{GS} = 1.5 V (Note2)	—	3.07	5.60	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	12	—	pF
Output capacitance		C_{oss}		—	5.5	—	
Reverse transfer capacitance		C_{rss}		—	4.1	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 100 mA	—	18	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to 2.5 V, R_G = 50 Ω	—	36	—	
Drain-Source forward voltage		V_{DSF}	I_D = -200 mA, V_{GS} = 0 V (Note2)	—	-0.89	-1.2	V

Note2: Pulse test

Switching Time Test Circuit

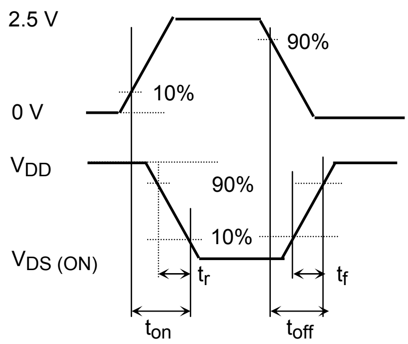
(a) Test Circuit



V_{DD} = 10 V
R_G = 50Ω
Duty ≤ 1%
V_{IN} : t_r, t_f < 5 ns
Common source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Precaution

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (1mA for the SSM3K37CT). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than $V_{th.}$ This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

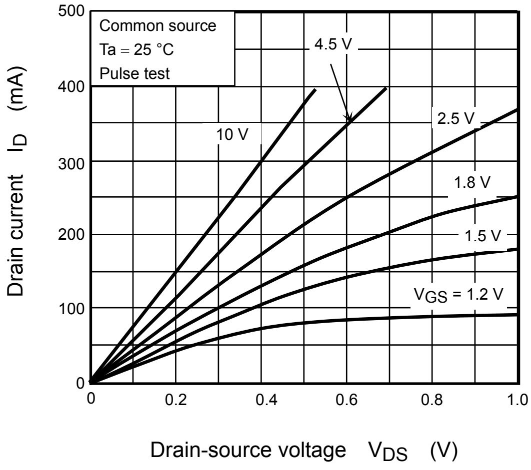
Take this into consideration when using the device.

Handling Precaution

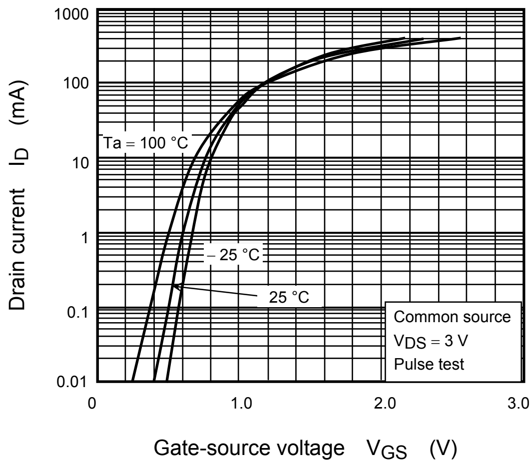
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\,(ch\text{-}a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

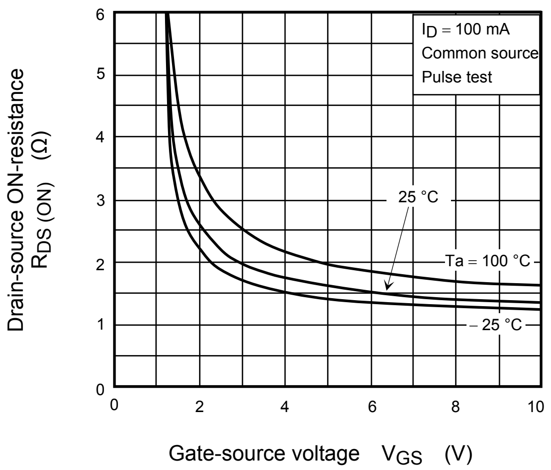
$I_D – V_{DS}$



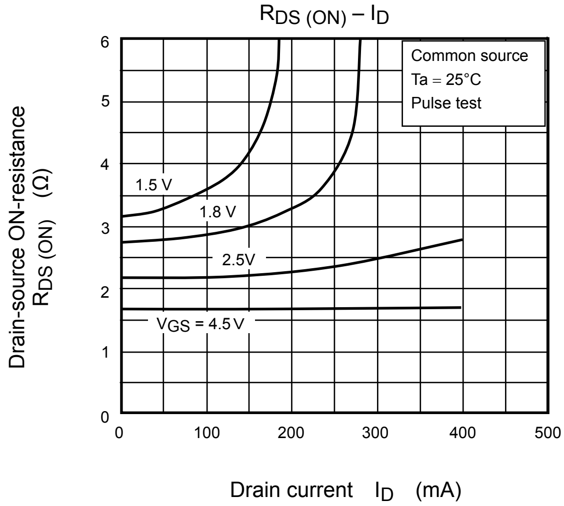
$I_D – V_{GS}$



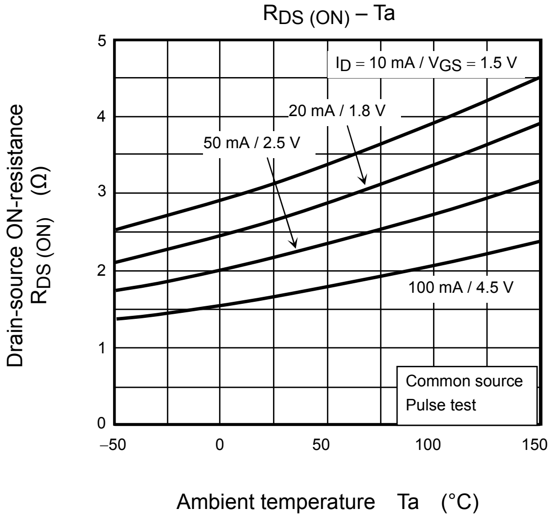
$R_{DS\ (ON)} – V_{GS}$



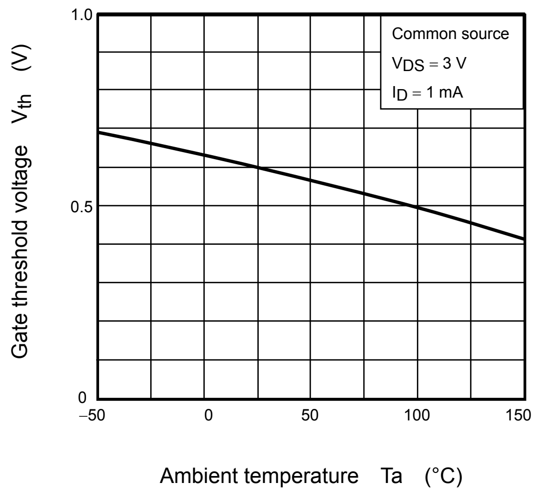
$R_{DS\ (ON)} – I_D$

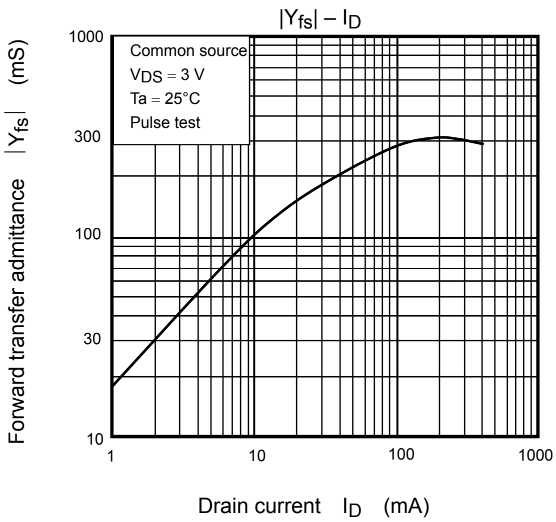


$R_{DS\ (ON)} – Ta$

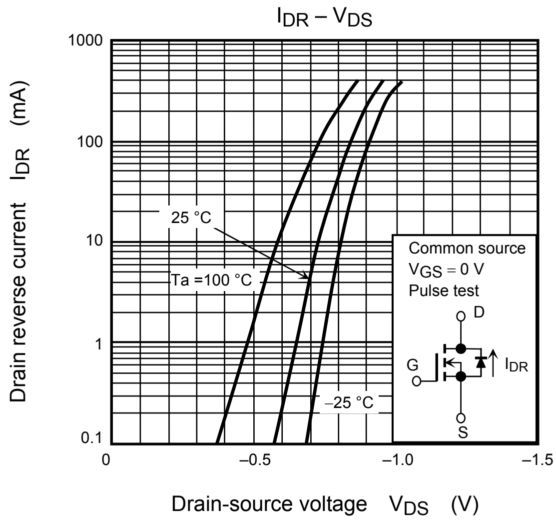


$V_{th} – Ta$

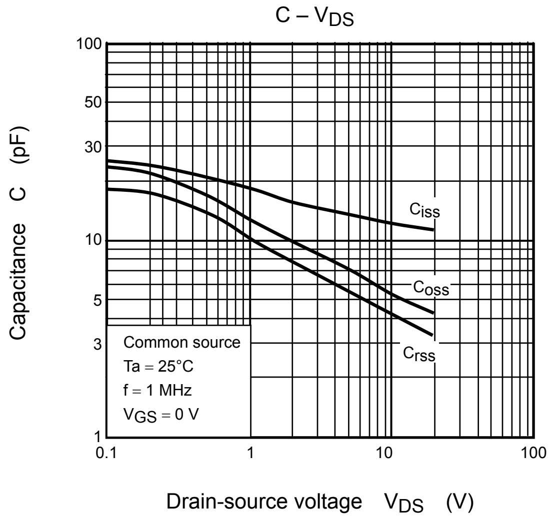




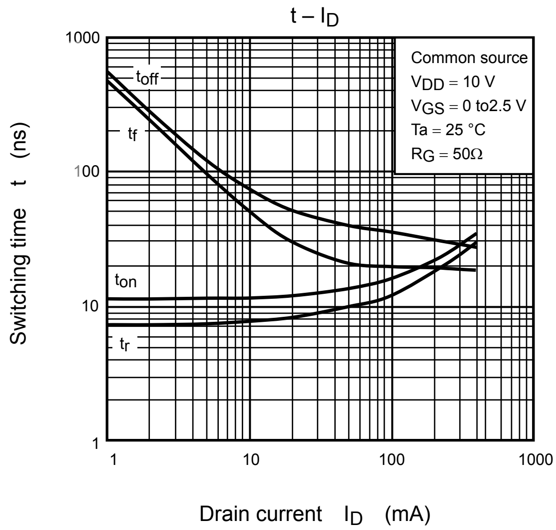
|Yfs| – ID
Common source
VDS = 3 V
Ta = 25°C
Pulse test
Forward transfer admittance |Yfs| (mS)
Drain current ID (mA)



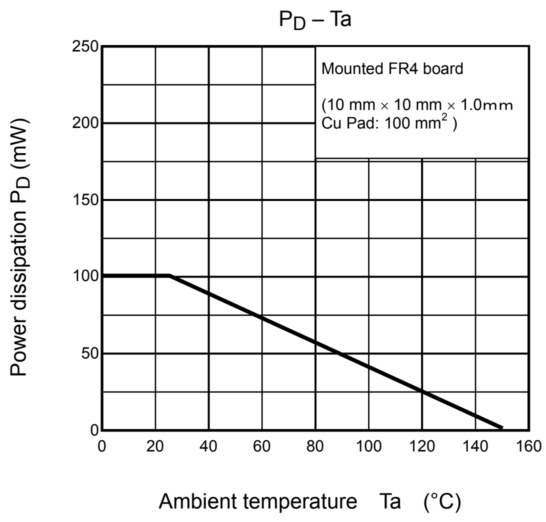
IDR – VDS
25 °C
Ta =100 °C
–25 °C
Common source
VGS = 0 V
Pulse test
D
G
S
IDR
Drain reverse current IDR (mA)
Drain-source voltage VDS (V)



C – VDS
Ciss
Coss
Crss
Common source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
Drain-source voltage VDS (V)



t – ID
toff
tf
ton
tr
Common source
VDD = 10 V
VGS = 0 to2.5 V
Ta = 25 °C
RG = 50Ω
Switching time t (ns)
Drain current ID (mA)



PD – Ta
Mounted FR4 board
(10 mm × 10 mm × 1.0mm
Cu Pad: 100 mm2)
Power dissipation PD (mW)
Ambient temperature Ta (°C)

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