

54ABT646

Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 54ABT646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \overline{OE} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \overline{OE} is Active LOW. In the isolation mode (control \overline{OE} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

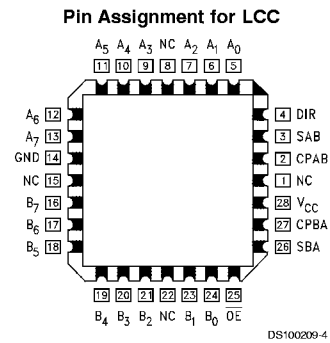
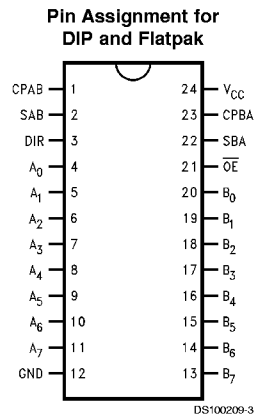
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9457701

Ordering Code

Military	Package Number	Package Description
54ABT646J-QML	J24A	24-Lead Ceramic Dual-In-Line
54ABT646W-QML	W24C	24-Lead Cerpack
54ABT646E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

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Connection Diagrams



Pin Descriptions

Pin Names	Description
A ₀ –A ₇	Data Register A Inputs/ TRI-STATE Outputs
B ₀ –B ₇	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
\overline{OE}	Output Enable Input
DIR	Direction Control Input

Connection Diagrams (Continued)

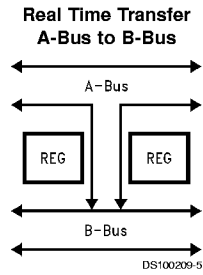


FIGURE 1.

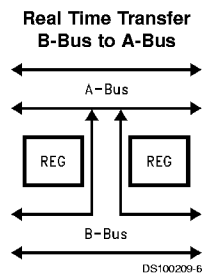


FIGURE 2.

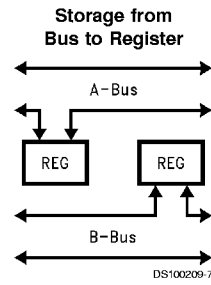


FIGURE 3.

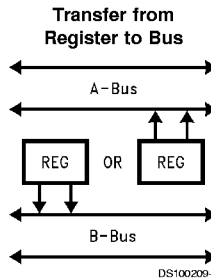


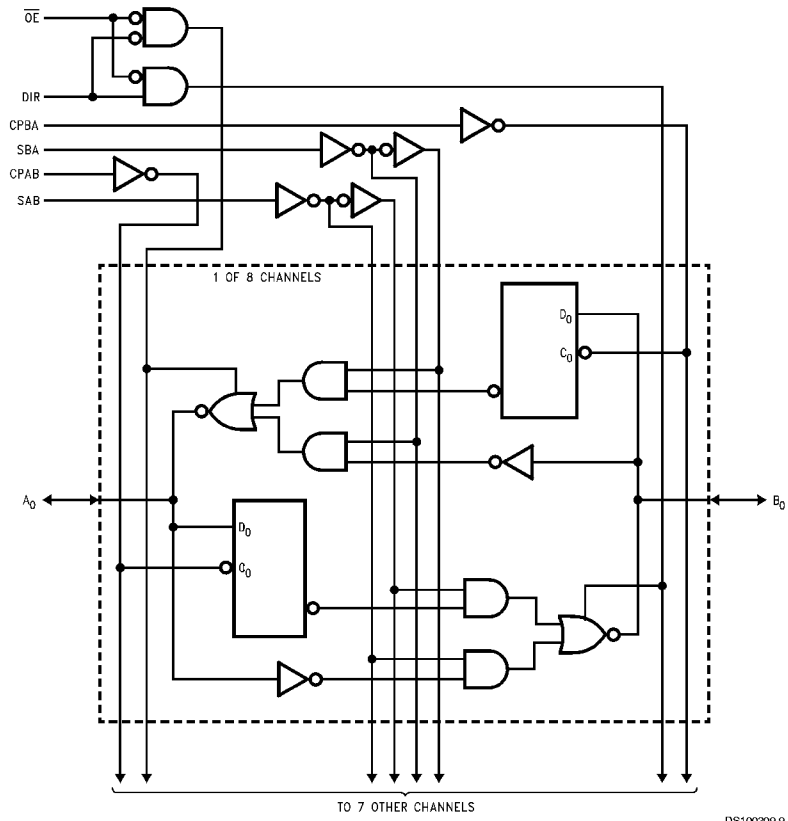
FIGURE 4.

Inputs						Data I/O (Note 1)		Function
OE	DIR	CPAB	CPBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	
H	X	H or L	H or L	X	X			Isolation
H	X	↗	X	X	X	Input	Input	Clock A _n Data into A Register Clock B _n Data into B Register
H	X	X	↗	X	X			
L	H	X	X	L	X			A _n to B _n — Real Time (Transparent Mode)
L	H	↗	X	L	X	Input	Output	Clock A _n Data into A Register A Register to B _n (Stored Mode)
L	H	H or L	X	H	X			A Register to B _n (Stored Mode)
L	H	↗	X	H	X			Clock A _n Data into A Register and Output to B _n
L	L	X	X	X	L			B _n to A _n — Real Time (Transparent Mode)
L	L	X	↗	X	L	Output	Input	Clock B _n Data into B Register B Register to A _n (Stored Mode)
L	L	X	H or L	X	H			B Register to A _n (Stored Mode)
L	L	X	↗	X	H			Clock B _n Data into B Register and Output to A _n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

Logic Diagram



DS100209-9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	Military	-55°C to +125°C
Supply Voltage	Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)	
Data Input		50 mV/ns
Enable Input		20 mV/ns
Clock Input		100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT646			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage	0.8			V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2			V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	54ABT	2.5		V		I _{OH} = -3 mA, (A _n , B _n)
		54ABT	2.0		Min		I _{OH} = -24 mA, (A _n , B _n)
V _{OL}	Output LOW Voltage	0.55			V	Min	I _{OL} = 48 mA, (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current	5			μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 5)
		5					V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	7			μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	100			μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current	-5			μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 5)
		-5					V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current	50			μA	0V-5.5V	V _{OUT} = 2.7V (A _n , B _n); \overline{OE} = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current	-50			μA	0V-5.5V	V _{OUT} = 0.5V (A _n , B _n); \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current	50			μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test	100			μA	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{COH}	Power Supply Current	250			μA	Max	All Outputs HIGH
I _{COL}	Power Supply Current	30			mA	Max	All Outputs LOW
I _{COZ}	Power Supply Current	50			μA	Max	Outputs TRI-STATE; All Others GND
I _{CCT}	Additional I _{CC} /Input	2.5			mA	Max	V _I = V _{CC} - 2.1V All Other Outputs at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 5)	No Load	0.18		mA/MHz	Max	Outputs Open \overline{OE} and DIR = GND, Non-I/O = GND or V _{CC} (Note 4) One Bit toggling, 50% duty cycle

DC Electrical Characteristics (Continued)

Note 4: For 8-bit toggling, $I_{CCD} < 1.4 \text{ mA/MHz}$.

Note 5: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50 \text{ pF}$			
		Min	Max		
f_{max}	Max Clock Frequency	125		MHz	
t_{PLH}	Propagation Delay	2.2	8.8	ns	Figure 8
t_{PHL}	Clock to Bus	1.7	8.8		
t_{PLH}	Propagation Delay	1.5	7.9	ns	Figure 8
t_{PHL}	Bus to Bus	1.5	7.9		
t_{PLH}	Propagation Delay	1.5	8.1	ns	Figure 8
t_{PHL}	SBA or SAB to A_n to B_n	1.5	8.9		
t_{PZH}	Enable Time	1.0	7.3	ns	Figure 10
t_{PZL}	$\overline{\text{OE}}$ to A_n or B_n	1.9	8.8		
t_{PHZ}	Disable Time	1.5	9.3	ns	Figure 10
t_{PLZ}	$\overline{\text{OE}}$ to A_n or B_n	1.5	9.3		
t_{PZH}	Enable Time	1.0	7.7	ns	Figure 10
t_{PZL}	DIR to A_n or B_n	2.2	9.5		
t_{PHZ}	Disable Time	1.5	8.7	ns	Figure 10
t_{PLZ}	DIR to A_n or B_n	1.5	9.2		

AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50 \text{ pF}$			
		Min	Max		
$t_{\text{S(H)}}$	Setup Time, HIGH	3.5		ns	Figure 11
$t_{\text{S(L)}}$	or LOW Bus to Clock				
$t_{\text{H(H)}}$	Hold Time, HIGH	1.0		ns	Figure 11
$t_{\text{H(L)}}$	or LOW Bus to Clock				
$t_{\text{W(H)}}$	Pulse Width, HIGH	4.0		ns	Figure 9
$t_{\text{W(L)}}$	or LOW				

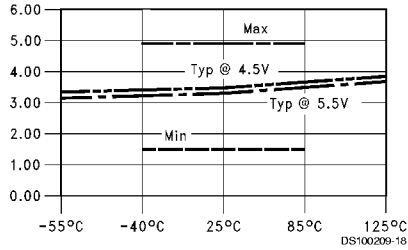
Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (non I/O pins)
$C_{\text{I/O}}$ (Note 6)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n , B_n)

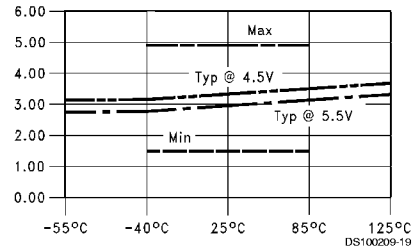
Note 6: $C_{\text{I/O}}$ is measured at frequency, $f = 1 \text{ MHz}$, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

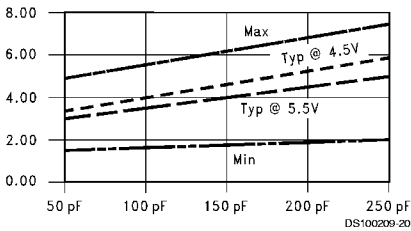
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



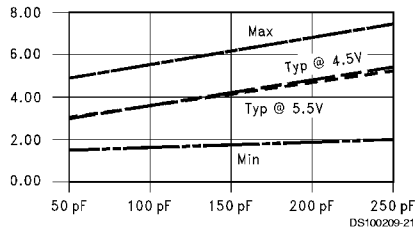
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



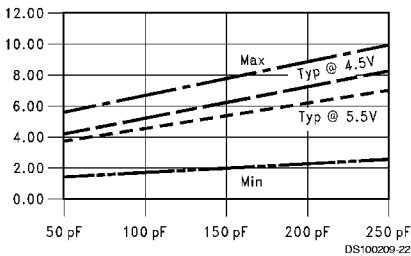
t_{PLH} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



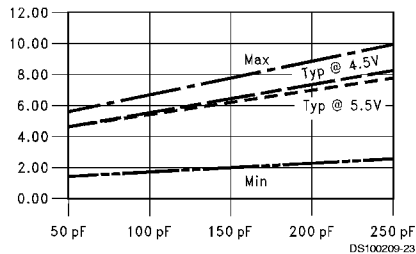
t_{PHL} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



t_{PLH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



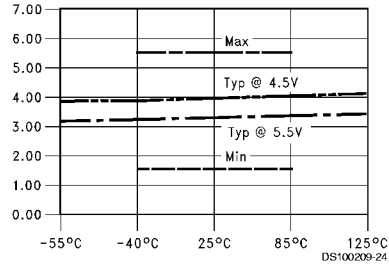
t_{PHL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 Clock to Bus



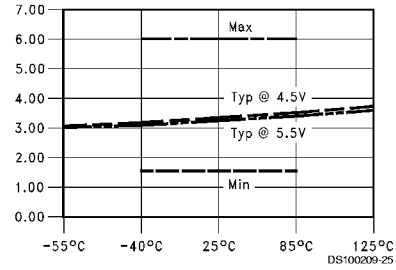
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

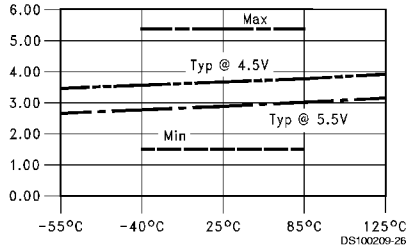
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 OE to Bus



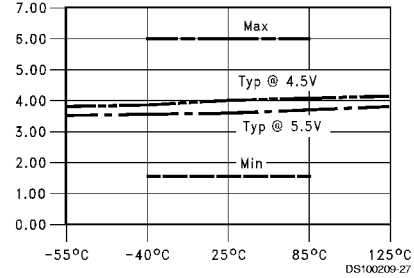
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 OE to Bus



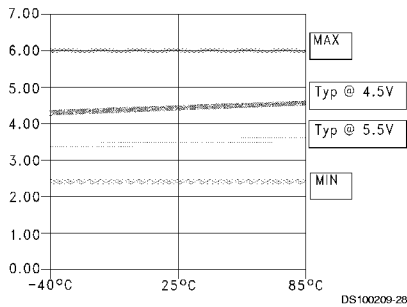
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



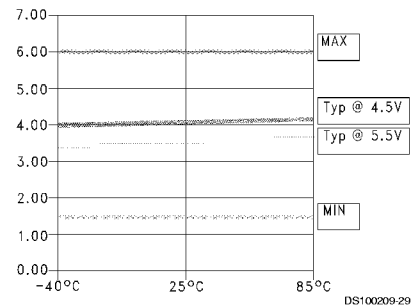
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 OE to Bus



t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 OE to Bus



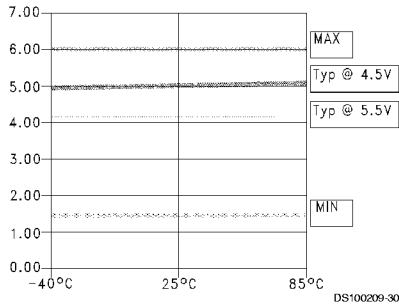
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 OE to Bus



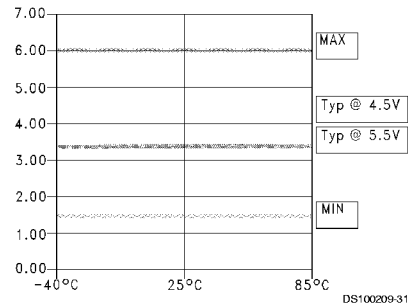
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

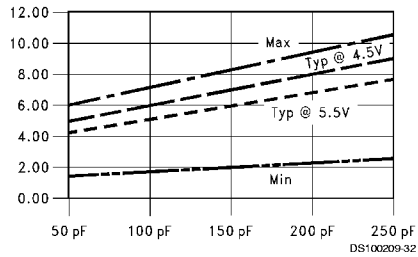
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 OE to Bus



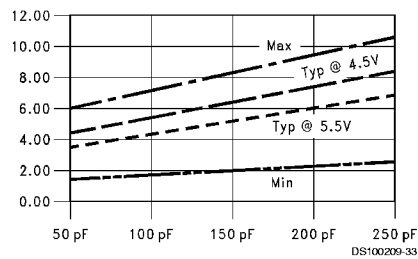
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching
 OE to Bus



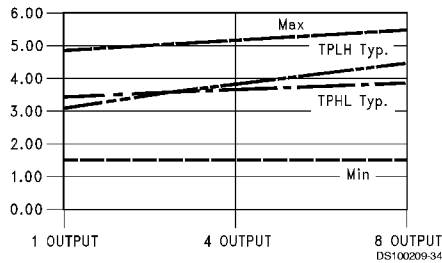
t_{PZL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 OE to Bus



t_{PZH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$
 OE to Bus



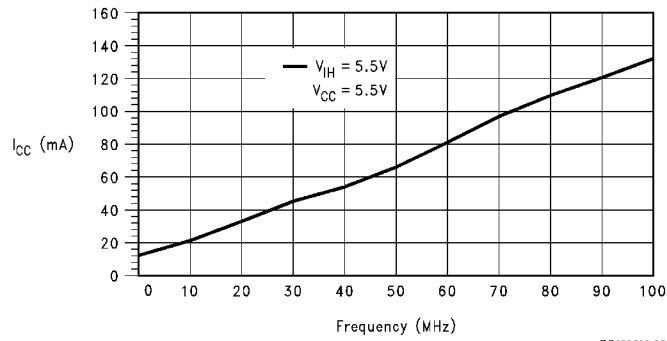
t_{PLH} and t_{PHL} vs Number Output Switching
 $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$
 $C_L = 50$ pF, Clock to Bus



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

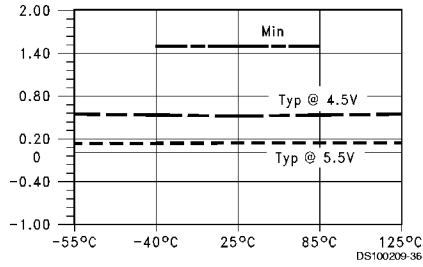
Capacitance (Continued)

I_{CC} vs Frequency, Average,
 $T_A = 25^\circ\text{C}$, $V_{CC} = 5.5\text{V}$
All Outputs Unloaded/Unterminated;
All Outputs Switching in phase @50% Duty Cycle



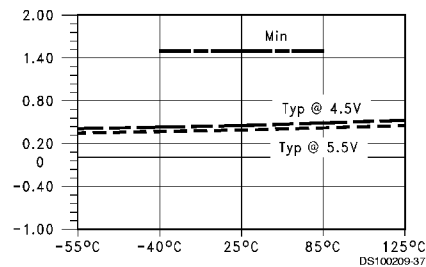
DS100209-35

t_{SET} LOW vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
Bus to Clock



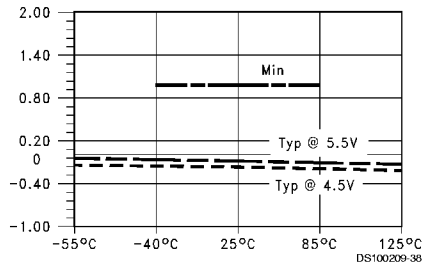
DS100209-36

t_{SET} HIGH vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
Bus to Clock



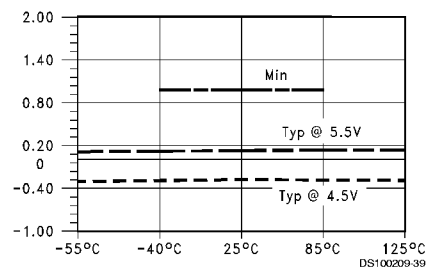
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t_{HOLD} LOW vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
Bus to Clock



DS100209-38

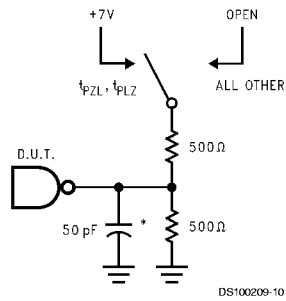
t_{HOLD} HIGH vs Temperature (T_A)
 $C_L = 50\text{ pF}$, 1 Output Switching
Bus to Clock



DS100209-39

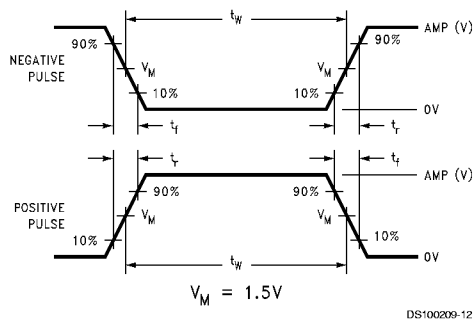
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

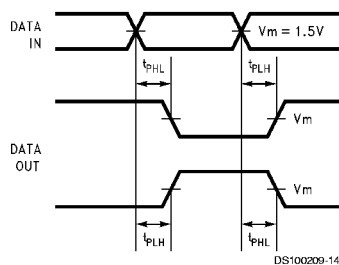
FIGURE 5. Standard AC Test Load



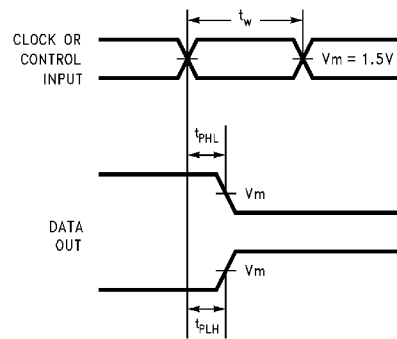
**FIGURE 6. Test Input Signal Levels
Input Pulse Requirements**

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

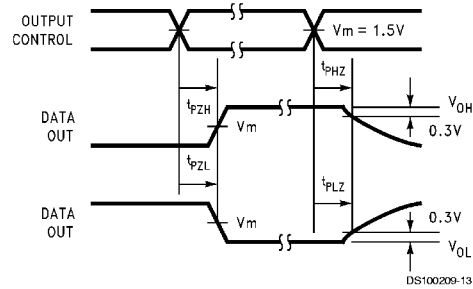
FIGURE 7. Test Input Signal Requirements



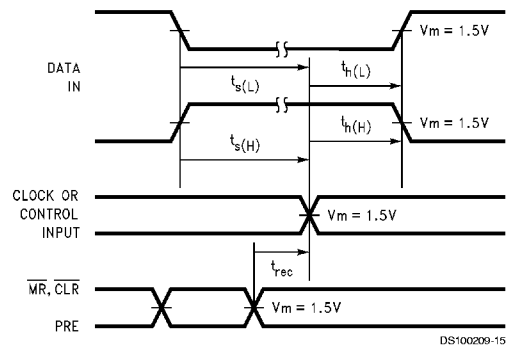
**FIGURE 8. Propagation Delay Waveforms for Inverting
and Non-Inverting Functions**



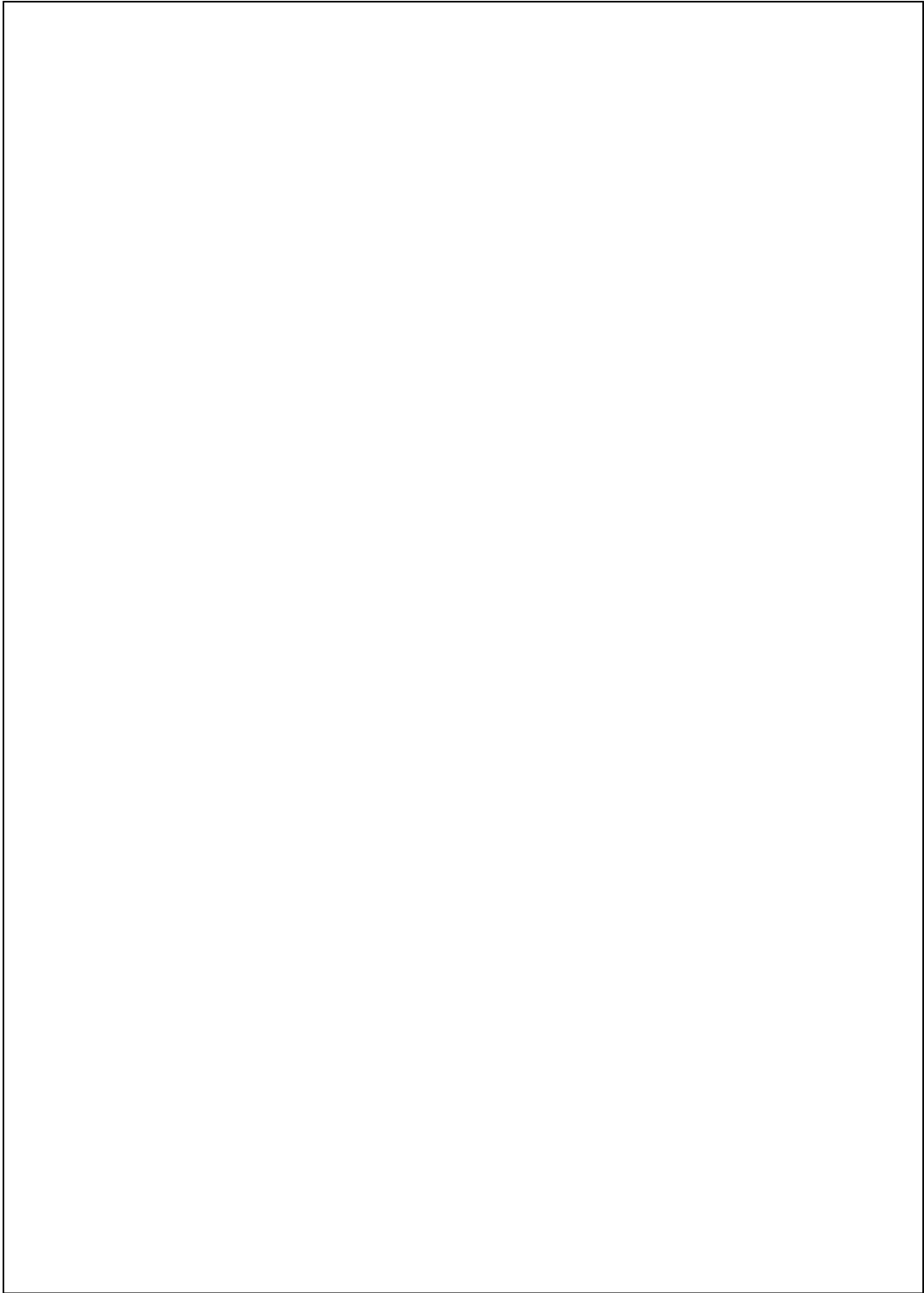
**FIGURE 9. Propagation Delay,
Pulse Width Waveforms**



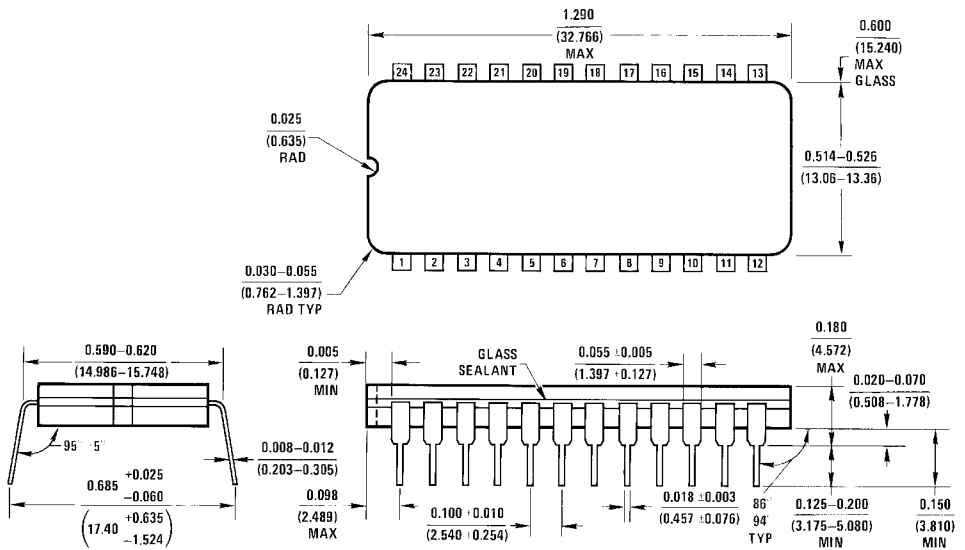
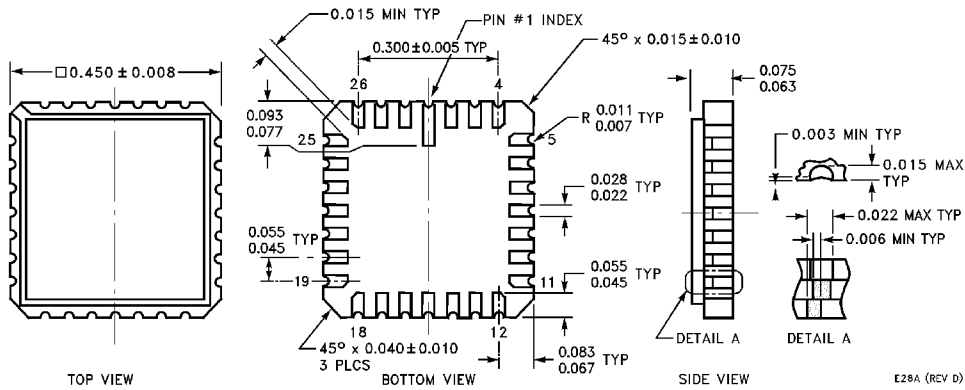
**FIGURE 10. TRI-STATE Output HIGH
and LOW Enable and Disable Times**



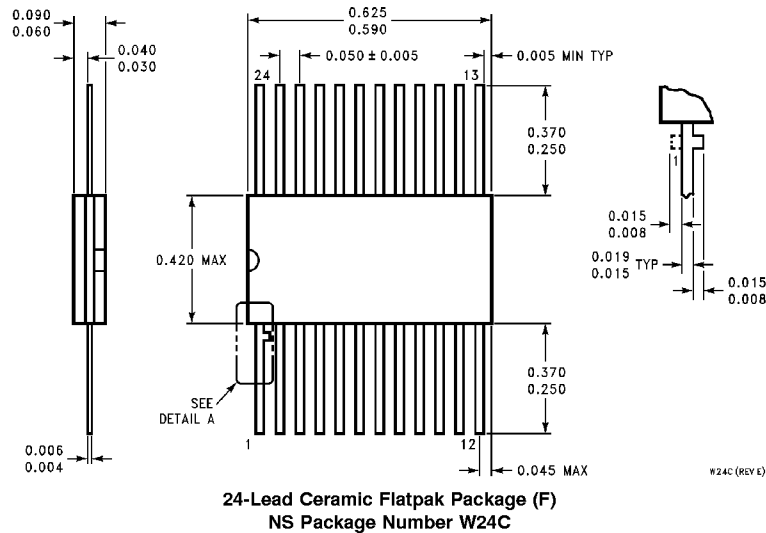
**FIGURE 11. Setup Time, Hold Time
and Recovery Time Waveforms**



Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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