

APX4 DEVELOPMENT KIT

DATA SHEET

Thursday, 22 November 2012

Version 0.6



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VERSION HISTORY

| Version | Comment |
|---------|----------------------------------|
| 0.6 | Updated pictures and fixed style |
| 0.5 | Renamed to development kit |
| 0.4 | Added pictures of display board |
| 0.3 | Added pictures |
| 0.2 | Second draft |
| 0.1 | First draft |

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DESCRIPTION

The Bluegiga APx4 is a small form factor, low power system-on-module that includes the latest wireless connectivity standards: 802.11 b/g/n and *Bluetooth* 4.0. APx4 is based on Freescale's i.MX28 processor family and runs an embedded Linux operating system based on the Yocto Project™. In addition to integrating the 454MHz ARM9 processor, the wireless connectivity technologies, Linux operating system the APx4 also includes with several built in applications, such as the 802.11 and *Bluetooth* 4.0 stacks, Continua v.1.5 compliant IEEE manager and many more. This combination provides an ideal platform for designing multi-radio wireless gateways that enables fast time-to-market and minimum R&D risks.

The Bluegiga APx4 software can be easily extended or tailored customizing the Linux operating system with applications. The motherboards for the APx4 can be easily extended to include almost anything from 3G modems to Ethernet and audio interfaces to and touch screen displays.

The Bluegiga APx4 is an ideal product for applications requiring wireless or wired connectivity technologies and the processing power of the ARM9 processor, such as health and fitness gateways, building and home automation gateways, M2M, point-of-sale and industrial connectivity.

APPLICATIONS:

- Health gateways
- M2M connectivity
- Fitness gateways
- Home and building automation
- Point-of-sale gateways
- People and asset tracking

KEY FEATURES

APx4 is a computing platform:

- 450MHz ARM9 core (Freescale i.MX28)
- 64MB RAM
- 128MB Flash
- Real Time Clock
- Linux operating system
- SO-DIMM form factor

A connectivity platform:

- *Bluetooth* 4.0 dual-mode radio
- 2.4GHz 802.11 b/g/n radio
- Wi-Fi Access Point mode
- 10/100 Ethernet
- USB 2.0 High Speed

With many extension options:

- Up to 800 x 480, 24bit display
- Resistive touch screen
- MMC/SDIO
- Multiple SPI, UART and I²C
- I²S
- PWM, GPIO and AIO

Linux operating system:

- Based on the Yocto Project(TM)
- Thousands of open source software packets available

Qualifications:

- *Bluetooth*
- CE
- FCC and IC

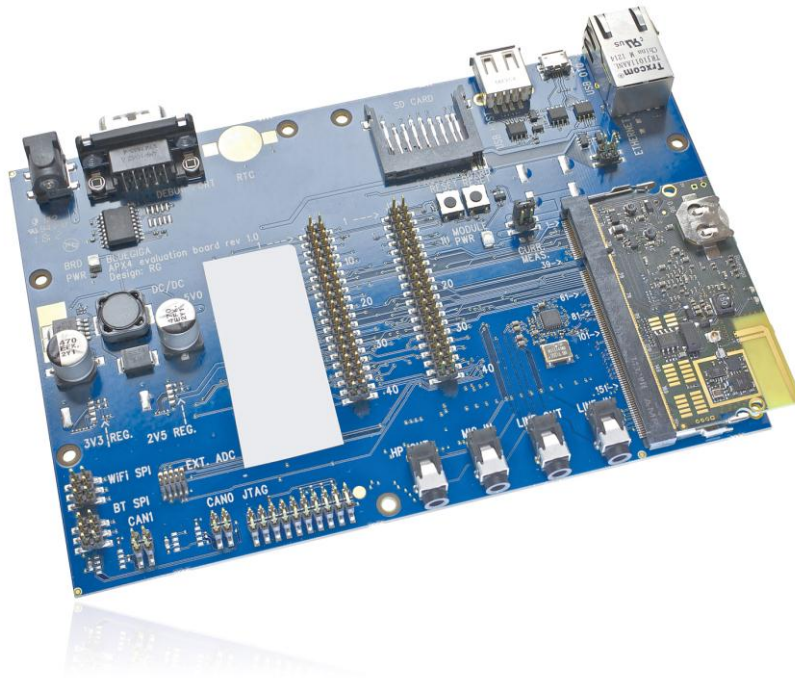


Figure 1 Development kit top view

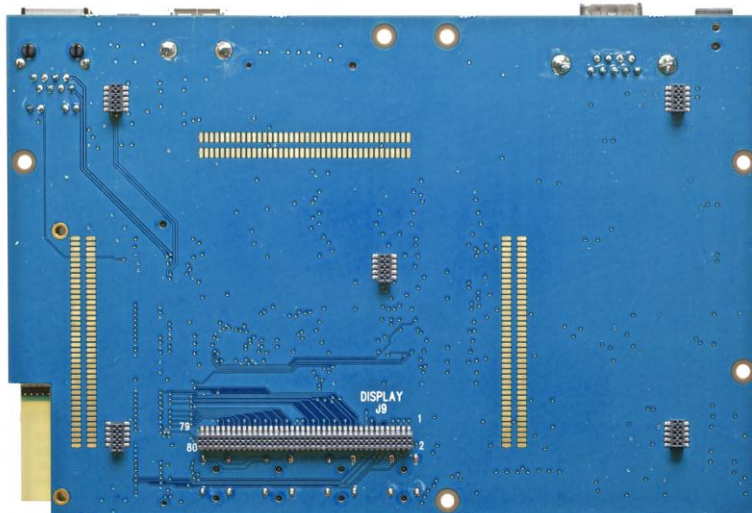


Figure 2 Development kit / mother board bottom view

1 Ordering information

| Product code | CPU and memories | Connectivity | Antenna | Temperature range |
|--------------|-------------------------------------|-------------------|----------|-------------------|
| APX4-DEVKIT | i.MX283 64MB DDR2 128MB Flash | Bluetooth + Wi-Fi | Internal | -10 – 50°C |

2 Technical data

| Power supply input range | 6V-24V DC |
|--------------------------|--|
| Power supply polarity | + in center |
| Size | 180 x 120mm |
| Power consumption* | Idle: 0.9W, Boot: 1.25W, WiFi Tx: 1.8W |

- Power drawn from the USB port and power to display is excluded
- Any power supply can be used as long as the input range and polarity are correct, but we recommend using the one supplied with the development kit.
 - In case you are using your own power supply, please check the polarity of the power supply. Positive voltage is in center. ***Incorrect polarity will damage the board.***

Note: The current measurement header must have a jumper installed in order to supply voltage to APx4.

3 Development kit

3.1 APx4 Development kit contents

- 1 x Bluegiga APx4 module
- 1 x Bluegiga APx4 mother board
- 1 x 12V power supply
- 1 x RS232 cable
- 1 x Ethernet cable
- 1 x Micro USB cable
- Documentation

3.2 Mother board functions

- +12V to +5V switch mode power supply feeding APx4
- SGTL5000 stereo codec with headphone amplifier
- Headers for all signals that are not connected to peripherals
- Connectors for
 - Ethernet
 - USB host
 - USB OTG
 - SD card
 - Analog audio in/out
 - Debug RS232 port
 - Power
- Sockets for additional display board

4 Mother board interfaces

- DC input 12V
- RS-232 debug port w/o flow control
- SDIO
- USB host
- USB On-The-Go (OTG)
- Ethernet 10Base-T/100Base-TX IEEE 802.3
- Socket for APx4
- Audio Line input
- Audio Line output
- Microphone input
- Headphone output (stereo)
- JTAG header
- 2x CAN header (can drivers Mounted=FALSE)
- Bluetooth SPI
- Wi-Fi SPI
- CPU Reset Button
- Factory Reset Button
- 1.27mm sockets for display board on bottom
- Header for current measurement

5 SO-DIMM Receptacle for APx4

Suitable receptacles are available from multiple vendors. For example TE Connectivity part number 1473005-1 is used on the development kit. Digi-Key's part number is A99605-ND.

PCB footprint and schematic symbol for the mentioned part number will be available for download for customers. The format is Mentor Graphics' PADS format.

6 Debug port

The evaluation board has a DB9 male connector which is connected to APx4's debug port. Between APx4 and the DB9 there is an RS-232 driver.

| Pin# | Net name |
|--------------|----------------|
| Baud rate | 115.200 baud/s |
| Data bits | 8 |
| Parity | None |
| Stop bits | 1 |
| Flow control | None |

Table 1 Debug port parameters

| Pin# | Net name | Function | Direction |
|------|----------|----------------------------|-----------------|
| 2 | DUART_TX | Debug UART, APx4's Tx line | From APx4 to PC |
| 3 | DUART_RX | Debug UART, APx4's Rx line | From PC to APx4 |
| 5 | GND | Ground | - |

Table 2 Debug port pins

See development kit's schematic for more details.

7 Header J6

| Pin# | Function | Pin # | Function |
|------|-------------|-------|--|
| 1 | GND | 2 | BOOTMODE FLOAT: Boot from NAND L: Boot from UART/USB |
| 3 | GND | 4 | BT_SPI_PCM1N |
| 5 | SPDIF | 6 | BT_PCM1_IN_MOSI |
| 7 | I2C0_SDA | 8 | BT_PCM1_OUT_MISO |
| 9 | I2C0_SCL | 10 | BT_PCM1_SYNC_CSN |
| 11 | PWM3 | 12 | BT_PCM1_CLK_CLK |
| 13 | PWM4 | 14 | BT_PIO7 |
| 15 | SSP2_MOSI | 16 | BT_PIO8 |
| 17 | SSP2_MISO | 18 | BT_PIO9 |
| 19 | SSP2_SCK | 20 | BT_PIO25 |
| 21 | SSP2_SS0 | 22 | SAIF0_MCLK_HDR |
| 23 | GPMI_RDY2 | 24 | SAIF1_SDATA0 |
| 25 | GPMI_RDY3 | 26 | SAIF0_SDATA0 |
| 27 | GPMI_CE2N | 28 | SAIF0_BITCLK |
| 29 | GPMI_CE3N | 30 | SAIF0_LRCLK |
| 31 | LRADC0 | 32 | INT_EXT_RTC_N |
| 33 | LRADC1 | 34 | HSADC0 |
| 35 | DEBUG | 36 | 3V3 |
| 37 | 3V3 | 38 | 3V3 |
| 39 | PSWITCH_OUT | 40 | GND |

Table 3 Debug port pins

8 Header J20

| Pin# | Function | Pin # | Function |
|------|------------------|-------|----------------|
| 1 | LCD_D0 | 2 | Pull-up to 3V3 |
| 3 | LCD_D1 | 4 | Pull-up to 3V3 |
| 5 | Pull-down to GND | 6 | LCD_D2 |
| 7 | LCD_D3 | 8 | Pull-up to 3V3 |
| 9 | LCD_D4 | 10 | Pull-up to 3V3 |
| 11 | SDIO_DAT1_OUT | 12 | |
| 13 | SDIO_DAT0_OUT | 14 | |
| 15 | SDIO_CLK_OUT | 16 | |
| 17 | SDIO_CMD_OUT | 18 | |
| 19 | SDIO_DAT3_OUT | 20 | |
| 21 | SDIO_DAT2_OUT | 22 | |
| 23 | AUART0_TX | 24 | |
| 25 | AUART0_CTS | 26 | VBATTERY |
| 27 | AUART0_RX | 28 | VBACKUP |
| 29 | AUART0_RTS | 30 | 1V4_CPU |
| 31 | PWM0_DUART_RX | 32 | 1V8 |
| 33 | PWM1_DUART_TX | 34 | 3V3_MODULE |
| 35 | | 36 | 4V2_CPU |
| 37 | | 38 | 5V0 |
| 39 | GND | 40 | GND |

Table 4 Debug port pins

9 Boot mode select on J20

The four upper rows on J20 determine APx4's boot mode by using jumpers according to following table:

| | | Jumper1 | Jumper2 | Jumper3 | Jumper4 |
|-----------|------|---------|---------|---------|---------|
| Boot mode | Pins | 1-2 | 3-4 | 5-6 | 7-8 |
| NAND | | 0 | 0 | 0 | 0 |
| SD Card | | 1 | 0 | 1 | 1 |
| USB OTG | | 0 | 0 | 1 | 0 |
| JTAG | | 0 | 1 | 0 | 0 |

Table 5 APx4 boot mode

Remove all jumpers for ordinary boot from NAND flashed in factory.

10 Module pins

Note: Signals/nets marked with a star (*) are not present on standard version

| Pin# | Default function | Net name |
|------|-------------------------|-------------|
| 1 | 5V input | VIN |
| 2 | 5V input | VIN |
| 3 | 5V input | VIN |
| 4 | 5V input | VIN |
| 5 | Battery input/output | VBATTERY |
| 6 | Battery input/output | VBATTERY |
| 7 | Battery input/output | VBATTERY |
| 8 | Bootmode | BOOTMODE |
| 9 | 3.3V output | 3V3 |
| 10 | 3.3V output | 3V3 |
| 11 | 3.3V output | 3V3 |
| 12 | 3.3V output | 3V3 |
| 13 | RTC battery | VBACKUP |
| 14 | PS switch | PSWITCH_OUT |
| 15 | NC | NC |
| 16 | NC | NC |
| 17 | Reset in - Master reset | RESETN |
| 18 | Ground | GND |

Table 6 Main power pins

| Pin# | Default function | Net name |
|------|------------------|-----------|
| 19 | Ethernet TX - | ETN_TXN |
| 20 | GND | GND |
| 21 | Ethernet TX + | ETN_TXP |
| 22 | 3.3V output | 3V3 |
| 23 | Ethernet RX - | ETN_RXN |
| 24 | Ethernet LED | #ETN_LED1 |
| 25 | Ethernet RX + | ETN_RXP |
| 26 | GND | GND |

Table 7 Ethernet

| Pin# | Default function | Net name |
|------|--------------------------|----------|
| 27 | USB External VBUS enable | SPDIF* |
| 28 | | NC |
| 29 | USB D- | USB1DM |
| 30 | | NC |
| 31 | USB D+ | USB1DP |
| 32 | Ground | GND |

Table 8 USB Host

| Pin# | Default function | Net name |
|------|------------------|----------|
| 33 | USB OTG id | USB0_ID |
| 34 | | NC |
| 35 | USB D- | USB0DM |
| 36 | | NC |
| 37 | USB D+ | USB0DP |
| 38 | | NC |
| 39 | Ground | GND |

Table 9 USB On-the-go

| Pin# | Default function | Net name |
|------|------------------------|----------|
| 40 | I ² C Data | I2C0_SDA |
| 41 | I ² C Clock | I2C0_SCL |

Table 10 I²C 0

| Pin# | Default function | Net name |
|------|------------------|----------|
| 42 | PWM (Backlight) | PWM4 |
| 43 | Status led | PWM3 |

Table 11 Dedicated PWMs

| Pin# | Default function | Net name |
|------|--------------------------------|----------------|
| 44 | Slave select 1 | SDIO_DAT1_OUT* |
| 45 | Slave select 2 | SDIO_DAT2_OUT* |
| 46 | Command - Master out, slave in | SDIO_CMD_OUT* |
| 47 | Data 0, Master in, slave out | SDIO_DAT0_OUT* |
| 48 | Clock | SDIO_CLK_OUT* |
| 49 | Ready - Slave select 0 | SDIO_DAT3_OUT* |
| 50 | Ground | GND |

Table 12 SSP2 – SDIO/MMC/SPI

| Pin# | Default function | Net name |
|------|------------------|-------------|
| 51 | Card detect | SSP0_DETECT |
| 52 | Data 0 | SSP0_DATA0 |
| 53 | Data 1 | SSP0_DATA1 |
| 54 | Data 2 | SSP0_DATA2 |
| 55 | Data 3 | SSP0_DATA3 |
| 56 | Command | SSP0_CMD |
| 57 | Clock | SSP0_SCK |
| 58 | Ground | GND |

Table 13 SSP0 - SDIO/MMC/SPI

| Pin# | Default function | Net name |
|------|----------------------|------------|
| 59 | UART transmit | AUART0_TX |
| 60 | UART receive | AUART0_RX |
| 61 | UART clear-to-send | AUART0_CTS |
| 62 | UART request-to-send | AUART0_RTS |

Table 14 UART 0

| Pin# | Default function | Net name |
|------|------------------|-----------|
| 63 | UART transmit | SSP2_MOSI |
| 64 | UART receive | SSP2_SCK |
| 65 | | NC |
| 66 | | NC |

Table 15 UART 2

| Pin# | Default function | Net name |
|------|--|-----------|
| 67 | UART transmit and USB OTG power enable | SSP2_SS0 |
| 68 | UART receive and USB HOST power enable | SSP2_MISO |
| 69 | | NC |
| 70 | | NC |
| 71 | Ground | GND |

Table 16 UART 3

| Pin# | Default function | Net name |
|------|------------------|----------|
| 72 | Bluetooth GPIO | BT_PIO7 |
| 73 | Bluetooth GPIO | BT_PIO8 |
| 74 | Bluetooth GPIO | BT_PIO9 |
| 75 | Bluetooth GPIO | BT_PIO25 |

Table 17 Bluetooth GPIO

| Pin# | Default function | Net name |
|------|------------------|------------|
| 76 | CAN 0 transmit | GPMI_RDY2* |
| 77 | Ground | GND |
| 78 | CAN 1 transmit | GPMI_CE2N* |
| 79 | CAN 1 receive | GPMI_CE3* |
| 80 | Ground | GND |
| 81 | CAN 0 receive | GPMI_RDY3* |
| 82 | Ground | GND |

Table 18 CAN

| Pin# | Default function | Net name |
|------|------------------|--------------|
| 83 | MCLK | SAIF0_MCLK |
| 84 | Data line 1 | SAIF1_SDATA0 |
| 85 | Data line 0 | SAIF0_SDATA0 |
| 86 | Bit clock | SAIF0_BITCLK |
| 87 | Left/Right clock | SAIF0_LRCLK |
| 88 | GND | GND |

Table 19 Primary audio / UART 4

| Pin# | Default function | Net name |
|------|------------------|----------|
| 89 | | NC |
| 90 | | NC |
| 91 | | NC |
| 92 | | NC |
| 93 | | NC |
| 94 | Ground | GND |
| 95 | | NC |
| 96 | | NC |
| 97 | | NC |
| 98 | | NC |
| 99 | | NC |
| 100 | | NC |

Table 20 Reserved group 1

| Pin# | Default function | Net name |
|------|------------------|----------|
| 101 | | NC |
| 102 | Ground | GND |
| 103 | | NC |
| 104 | | NC |
| 105 | | NC |
| 106 | | NC |
| 107 | 1.4V output | 1V4_CPU |
| 108 | 1.8V output | 1V8 |
| 109 | 4.2V output | 4V2_CPU |
| 110 | | NC |
| 111 | | GND |
| 112 | | NC |
| 113 | | NC |
| 114 | | NC |
| 115 | | NC |
| 116 | Ground | GND |

Table 21 Reserved group 2

| Pin# | Default function | Net name |
|------|------------------|----------|
| 117 | Data 0 | LCD_D0 |
| 118 | Data 1 | LCD_D1 |
| 119 | Data 2 | LCD_D2 |
| 120 | Data 3 | LCD_D3 |
| 121 | Data 4 | LCD_D4 |
| 122 | Data 5 | LCD_D5 |
| 123 | Data 6 | LCD_D6 |
| 124 | Data 7 | LCD_D7 |
| 125 | Data 8 | LCD_D8 |
| 126 | Data 9 | LCD_D9 |
| 127 | Data 10 | LCD_D10 |
| 128 | Data 11 | LCD_D11 |
| 129 | Ground | GND |
| 130 | Data 12 | LCD_D12 |
| 131 | Data 13 | LCD_D13 |
| 132 | Data 14 | LCD_D14 |
| 133 | Data 15 | LCD_D15 |
| 134 | Data 16 | LCD_D16 |
| 135 | Data 17 | LCD_D17 |
| 136 | Data 18 | LCD_D18 |
| 137 | Data 19 | LCD_D19 |
| 138 | Data 20 | LCD_D20 |
| 139 | Data 21 | LCD_D21 |
| 140 | Data 22 | LCD_D22 |
| 141 | Data 23 | LCD_D23 |
| 142 | Ground | GND |

Table 22 LCD data lines

| Pin# | Default function | Net name |
|------|------------------|------------|
| 143 | Horizontal Sync | LCD_WR_RWN |
| 144 | Vertical Sync | LCD_RD_E |
| 145 | LCD Enable | LCD_CS |
| 146 | Dot clock | LCD_RS |
| 147 | Ground | GND |

Table 23 LCD control lines

| Pin# | Function | Net name |
|------|---------------------------|---|
| 148 | Debug UART RX or I2C1_SDA | PWM0 (also connected to PTH pins on right side) |
| 149 | Debug UART TX or I2C1_SCL | PWM1 (also connected to PTH pins on right side) |
| 150 | LCD reset / GPIO | LCD_RESET |
| 151 | | NC |

Table 24 Debug UART / PWM / I2C1 / GPIO

| Pin# | Function | Net name |
|------|---------------|----------|
| 152 | | NC |
| 153 | | NC |
| 154 | | NC |
| 155 | | NC |
| 156 | | NC |
| 157 | | NC |
| 158 | | NC |
| 159 | Ground | GND |
| 160 | Ground | GND |
| 161 | | NC |
| 162 | | NC |
| 163 | Ground | GND |
| 164 | Ground | GND |
| 165 | | NC |
| 166 | | NC |
| 167 | Ground | GND |
| 168 | Ground | GND |
| 169 | | NC |
| 170 | WiFi Activity | WIFI_ACT |
| 171 | Ground | GND |

Table 25 Reserved group 3

| Pin# | Function | Net name |
|------|--|---------------|
| 172 | Wi-Fi Debug SPI - MISO | SPI_WIFI_MISO |
| 173 | Wi-Fi Debug SPI – CLK | SPI_WIFI_CLK |
| 174 | Wi-Fi Debug SPI – MOSI | SPI_WIFI_MOSI |
| 175 | Wi-Fi Debug SPI - CS | SPI_WIFI_CS |
| 176 | RTC interrupt | INT_EXT_RTC_N |
| 177 | Factory reset button / JTAG return clock | JTAG_RTCK |
| 178 | JTAG test clock | JTAG_TCK |
| 179 | JTAG test data in | JTAG_TDI |
| 180 | JTAG test data out | JTAG_TDO |
| 181 | JTAG test mode state | JTAG_TMS |
| 182 | JTAG test reset | JTAG_TRST |
| 183 | Ground | GND |
| 184 | JTAG enable boundary scan | DEBUG |

Table 26 Misc

| Pin# | Function | Net name |
|------|------------------------|----------|
| 185 | Touch controller XN | LRADC4 |
| 186 | Touch controller XP | LRADC2 |
| 187 | Touch controller YN | LRADC5 |
| 188 | Touch controller YP | LRADC3 |
| 189 | Touch controller WIPER | LRADC6 |
| 190 | Generic ADC 0 | LRADC0 |
| 191 | Generic ADC 1 | LRADC1 |
| 192 | High speed ADC | HSADC0 |
| 193 | Ground | GND |
| 194 | Ground | GND |

Table 27 ADC

| Pin # | Function | Net name |
|-------|------------------------|--------------|
| 195 | Bluetooth debug enable | BT_SPI_PCM1N |
| 196 | PCM in | BT_PCM1_IN |
| 197 | PCM out | BT_PCM1_OUT |
| 198 | PCM clock | BT_PCM1_CLK |
| 199 | PCM sync | BT_PCM1_SYNC |
| 200 | Ground | GND |

Table 28 Bluetooth audio

Contact Information

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