3W Stereo Class-D Audio Power Amplifier with DC Volume Control

General Description

The RT9104 is a stereo, high efficiency, filter free Class-D audio amplifier capable of delivering 3W per channel into 3Ω speakers. For application flexibility, the gain can be set by external DC volume control. Thermal protection as well as overcurrent protection functions are included in the stereo amplifier. The SOP-16 packaging without additional heat sink makes the RT9104 Class-D amplifier an ideal choice for monitor applications. The RT9104 is also well suited for battery powered applications because of its operating voltage (from 4.5V to 5.5V) and very low shutdown current.

The RT9104 is available in WQFN-16L 3x3, SOP-16 and DIP-16 packages.

Ordering Information

RT9104 □ □

- Package Type
  - QW : WQFN-16L 3x3 (W-Type)
  - S : SOP-16
  - N : DIP-16
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

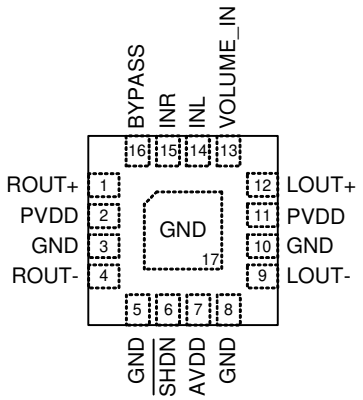
- **4.5V to 5.5V Input Supply Range**
- **3W Per Channel into 3Ω Speakers (THD+N = 10%)**
- **300kHz High Internal Switching Frequency**
- **Efficiency Greater than 85%**
- **DC Volume Control from –70dB to 20dB**
- **Fade In at Enable and Power On**
- **Thin 16-Lead WQFN and SOP-16 and DIP-16 Packages**
- **RoHS Compliant and Halogen Free**

Applications

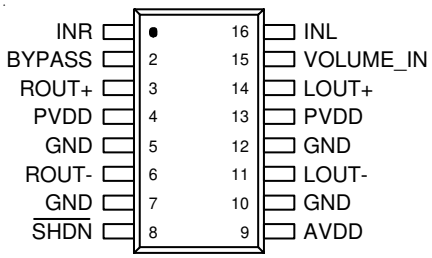
- LCD Monitors
- Consumer Device
- Powered Speakers

Pin Configurations

(TOP VIEW)



WQFN-16L 3x3



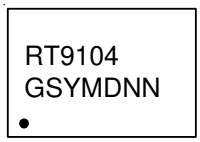
SOP-16/DIP-16

Marking Information

RT9104GQW

GU= : Product Code
YMDNN : Date Code

RT9104GS



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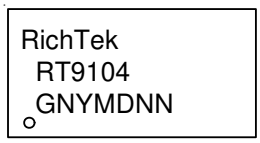
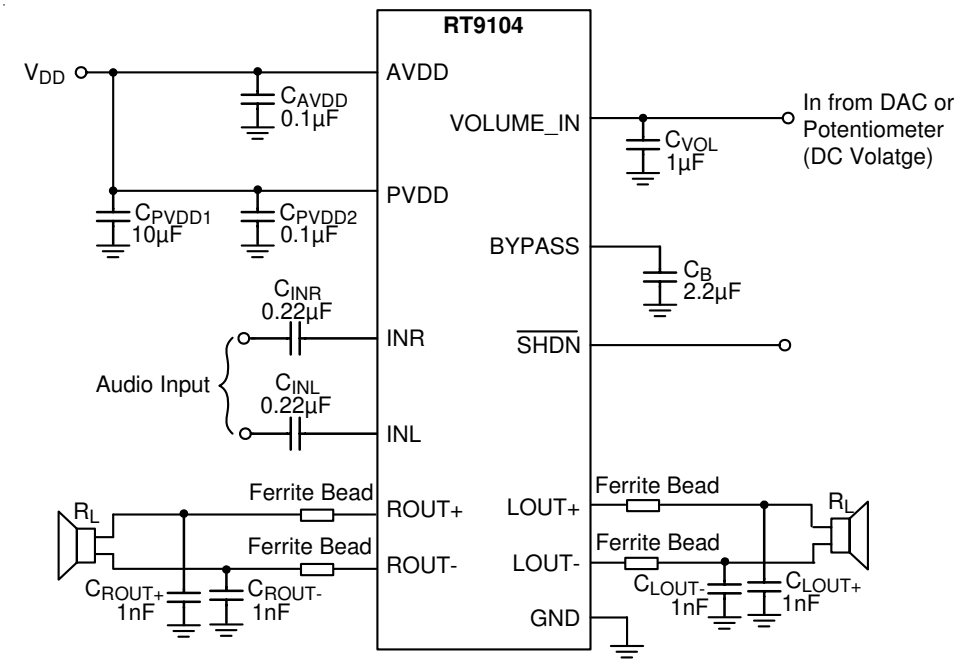
RT9104GN



RT9104GN : Product Number
YMDNN : Date Code

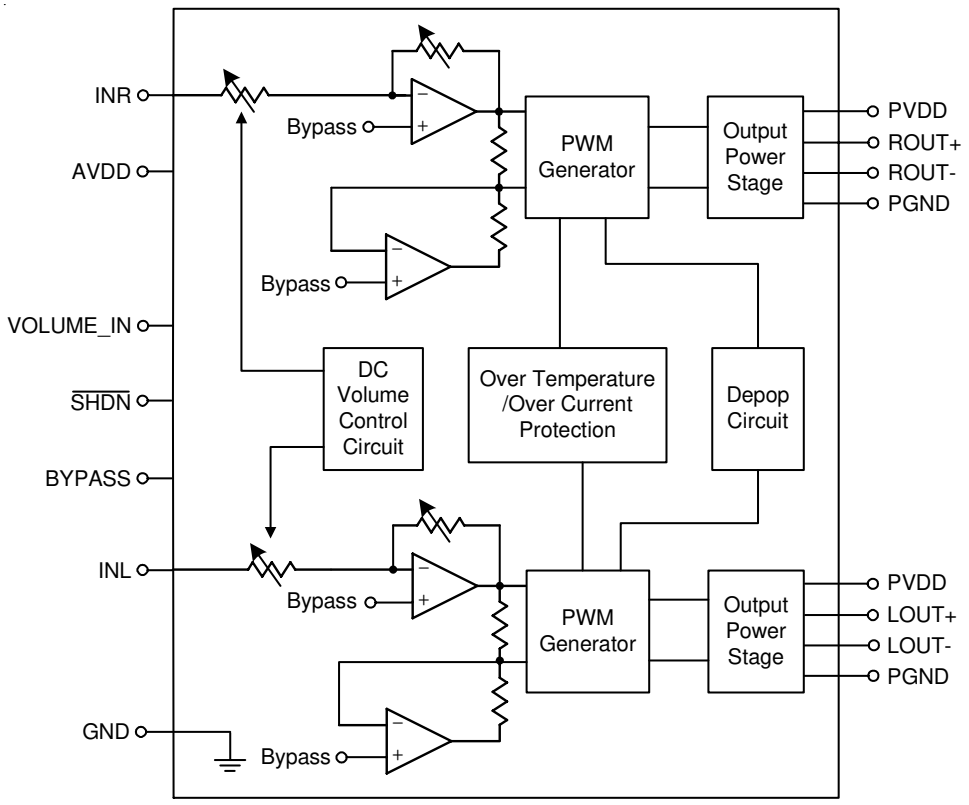
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-16/DIP-16	WQFN-16L 3x3		
1	15	INR	Right Channel Audio Signal Input.
2	16	BYPASS	Common Mode Voltage Output.
3	1	ROUT+	Positive Right Channel BTL Output.
4, 13	2, 11	PVDD	Power Supply.
5, 7, 10, 12	3, 10, 5, 8, 17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	4	ROUT−	Negative Right Channel BTL Output.
8	6	$\overline{SHDN}$	Shutdown Pin, Enable when $\overline{SHDN}$ = '1', Disable when $\overline{SHDN}$ = '0'.
9	7	AVDD	Analog Reference Input Voltage. Connect to a regulator output voltage as better.
11	9	LOUT−	Negative Left Channel BTL Output.
14	12	LOUT+	Positive Left Channel BTL Output.
15	13	VOLUME_IN	Volume Control Pin. DC in for controlling volume.
16	14	INL	Left Channel Audio Signal Input.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, AVDD, PVDD ---------- 0.3V to 6V
- Input Voltage, INL, INR ---------- 0.3V to (V_{DD} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 1.471W
  - SOP-16 ---------- 1.176W
  - DIP-16 ---------- 1.333W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
  - SOP-16, θ_{JA} ---------- 85°C/W
  - DIP-16, θ_{JA} ---------- 75°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage Range, AVDD, PVDD ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, Gain = 6dB, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Threshold		V_{UVLO}	V_{DD} Rising	--	4	--	V
V_{DD} Under Voltage Lockout Hysteresis				--	100	--	mV
$\overline{SHDN}$ Input Threshold Voltage	Logic-High	V_{IH}		2	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Quiescent Current		I_Q	V_{DD} = 5.5V, No Load ,	--	3	--	mA
Shutdown Current		I_{SHDN}	$V_{\overline{SHDN}}$ = 0V, V_{DD} = 4.5 V to 5.5V	--	--	10	μA
Output Impedance in $\overline{SHDN}$			$V_{\overline{SHDN}}$ = 0V	--	>1	--	kΩ
Switching Frequency		f_{SW}	V_{DD} = 4.5V to 5.5V	--	300	--	kHz
Resistance from Shutdown to GND				20	--	--	kΩ
Thermal Shutdown		T_{SD}		130	150	170	°C

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Power (Per Channel)	P_O	THD+N = 10%, f = 1kHz, R_L = 3Ω	--	3	--	W
		THD+N = 1%, f = 1kHz, R_L = 3Ω	--	2.35	--	
		THD+N = 10%, f = 1kHz, R_L = 4Ω	--	2.7	--	
		THD+N = 1%, f = 1kHz, R_L = 4Ω	--	2.3	--	
		THD+N = 10%, f = 1kHz, R_L = 8Ω	--	1.6	--	
		THD+N = 1%, f = 1kHz, R_L = 8Ω	--	1.25	--	
Total Harmonic Distortion Plus Noise	THD+N	P_O = 1W, R_L = 8Ω, f = 1kHz	--	0.2	--	%
Crosstalk		f = 1kHz, V_{DD} = 4.5V to 5.5V, P_O = 2W, R_L = 4Ω	--	–85	--	dB
Signal-to-Noise Ratio	SNR	P_O = 1W, R_L = 8Ω, A Weighting	--	90	--	dB
Start-Up Time from Shutdown			--	300	--	ms
Efficiency		Load = (8Ω + 33μH)	--	85	--	%

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

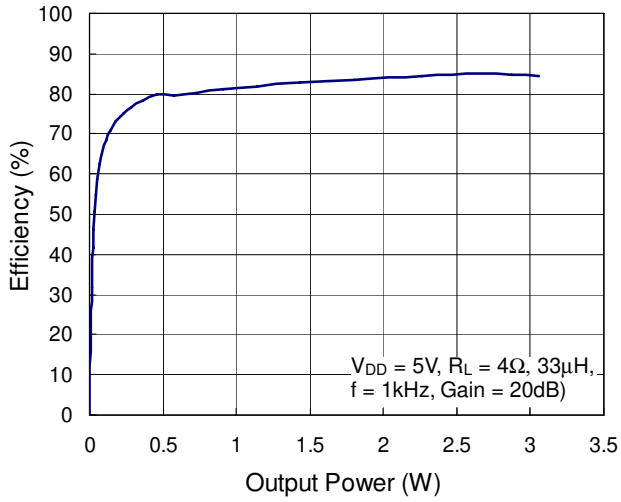
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

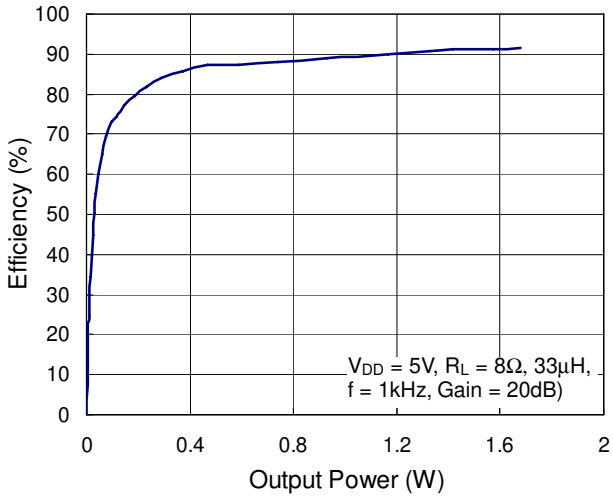
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

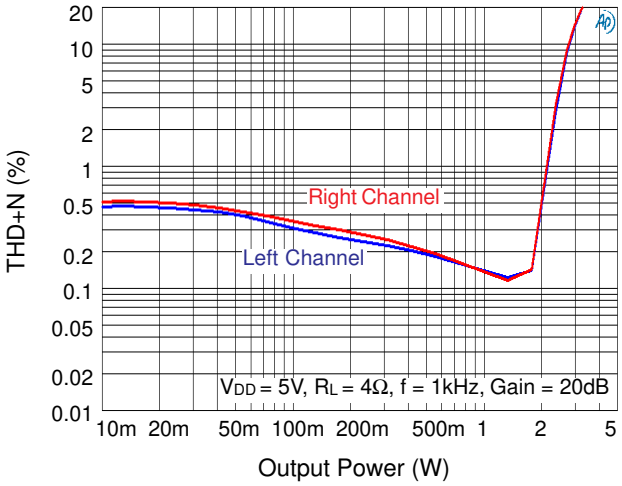
Efficiency vs. Output Power



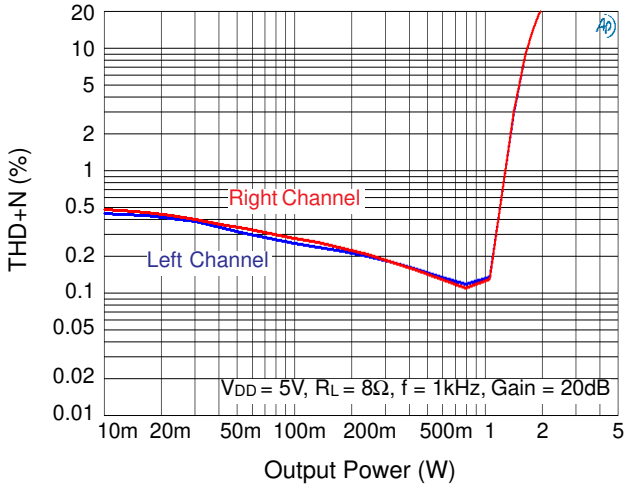
Efficiency vs. Output Power



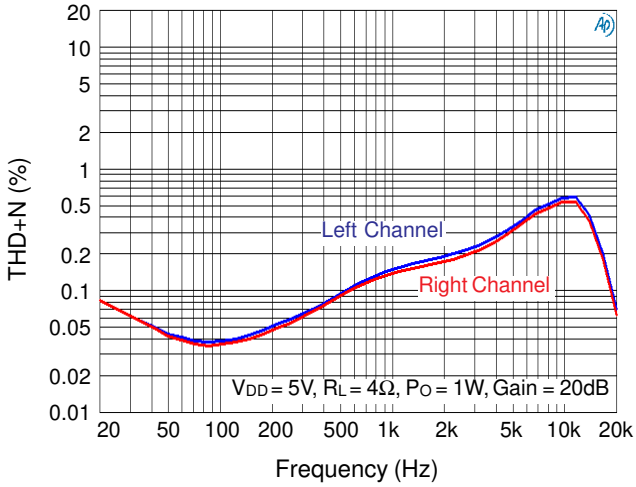
THD+N vs. Output Power



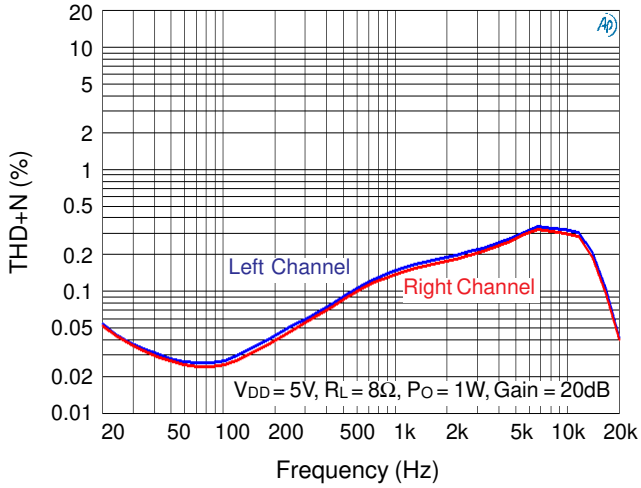
THD+N vs. Output Power



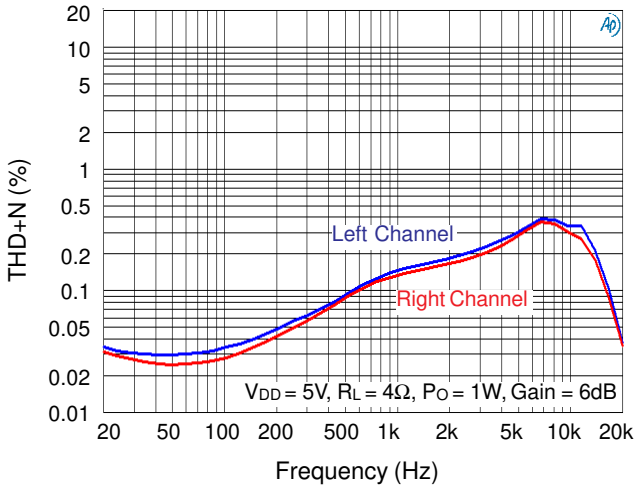
THD+N vs. Frequency



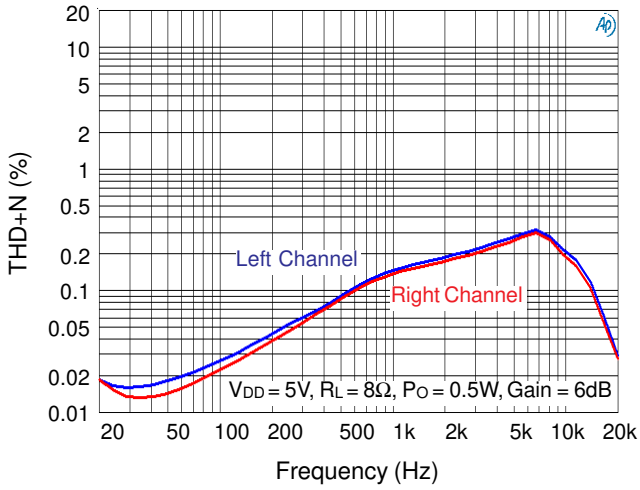
THD+N vs. Frequency



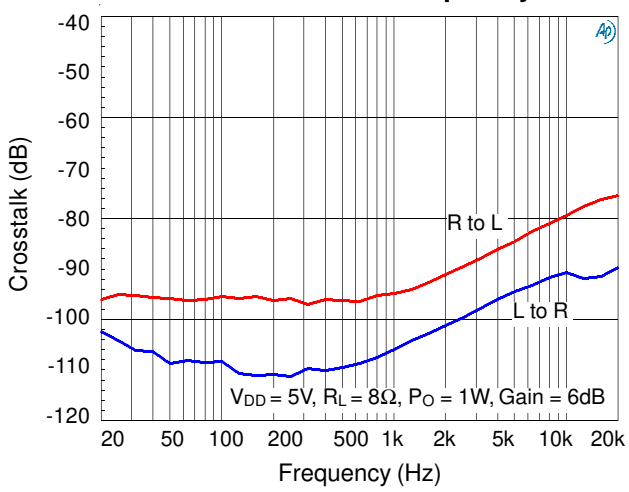
THD+N vs. Frequency



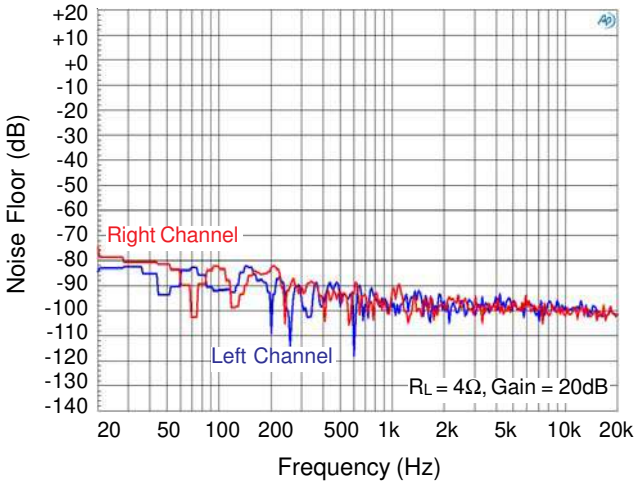
THD+N vs. Frequency



Crosstalk vs. Frequency



Noise Floor vs. Frequency



Application information

The RT9104 is a single-ended input and high efficiency Class-D stereo audio amplifier featuring low resistance internal power MOSFETs and over 85% power efficiency. It requires only a few external components with small footprints. The RT9104 also supports DC volume control from −70dB to 20dB. Therefore, it is very suitable for portable devices and LCD monitor applications. With a filter-less modulation feature, the RT9104 can limit the number of external components to a minimum.

DC Volume control

The voltage gain of RT9104 can be set by the external DC voltage through the "VOLUME_IN" pin. There are a total of 32 discrete gain steps of the amplifier with a range from −70dB to 20dB for BTL operation.

A pictorial representation of the typical volume control can be found in Figure 1.

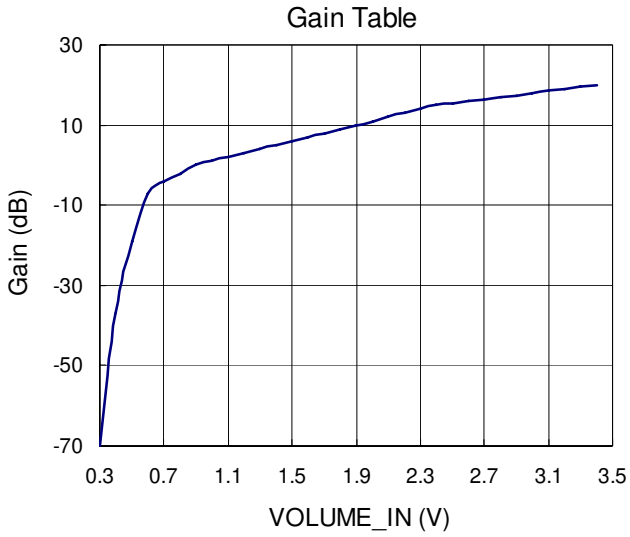


Figure 1. Typical DC Voltage Control Operation

Table 1. VOLUME_IN Voltage for Gain Control

Gain (dB)	VOLUME_IN (V)	Gain (dB)	VOLUME_IN (V)
20	3.4	9	1.8
19.5	3.3	8	1.7
19	3.2	7	1.6
18.5	3.1	6	1.5
18	3	5	1.4
17.5	2.9	4	1.3
17	2.8	3	1.2
16.5	2.7	2	1.1
16	2.6	1	1
15.5	2.5	0	0.9
15	2.4	-2	0.8
14	2.3	-4	0.7
13	2.2	-7	0.6
12	2.1	-19	0.5
11	2	-37	0.4
10	1.9	-70	0.3

Fade In

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

Decoupling Capacitor

The RT9104 is a high performance Class-D audio amplifier that requires adequate power supply decoupling to ensure high efficiency and low total harmonic distortion (THD). To filter out higher frequency transients, spikes, or digital hash on the line, a low equivalent-series-resistance (ESR) ceramic capacitor (typically 10μF), placed as close as possible to the PVDD pins will achieve the best performance. Placing this decoupling capacitor close to the RT9104 is very important, since any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering out lower frequency noise signals, a 10μF or greater capacitor can be placed near the audio power amplifier.

Short Circuit Protection

The RT9104 has short circuit protection circuitry on the outputs which prevents damage to the device during unexpected applications. When a short circuit is detected, the outputs are disabled immediately .However, once the short is removed, the device will re-activate again.

Low Supply Voltage Detection

The RT9104 incorporates circuitry designed to detect low supply voltage level. When the supply voltage falls to 4V or below, the RT9104 goes into a state of shutdown and the current consumption drops from milliamperes to microamperes. The device will resume normal function again once V_{DD} > 4.2V.

Thermal Protection

Thermal protection on the RT9104 automatically disables the outputs when the junction temperature exceeds 150°C in order to prevent damage to the device. There is a ±20 degree tolerance on this trip point from device to device. Once the temperature cools below 130°C, the device will auto-resume normal operations.

How to Reduce EMI

Most applications require a ferrite bead filter as shown in Figure 2. The ferrite filter reduces EMI of around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies and low impedance at low frequencies.

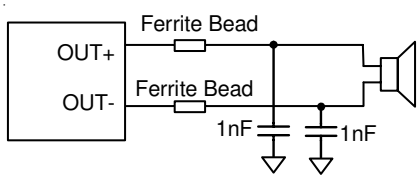


Figure 2. Typical Ferrite Chip Bead Filter

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9104, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 packages, the thermal resistance, θ_{JA}, is 68°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-16 packages, the thermal resistance, θ_{JA}, is 85° C/W on a standard JEDEC 51-7 four-layer thermal test board. For DIP-16 packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board.The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for WQFN-16L 3x3 package

$P_{D(MAX)}$ = (125°C– 25°C) / (85°C/W) = 1.176W for SOP-16 package

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for DIP-16 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9104 packages, the derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

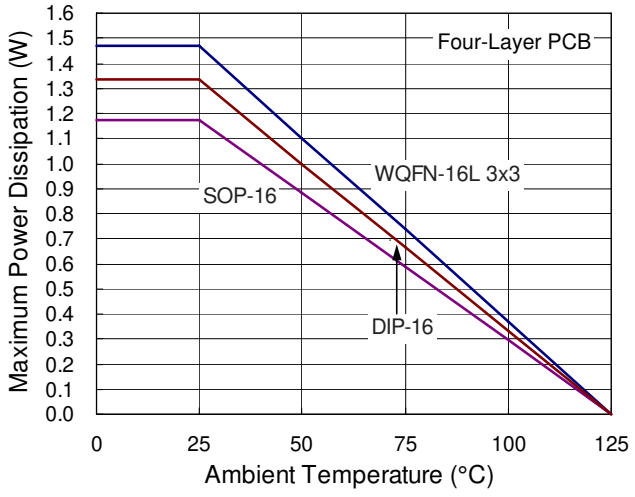


Figure 3. Derating Curves for RT9104 Package

Layout Considerations

For best performance of the RT9104, the below PCB Layout guidelines must be strictly followed.

- Place the decoupling capacitors as close as possible to the PVDD, AVDD and GND pins.
- Keep the differential output traces as wide and short as possible.
- The traces of (INR & INL) and (LOUT+ & LOUT–, ROUT+ & ROUT–) should be kept equal width and length respectively.
- Connect power sections directly to the ground plane for maximum thermal dissipation and noise protection.

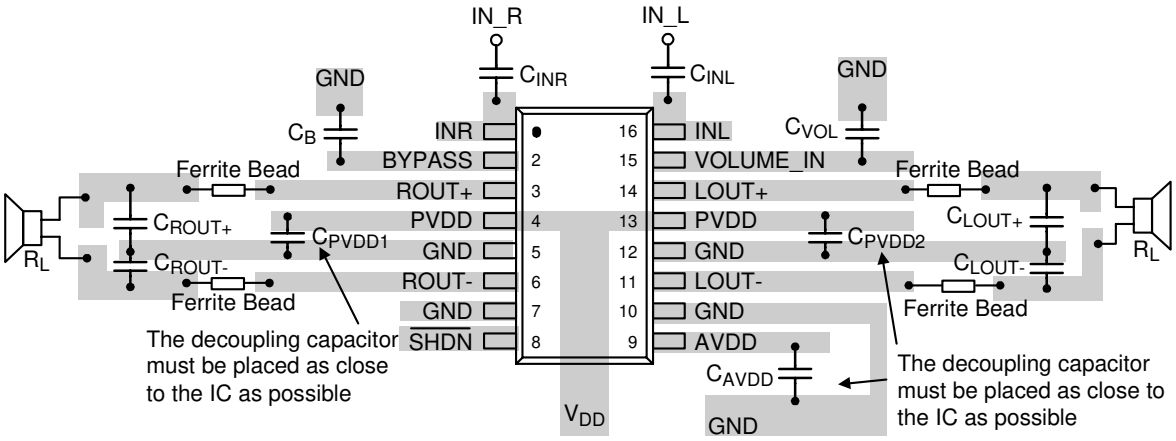
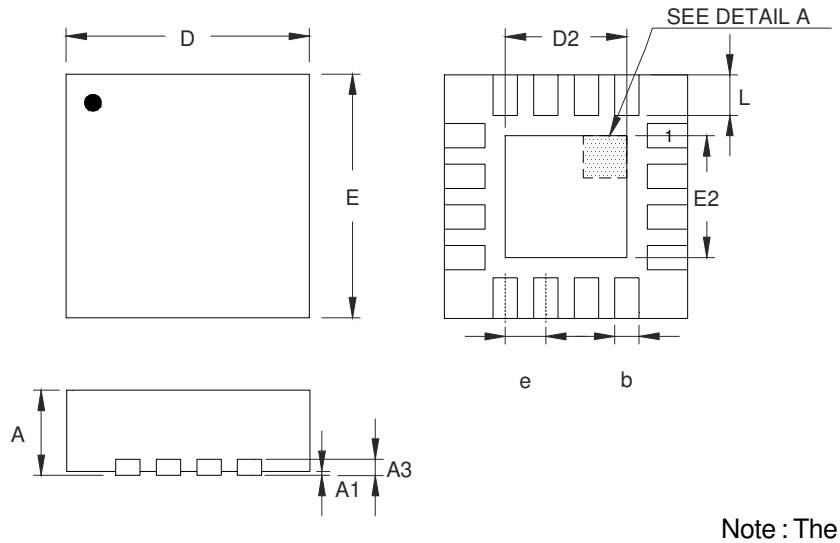
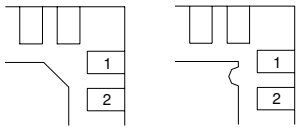


Figure 4. PCB Layout Guide

Outline Dimension





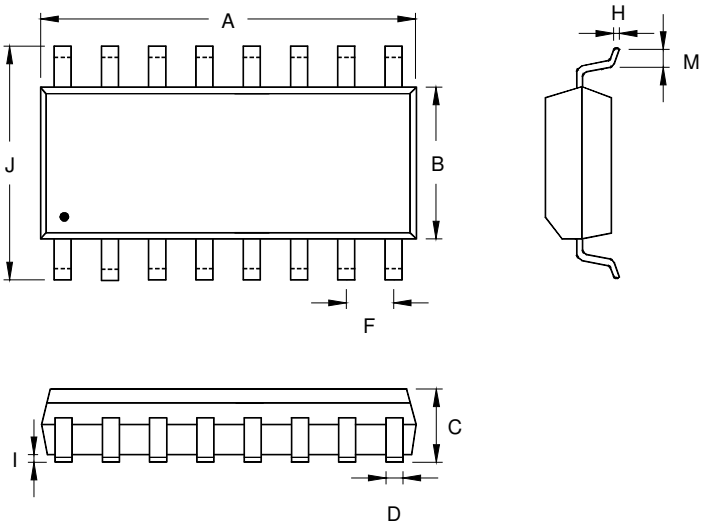
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

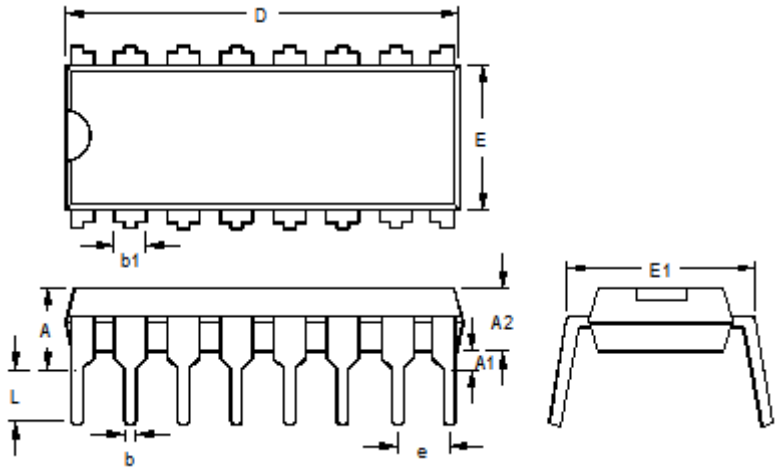
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16–Lead SOP Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.700	4.320	0.146	0.170
A1	0.381	0.710	0.015	0.028
A2	3.200	3.600	0.126	0.142
b	0.360	0.560	0.014	0.022
b1	1.143	1.778	0.045	0.070
D	18.800	19.300	0.740	0.760
E	6.200	6.600	0.244	0.260
E1	7.620	8.255	0.300	0.325
e	2.540		0.100	
L	3.000	3.600	0.118	0.142

16-Lead DIP Plastic Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com

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