TEXAS INSTRUMENTS

DAP Signal Conditioning Board

User's Guide

June 2003

Data Acquistion — Digital/Analog Converters

SLAU105

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During normal operation, some circuit components may have case temperatures greater than xxx°C. The EVM is designed to operate properly with certain components above xxx°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

The DAP Signal Conditioning Board is designed to provide general purpose signal conditioning to evaluation modules from the Data Acquisition Products-Group. This board amplifies/filters analog signals to/from a variety of A-to-D and D-to-A converters. When combined with additional sensor or amplifier boards, it can be used as part of a complete data acquisition system for a variety of applications.

How to Use This Manual

This document contains the following chapters:

Chapter 1—Introduction

Chapter 2—Analog Inputs

Chapter 3—Analog Outputs

Chapter 4—Power Supply Requirements

Chapter 5—Amplifier Configuration Options

Chapter 6—DAP Signal Conditioning Board Assembly and Board Schematics

Related Documentation From Texas Instruments

TMS320 Cross -Platform Daughtercard Specification – SPRA711

5-6K Interface Evaluation Module – SLAU104

C2000 Interface Evaluation Module - SLAU106

OPA2132, High Speed FET - Input Operational Amplifiers – OPA2132

OPA2350, High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier(TM) Series - SBOS099

REG1117-25, 800mA Low Dropout (LDO) Positive Regulator 2.5V - SBVS001

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Chapter 1

Introduction

The DAP Signal Conditioning Board provides data converter customers with a general purpose analog front/back end to Data Acquisition Products Evaluation Modules from Texas Instruments.

The signal conditioning board is compatible with the 5-6K interface board (SLAU104), the C2000 interface board (SLAU106) and the HPA449 evaluation system from SoftBaugh, Inc. (www.softbaugh.com).

The signal conditioning board provides up to eight single ended or four differential channels for use with a wide selection of data converter evaluation boards. Two fundamentally equivalent varieties using either the single supply OPA2350 or dual supply OPA2132 are available. The board contains jumpers and additional component locations which provide a variety of configuration options.

While the Signal Conditioning Board can serve as a stand-alone amplifier for many applications, its primary purpose is as an interface to data acquisition products evaluation boards. This document describes how to use the DAP Signal Conditioning Board in conjunction with the interface boards mentioned above.

Chapter 2

Analog Inputs

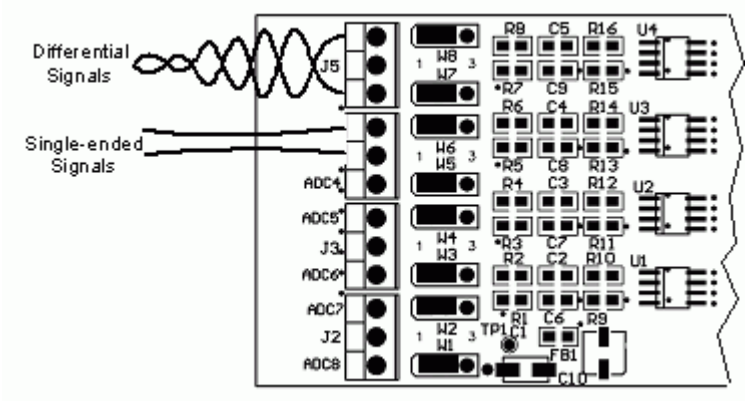
The Signal Conditioning Board provides two primary ways to apply an analog-signal to the amplifiers. The method used to apply the signal is based on whether the board is being used as an input to an analog to digital converter, or an output from a digital to analog converter.

Topic **Page**

2.1 As an Input to a Analog-to-Digital Converter EVM

Four three-terminal screw jacks (J5, J4, J3, and J2 are located on the top side of the board to provide a convenient way to attach a variety of signal sources. The screw jacks are arranged as a channel pair for the easy application of differential or single ended analog sources. Single ended sources can be applied to terminal 1 or 3, referenced to terminal 2. Differential sources can be applied between terminals 1 and 3.

Figure 2-1. Application of Analog Source to ADC



When used with an analog-to-digital converter EVM, connector J1 (bottom side of PCB) plugs into a male header located on the left edge of the interface board. In this case, J1 acts as a support/stabilization mechanism. The output from the signal conditioning board is available on J7 (top side —20 pin header, bottom side—20 pin socket). The 20-pin socket portion of J7 plugs into the analog I/O header located on the interface board.

2.2 As an Output to a Digital-to-Analog Converter EVM

The twenty pin female socket (J1) provides the analog input to the signal conditioning board when it is used in conjunction with a digital to analog converter EVM.

Connector J1 plugs onto the male analog I/O header located on the interface board. Table 2-1 shows the analog input connector pin out.

Table 2-1. Signal Conditioning Board J1 and J2-J5 Connections

Signal	Pin Number			Signal
	J1		J2-J5	
AGND	1	2	J2.1	A0
AGND	3	4	J2.3	A1
AGND	5	6	J3.1	A2
AGND	7	8	J3.3	A3
AGND	9	10	J4.1	A4
AGND	11	12	J4.3	A5
AGND	13	14	J5.1	A6
AGND	15	16	J4.3	A7
AGND	17	18		No connection
AGND	19	20		No connection

Note: AGND connections on J2 through J5 are made on pin 2 (center screw termainal)

Differential signals are typically applied across adjacent channels. For instance, a single channel, differential DAC output would connect to the A0(+) and A1(-) inputs. Check the data converter EVM User's Guide for the exact input configuration.

Chapter 3

Analog Outputs

The signal conditioning board provides two 20-pin connectors, designated J7 top and J7 bottom. J7 facilitates easy connections to various interface boards, ribbon cables or other user customized boards. The following sections provide details based on the signal conditioning needs of the application.

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3.1 As an Input to a Analog-to-Digital Converter EVM

When the signal conditioning board is used with an analog-to-digital converter EVM, connector J1 (bottom side of PCB) plugs into a male header located on the left edge of the interface board, providing support/stabilization.

The output from the signal conditioning board is available on J7. The 20-pin socket portion of J7 plugs into the analog I/O header located on the interface board which then routes the analog signals to the input of the ADC. The 20-pin header portion of J7 provides test point access to the analog signals feeding the ADC. See Table 3-1 for the details of J7 connections.

3.2 As an Output From a Digital-to-Analog Converter EVM

When the signal conditioning board is used with a digital-to-analog converter EVM, connector J1 (bottom side of PCB) plugs into one of two male analog I/O headers that provide the raw analog output from the DAC.

In this case, the female socket portion of J7 plugs into one of the male header located on the left edge of the interface board for support. The output from the signal conditioning board is available from the 20-pin male header portion of J7. Standard 0.1 inch center IDC ribbon cables can then feed the analog signal to any additional circuits or user customized board.

Table 3-1. Signal Conditioning Board J1 and J2-J5 Connections

Signal	Pin Number (Pins and Socket)		Signal
AGND	1	2	A0
AGND	3	4	A1
AGND	5	6	A2
AGND	7	8	A3
AGND	9	10	A4
AGND	11	12	A5
AGND	13	14	A6
VCOM	15	16	A7
AGND	17	18	REF(-)
AGND	19	20	REF(+)

The J7 header/socket combination is a feed through design. Signals at the pins are identical to those on the sockets located directly below them. As mentioned previously, differential signals are typically applied between adjacent channels; consult the user's guide of the data converter EVM for configuration information.

3.3 VCOM, REF(-) and REF(+) Options

Signals VCOM, REF(-) and REF(+) provide additional flexibility to certain ADC evaluation modules. In some cases, ADCs that provide a reference voltage output may have that voltage routed to the analog I/O connector for use as a biasing voltage for the amplifiers on the signal condition board. The REF(-) and REF(+) signals can also be routed to certain ADC and DAC boards in order to provide the data converter with a user definable reference input. Details for the specific use of these signals should be found in the users guide for the individual data converter evaluation module.

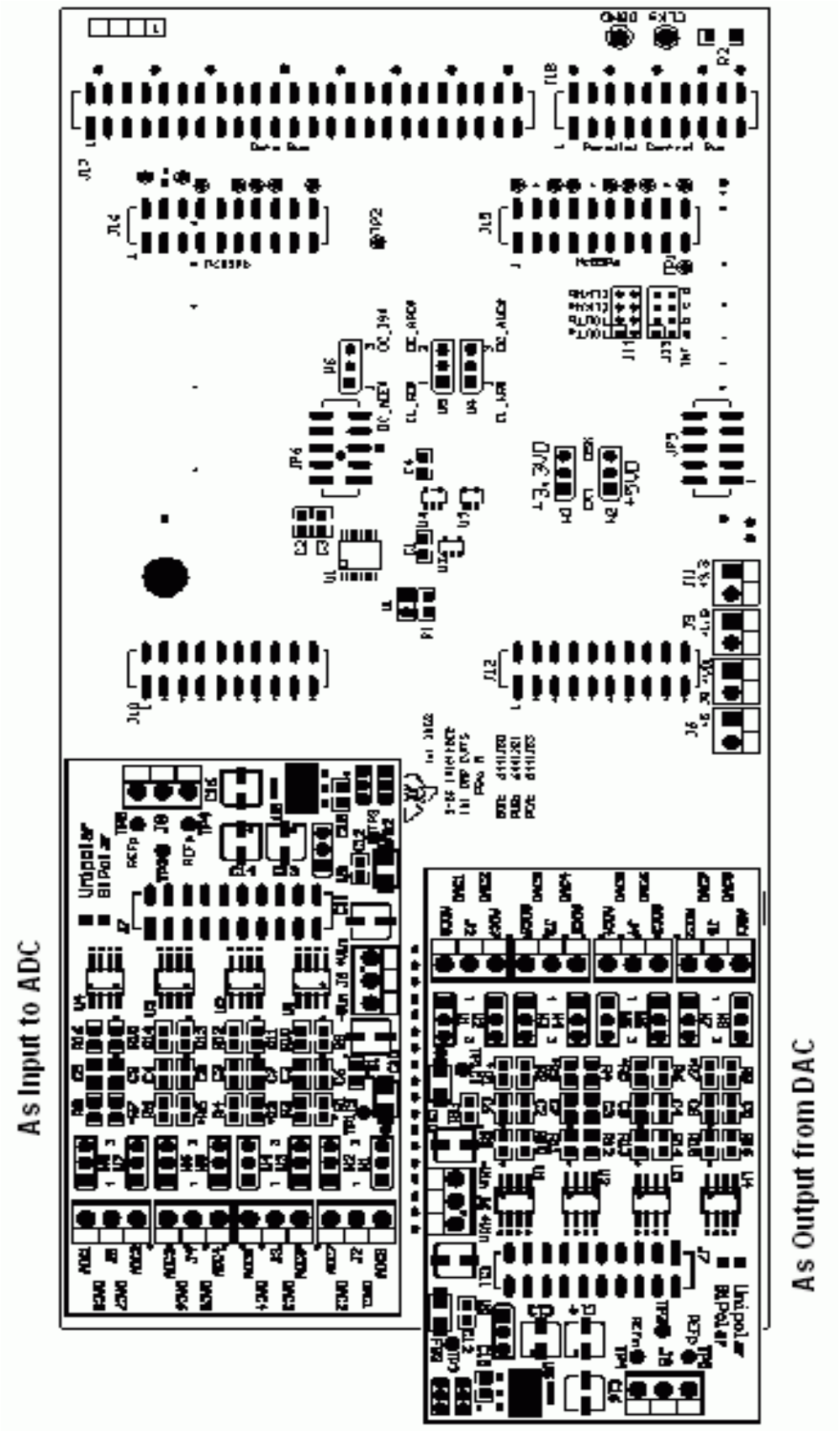
External reference voltages may be applied to three-terminal screw jack (J8). REF (+) is applied to pin 1, REF (-) to pin 3. The external reference voltages are grounded at J8, pin 2. Test points 2, 4, and 5 are used to monitor the external reference.

By default, the amplifiers on the signal conditioning board are biased to 2.5 V by means of an on-board voltage regulator (U5). W9 selects the on-board regulator (position 1-2) or the external VCOM voltage applied to J7 (position 2-3). To remove the bias voltage and ground the inverting inputs of the amplifiers, W9 is placed in position 2-3 with an additional shut jumper placed on J7, pins 15-17.

3.3.1 Installation Example

Figure 3-1 shows an installation example using two signal conditioning boards on the 5-6K interface card. The C2000 and HPA449 interface cards have the same connector arrangement which allows the signal conditioning board to be used across all three platforms.

Figure 3-1. Signal Conditiioning Board Installation on 5-6K Interfaces


As Input to ADC
As Output from DAC

Chapter 4

Power Supply Requirements

The following section provides details on the power option/requirements of the signal conditioning board.

Topic **Page**

4.1 Power Connections to the Signal Conditioning Card

As with the analog inputs, two power options are provided. When the signal condition board is used with an interface card, power is typically applied though J9, a 6-pin female socket located beside J7 on the bottom of the board. For stand alone applications, power can be applied to the three position screw jack, J6 (see the schematics for details).

4.2 Single- or Dual-Supply Options

Jumpers W10 and W11 are used to define power applied to the signal conditioning board. W10 and W11 are hard wired based on the installed op-amps. For the OPA2132 dual supply devices, pins 1-2 are shorted. For the single supply OPA2350 devices, W10 and W11 are shorted pins 2-3.

Dual supply OPA2132 devices are powered from VA and -VA as shown in Table 4-1 VA are defined as ±18 V max, but are typically powered from ±12 V or ±15 V when used with an appropriate interface board.

Single supply OPA2350 devices are powered from 5 VA. All power is referenced to AGND. Table 4-1 shows the power connector voltages supplied to the signal conditioning module.

Table 4-1. Signal Conditioning Power Connections—J9

Signal	Pin Number		Signal
+VA	1	2	-VA
5VA	3	4	-5VA
AGND	5	6	AGND

Warning

Do not exceed recommended power supply input voltages to the 5-6K interface board or to the C2000 interface board when used in conjunction with the DAP signaling conditioning boards.

Chapter 5

Amplifier Configuration Options

This section provides details on the signal conditioning board input configuration options. The information is based on applying signals to the three-terminal screw jacks, J2–J5. Refer to the schematic at the end of this document and/or Table 1-1 when analog inputs are applied to the J1 connector.

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5.1 Single Ended Inputs

Single ended analog input signals can be applied to screw jack terminals one or three, referenced to terminal two. While jumpers W1–W9 are in their default positions (pins 1-2), 2.5 V is applied to the noninverting terminals of U1 through U4. A 5 Vp-p signal, from 0-5 V, applied to terminals 1 or 3 will provide an inverted 0-5 V signal to the corresponding output pin on J7. Table 5-1 shows the mapping of J1 through J5 to J7.

Table 5-1. Analog Signal Mapping J2-J5 and J1 to J7

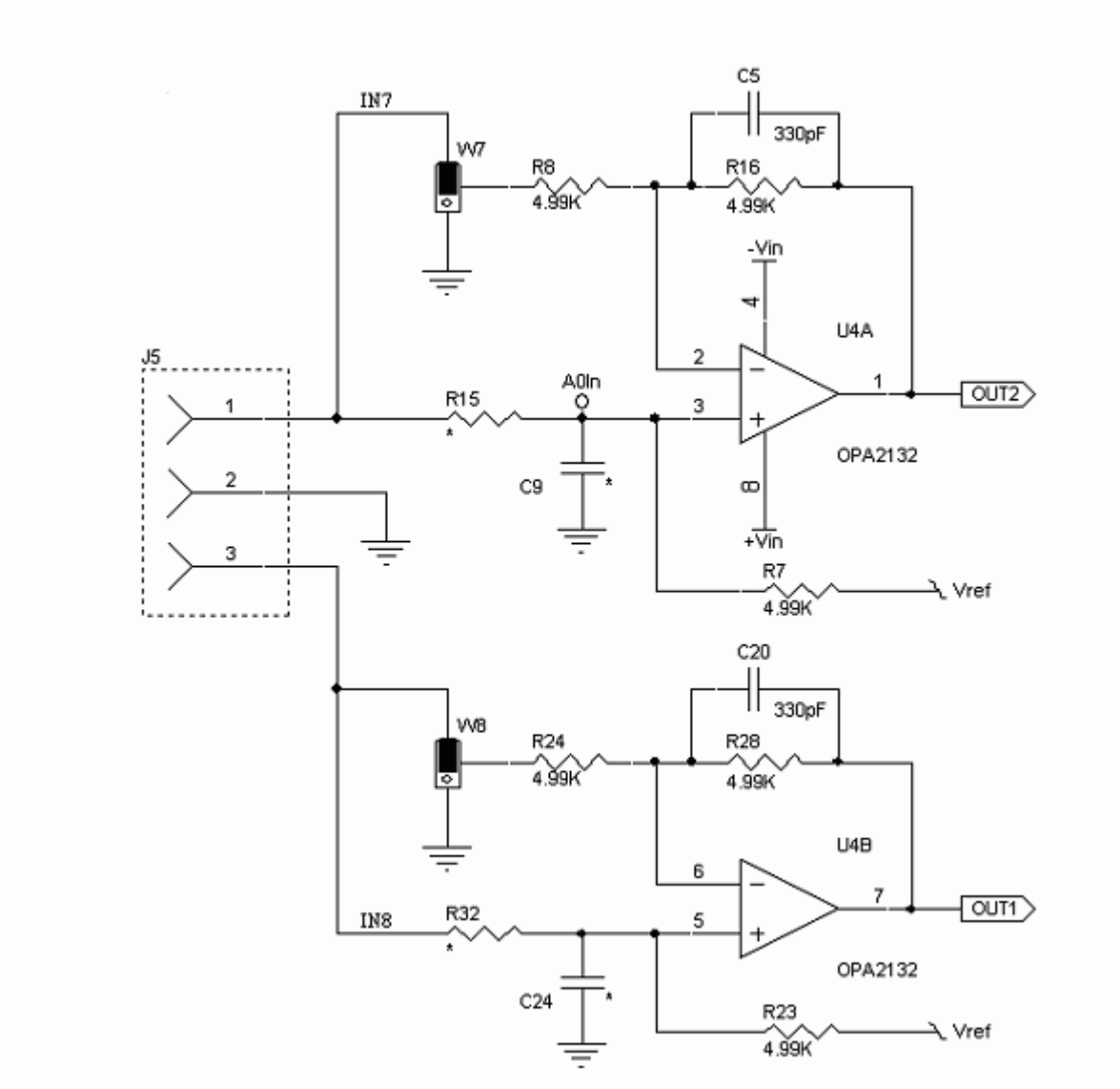
Screw Terminal Signal Input	J1 Signal Input	Signal Output
J5.3 (ADC1)	J1.16 (DAC8)	J7.2
J5.1 (ADC2)	J1.14 (DAC7)	J7.4
J4.3 (ADC3)	J1.12 (DAC6)	J7.6
J4.1 (ADC4)	J1.10 (DAC5)	J7.8
J3.3 (ADC5)	J1.8 (DAC4)	J7.10
J3.1 (ADC6)	J1.6 (DAC3)	J7.12
J2.3 (ADC7)	J1.4 (DAC2)	J7.14
J2.1 (ADC8)	J1.2 (DAC1)	J7.16

5.2 Differential Inputs

Differential analog input signals can be applied between screw jack terminals one and three. The output in this case would be a differential signal taken between pins 2 and 4, 6 and 8, 10 and 12 or 14 and 16 of J7, with pins 2, 4, 6, and 8 assumed to be the positive input.

Figure 5-1 provides details of the default signal conditioning board configuration. Components noted with an asterisk in the schematic are not installed. These components are place holders for 0805 size surface mount resistors or capacitors. All shunt jumpers are installed in position 1-2, providing a unity gain inverting buffer configuration.

Figure 5-1. Typical Channel Configuration+Factory Defaults



Note: Components marked with asterisk are NOT installed.

Chapter 6

DAP Signal Conditioning Board Assembly and Board Schematics

This chapter contains the board assembly and board schematics.

Topic **Page**

6.1 DAP Signal Conditioning Board Assembly

Figure 6-1. Board Assembly (Top View)

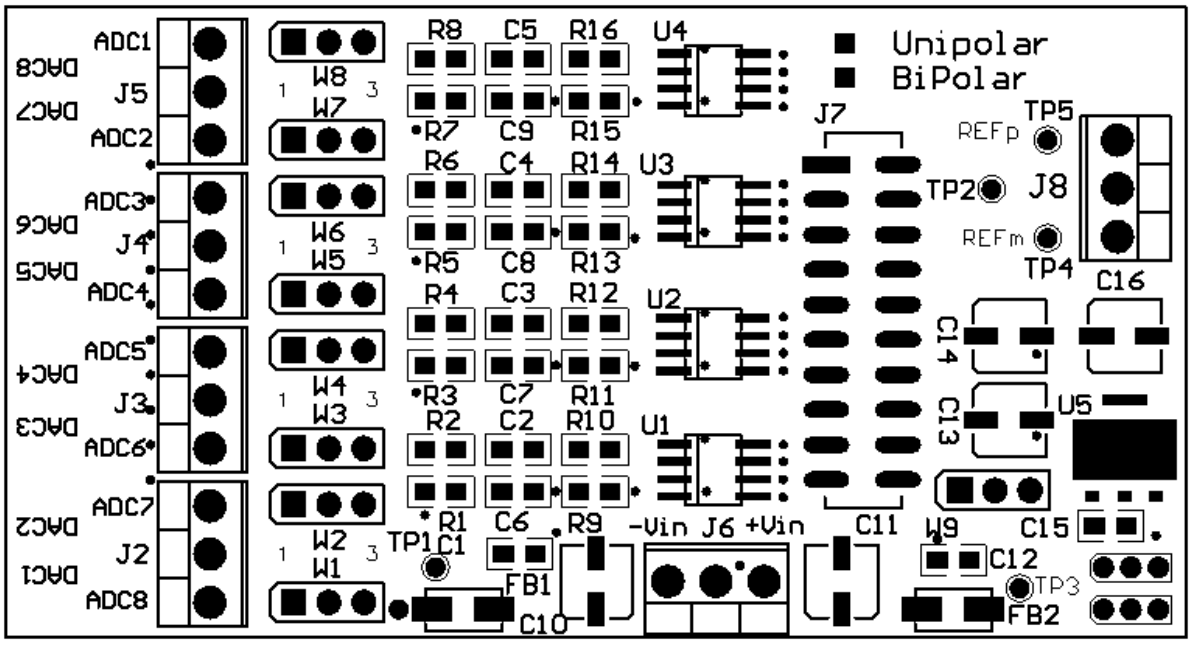


Figure 6-2. Board Assembly (Bottom View)

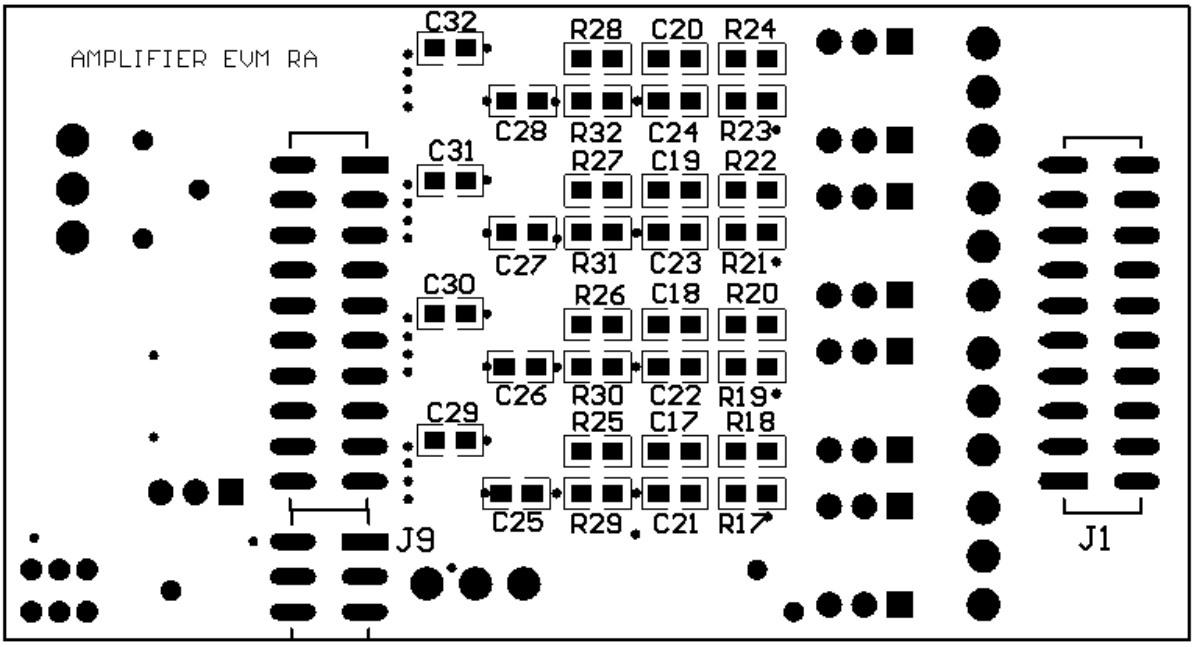
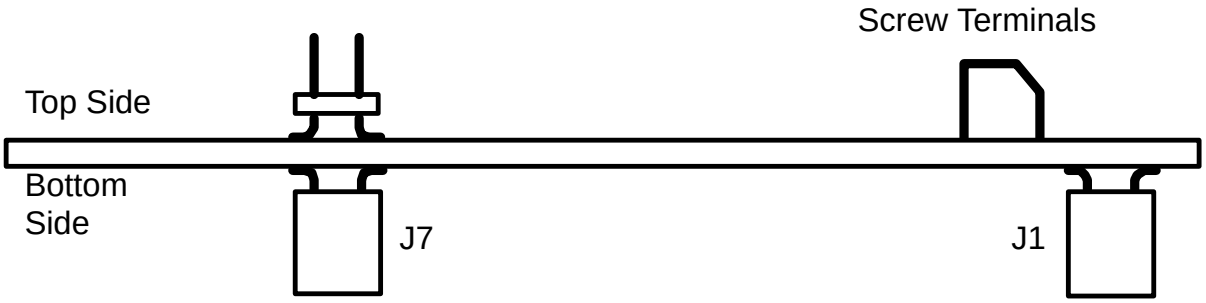


Figure 6-3. Board Assembly (Top / Side View)

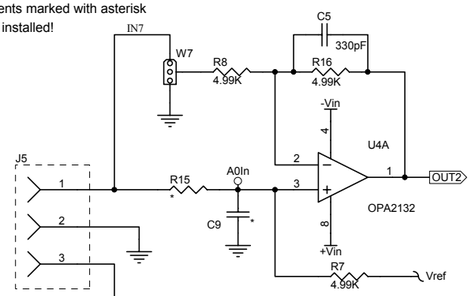


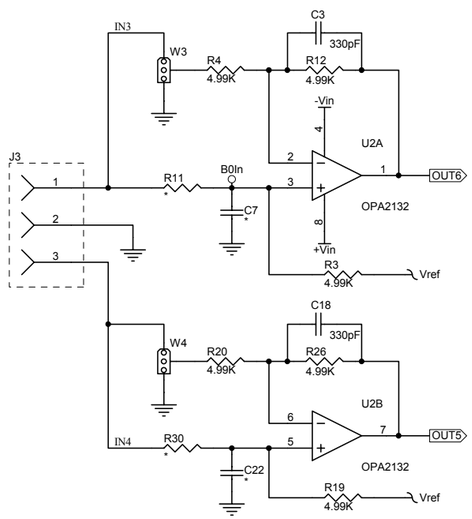
6.2 DAP Signal Conditioning Board Schematic

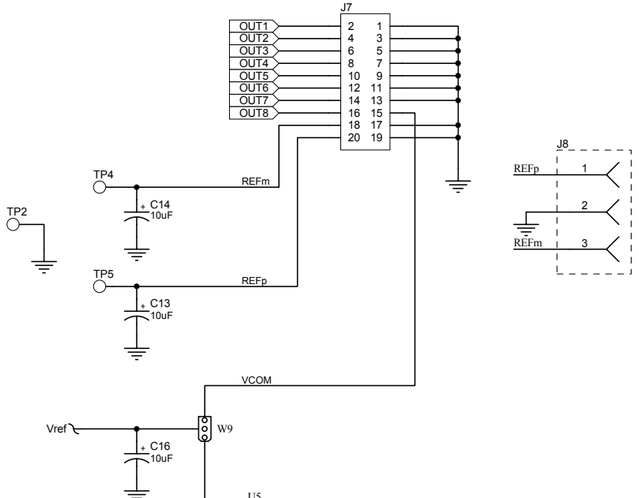
Figure 6-4. Board Schematic

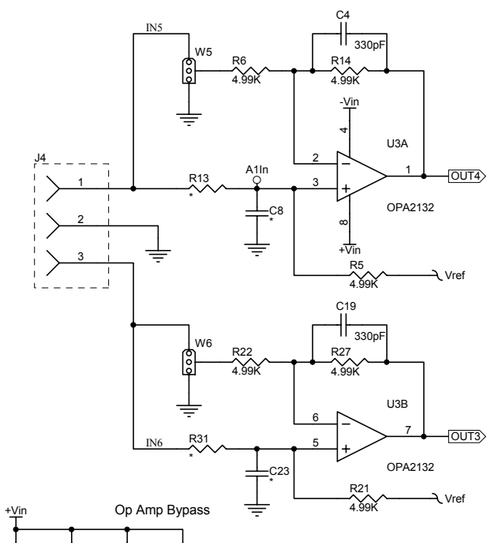
Note:
Components marked with asterisk are NOT installed!

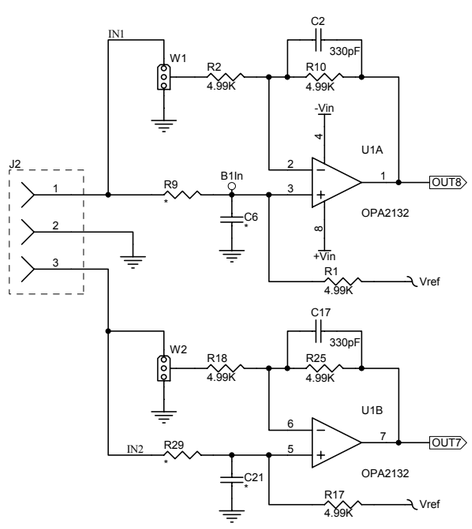
Revision History		
REV	ECN Number	Approved

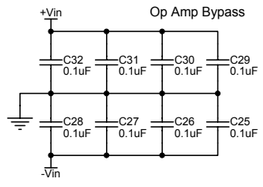


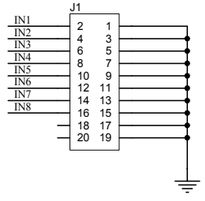


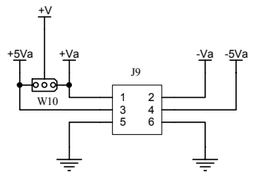












TEXAS INSTRUMENTS
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Title: Amplifier Board Schematic

Engineer: Various			
Drawn By: T. Hendrick	SIZE:	DATE: 7-Apr-2003	REV: A
FILE: 6447453.ddb			SHEET: 1 OF: 1