T-50-17-00

CD54/74HC7046A
CD54/74HCT7046A

File Number 1920

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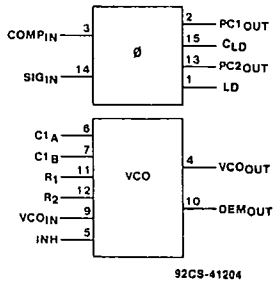


FUNCTIONAL DIAGRAM

Phase-Locked Loop with VCO And Lock Detector

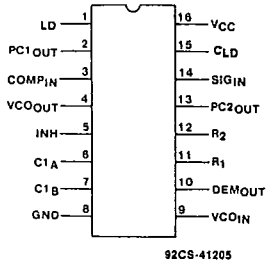
Type Features:

- *Center frequency of 18 MHz (typ.) at V_{CC} = 5 V*
- *Choice of two phase comparators: Exclusive-OR, Edge-triggered JK flip-flop*
- *Excellent VCO frequency linearity*
- *VCO-inhibit control for ON/OFF keying and for low standby power consumption*
- *Minimal frequency drift*
- *Zero voltage offset due to op-amp buffer*
- *Operating power-supply voltage range: VCO section 3 V to 6 V; Digital section 2 V to 6 V*

The RCA-CD54/74HC7046A and CD54/74HCT7046A high-speed silicon-gate CMOS devices, specified in compliance with JEDEC Standard No. 7A, are phase-locked-loop (PLL) circuits that contain a linear voltage-controlled oscillator (VCO), two-phase comparators (PC1, PC2), and a lock detector. A signal input and a comparator input are common to each comparator. The lock detector gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (Gnd). For a frequency range of 100 kHz to 10 MHz, the lock detector capacitor should be 1000 pF to 10 pF, respectively.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 7046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The CD54HC7046A and CD54HCT7046A are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC7046A and CD74HCT7046A are supplied in 16-lead plastic dual-in-line packages (E suffix) and in 16-lead small-outline plastic dual-in-line packages (M suffix). Both types are also available in chip form (H suffix).



TERMINAL ASSIGNMENT

Applications:

- *FM modulation and demodulation*
- *Frequency synthesis and multiplication*
- *Frequency discrimination*
- *Tone decoding*
- *Data synchronization and conditioning*
- *Voltage-to-frequency conversion*
- *Motor-speed control*
- *For additional information, refer to application note, ICAN-8823.*

Family Features:

- *Fanout (over temperature range); Standard outputs - 10 LSTTL loads Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range: CD74HC/HCT: -40 to +125° C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source: Philips/Signetics*
- *CD54HC/CD74HC types: 2 V to 6 V operation High noise immunity: N_{IL}=30%, N_{IH}=30% of V_{CC}; @V_{CC}=5 V*
- *CD54HCT/CD74HCT types: 4.5 V to 5.5 V operation Direct LSTTL input logic compatibility V_{IL}=0.8 V max., V_{IH}=2 V min. CMOS input compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F,H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H ..... -55 to +125°C
PACKAGE TYPE E,M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 In. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

PIN DESCRIPTION

Pin No.	Symbol	Name and Function
1	LD	Lock Detector output (active high)
2	$PC1_{OUT}$	Phase Comparator 1 output
3	$COMP_{IN}$	Comparator input
4	VCO_{OUT}	VCO output
5	INH	Inhibit input
6	$C1_A$	Capacitor C1 connection A
7	$C1_B$	Capacitor C1 connection B
8	Gnd	Ground (0 V)

Pin No.	Symbol	Name and Function
9	VCO_{IN}	VCO input
10	DEM_{OUT}	Demodulator output
11	R_1	Resistor R1 connection
12	R_2	Resistor R2 connection
13	$PC2_{OUT}$	Phase Comparator 2 output
14	SIG_{IN}	Signal Input
15	C_{LD}	Lock Detector Capacitor Input
16	V_{CC}	Positive Supply Voltage

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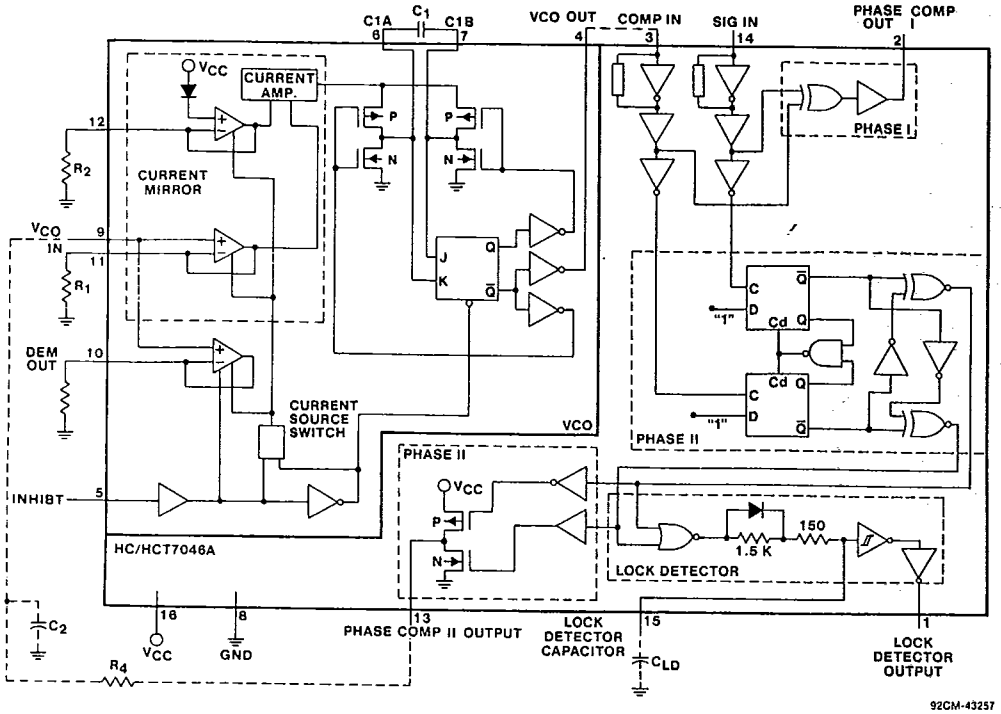

Fig. 1 - Logic diagram.

GENERAL DESCRIPTION

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R1 and Gnd) or two external resistors R1 and R2 (between R1 and Gnd, and R2 and Gnd). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. See logic diagram, Fig. 1.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to Gnd; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a guaranteed duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO, while a HIGH level disables the VCO to minimize standby power consumption.

Phase Comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase Comparator 1 (PC1)

This is an Exclusive-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 2. The average of V_{DEM} is equal to ½ V_{CC} when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 3.

The frequency capture range ($2f_C$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy input signals. Typical of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

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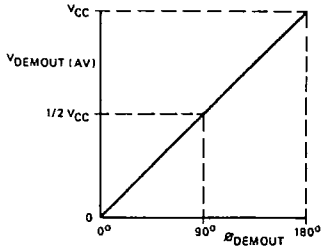

Fig. 2 - Phase comparator 1: average output voltage vs input phase difference:
$V_{DEMOUT}=V_{PC1OUT}=(V_{CC}/\pi)\ (\phi_{SIGIN}-\phi_{COMPIN})$;
$\phi_{DEMOUT}=(\phi_{SIGIN}-\phi_{COMPIN})$.

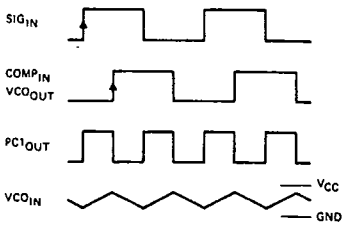

Fig. 3 - Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

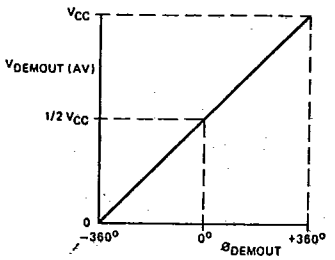

Fig. 4 - Phase comparator 2: average output voltage vs input phase difference:
$V_{DEMOUT}=V_{PC2OUT}=(V_{CC}/4\pi)\ (\phi_{SIGIN}-\phi_{COMPIN})$;
$\phi_{DEMOUT}=(\phi_{SIGIN}-\phi_{COMPIN})$.

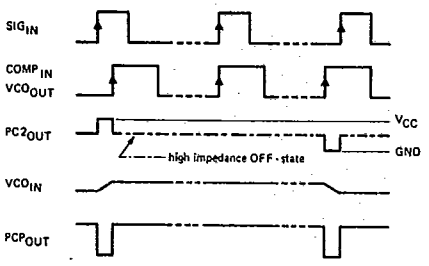

Fig. 5 - Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 1) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple (f_r = f_i) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/4\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 4. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 5.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n-and p-type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p- and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN}, the VCO adjusts, via PC2, to its lowest frequency.

Lock Detector Theory of Operation

Detection of a locked condition is accomplished by a NOR gate and an envelope detector as shown in Fig. 6. When the PLL is in Lock, the output of the NOR gate is High and the lock detector output (Pin 1) is at a constant high level. As the loop tracks the signal on Pin 14 (signal in), the NOR gate outputs pulses whose widths represent the phase differences between the VCO and the input signal. The time between pulses will be approximately equal to the time constant of the VCO center frequency. During the rise time of the pulse, the diode across the 1.5-kΩ resistor is forward biased and the time constant in the path that charges the lock detector capacitor is

$T = (150\ \Omega \times C_{LD})$.

During the fall time of the pulse the capacitor discharges through the 1.5 kΩ and the 150-Ω resistors and the channel resistance of the n-device of the NOR gate to ground

$(T = (1.5\ k\Omega + 150\ \Omega + Rn\text{-channel}) \times C_{LD})$.

The waveform present at the capacitor resembles a sawtooth as shown in Fig. 7. The lock detector capacitor value is determined by the VCO center frequency. The typical range of capacitor for a frequency of 10 MHz is about 10 pF and for a frequency of 100 kHz is about 1000 pF. The chart in Fig. 8 can be used to select the proper lock detector capacitor value. As long as the loop remains locked and tracking, the

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level of the sawtooth will not go below the switching threshold of the Schmitt-trigger inverter. If the loop breaks lock, the width of the error pulse will be wide enough to allow the sawtooth waveform to go below threshold and a level change at the output of the Schmitt trigger will indicate a loss of lock, as shown in Fig. 9. The lock detector capacitor also acts to filter out small glitches that can occur when the loop is either seeking or losing lock.

Note:
When using phase comparator 1, the detector will only indicate a lock condition on the fundamental frequency and not on the harmonics, which PC1 will also lock on. If a detection of lock is needed over the harmonic locking range of PC1, then the lock detector output must be OR-ed with the output of PC1.

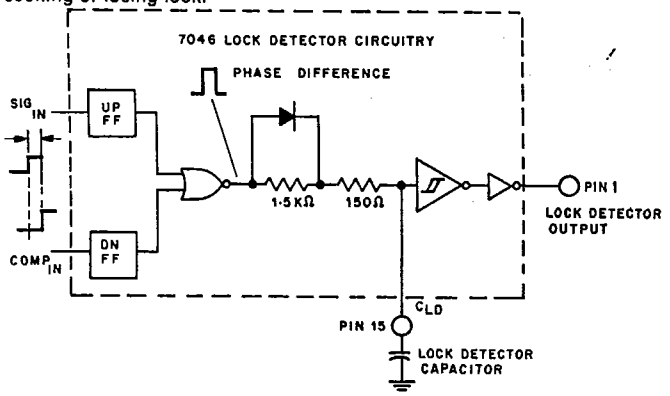

Fig. 6 - CD54/74HC/HCT7046A lock detector circuit.

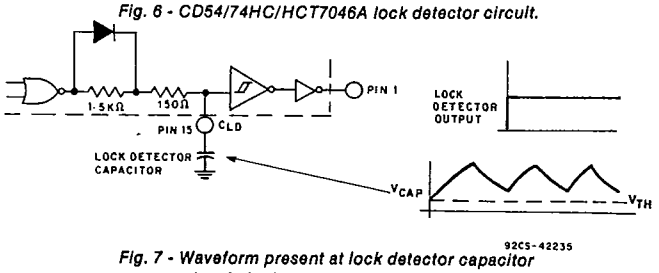

Fig. 7 - Waveform present at lock detector capacitor when in lock.

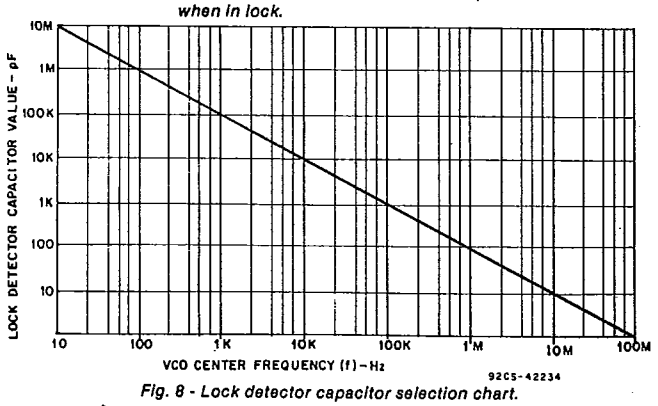

Fig. 8 - Lock detector capacitor selection chart.

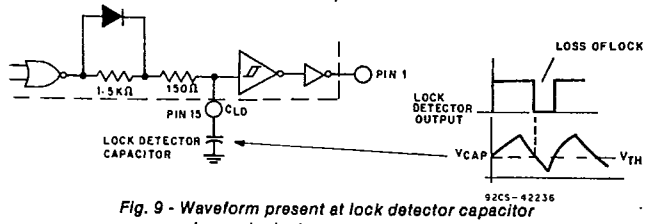

Fig. 9 - Waveform present at lock detector capacitor when unlocked.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			74HC/54HC			74HC		54HC −55/ +125°C		TEST CONDITIONS		74HCT/54HCT			74HCT		54HCT −55/ +125°C		UNITS
				+25°C			−40/ +85°C		74HC −40/ +125°C				+25°C			−40/ +85°C		74HCT −40/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
VCO SECTION																				
INH High-Level Input Voltage V_{IH}			3	2.1	—	—	2.1	—	2.1	—	—	4.5 / to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
INH Low-Level Input Voltage V_{IL}			3	—	—	0.9	—	0.9	—	0.9	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
VCO_{OUT} High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	3	2.9	—	—	2.9	—	2.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
VCO_{OUT} Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
C1A, C1B Low-Level Output Voltage (Test purposes only) V_{OL}	V_{IL} or V_{IH}	4	4.5	—	—	0.40	—	0.47	—	0.54	V_{IL} or V_{IH}	4.5	—	—	0.40	—	0.47	—	0.54	V
		5.2	6	—	—	0.40	—	0.47	—	0.54										
INH VCO_{IN} Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
R1 Range See Note 1			3	—	—	—	—	—	—	—		4.5	3	—	—	—	—	—	—	kΩ
			4.5	3	—	—	—	—	—	—										
			6	—	—	—	—	—	—	—										
R2 Range See Note 1			3	—	—	—	—	—	—	—		4.5	3	—	—	—	—	—	—	kΩ
			4.5	3	—	—	—	—	—	—										
			6	—	—	—	—	—	—	—										
C1 Capacitance Range			3	—		No LIMIT	—	—	—	—		4.5	40	—	No LIMIT	—	—	—	—	pF
			4.5	40	—		—	—	—	—										
			6	—	—		—	—	—	—										
VCO_{IN} Operating Voltage Range	Over the range specified for R1 for Linearity See Figs. 10 & 36-39 See Note 2		3	0.9	—	1.9	—	—	—	—		4.5	0.9	—	3.2	—	—	—	—	V
			4.5	0.9	—	3.2	—	—	—	—										
			6	0.9	—	4.6	—	—	—	—										

NOTES: 1. The value for R1 & R2 in parallel should exceed 2.7 kΩ; R1 & R2 values above 300 kΩ may contribute to frequency shift due to leakage currents.
2. The maximum operating voltage can be as high as V_{CC} -0.9 V; however, this may result in an increased offset voltage.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			74HC/54HC			74HC		54HC −55/ +125°C		TEST CONDITIONS		74HCT/54HCT			74HCT		54HCT −55/ +125°C		UNITS
	V_I V	I_O mA	V_{CC} V	+25°C			−40/ +85°C		74HC −40/ +125°C		V_I V	V_{CC} V	+25°C			−40/ +85°C		74HCT −40/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
PHASE COMPARATOR SECTION																				
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	3.15	—	—	3.15	—	3.15	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	1.35	—	1.35	—	1.35	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
LD, PCn_{OUT} High-Level Output Voltage CMOS Loads V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
LD, PCn_{OUT} Low-Level Output Voltage CMOS Loads V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
SIG_{IN}, $COMP_{IN}$ Input Leakage Current I_I	V_{CC} or Gnd		2	—	—	±3	—	±4	—	±5	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±30	—	±38	—	±45	μA
			3	—	—	±7	—	±9	—	±11										
			4.5	—	—	±18	—	±23	—	±29										
			6	—	—	±30	—	±38	—	±45										
$PC2_{OUT}$ 3-State Off-State Current I_{OZ}	V_{IL} or V_{IH}		6	—	—	±0.5	—	±5	—	±10		5.5	—	—	±0.5	—	±5	—	±10	μA
SIG_{IN}, $COMP_{IN}$ Input Resistance R_I See Fig. 10	V_I at Self-Bias Oper. Point: ΔV_I = 0.5 V See Fig. 10		3	—	800	—	—	—	—	—		4.5	—	250	—	—	—	—	—	kΩ
			4.5	—	250	—	—	—	—	—										
			6	—	150	—	—	—	—	—										

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			74HC/54HC			74HC		54HC −55/ +125°C		TEST CONDITIONS		74HCT/54HCT			74HCT		54HCT −55/ +125°C		UNITS
	V_I V	I_O mA	V_{CC} V	+25°C			−40/ +85°C		74HC −40/ +125°C		V_I V	V_{CC} V	+25°C			−40/ +85°C		74HCT −40/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
DEMODULATOR SECTION																				
Resistor Range R_S	at R_S > 300 kΩ Leakage Current can influence V_{DEMOUT}	3	10	—	300															
		4.5	10	—	300							4.5	10	—	300					kΩ
		6	10	—	300															
Offset Voltage VCO_{IN} to V_{DEM} V_{OFF}	$V_I = V_{VCOIN} = \frac{V_{CC}}{2}$ Values taken over R_S range See Fig. 17	3	—	±30	—															
		4.5	—	±20	—							4.5	—	±20	—					mV
		6	—	±10	—															
Dynamic Output Resistance at DEM_{OUT} R_O	$V_{DEMOUT} = \frac{V_{CC}}{2}$	3	—	25	—															
		4.5	—	25	—							4.5	—	25	—					Ω
		6	—	25	—															
Quiescent Device Current I_{CC}	Pins 3, 5 & 14 at V_{CC} Pin 9 at Gnd. I_L at Pins 3 & 14 to be excluded	6	—	—	8	—	80	—	160		V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current Per Input Pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1 (Excluding Pin 5)	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
INH	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS		25°C				-40°C to +85°C				-55°C to +125°C (54) -40°C to +125°C (74)				UNITS
		V_{CC}	HC		HCT		74HC		74HCT		HC		HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
PHASE COMPARATOR SECTION															
Propagation Delay,		2	—	200	—	—	—	250	—	—	—	300	—	—	
SIG_{IN}, $COMP_{IN}$ t_{PLH}		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
to $PC1_{OUT}$ t_{PHL}		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition		2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
t_{TLH}		6	—	13	—	—	—	16	—	—	—	19	—	—	
Output Enable Time,		2	—	280	—	—	—	350	—	—	—	420	—	—	ns
SIG_{IN}, $COMP_{IN}$ t_{PZH}		4.5	—	56	—	60	—	70	—	75	—	84	—	90	
to $PC2_{OUT}$ t_{PZL}		6	—	48	—	—	—	60	—	—	—	71	—	—	
Output Disable Time,		2	—	325	—	—	—	405	—	—	—	490	—	—	
SIG_{IN}, $COMP_{IN}$ t_{PHZ}		4.5	—	65	—	70	—	81	—	86	—	98	—	105	
to $PC2_{OUT}$ t_{PLZ}		6	—	55	—	—	—	69	—	—	—	83	—	—	
AC Coupled Input			TYPICAL												
Sensitivity (p-p) at	V_I (p-p)	3	11		11										
SIG_{IN} or $COMP_{IN}$		4.5	15		15										mV
		6	33		33										
VCO SECTION															
Frequency Stability		3	—		—										
with Temperature $\frac{\Delta f}{\Delta T}$	R_1 = 100 kΩ	4.5	—		—		TYP.		TYP.						%/°C
Change	R_2 = ∞	6	—		—		0.11		0.11						
Max. Frequency	C_1 = 50 pF	3	—		—										
	R_1 = 3.5 kΩ	4.5	24		24										MHz
f_{max}	R_2 = ∞	6	—		—										
	C_1 = 0 pF	3	—		—										
	R_1 = 9.1 kΩ	4.5	38		38										MHz
	R_2 = ∞	6	—		—										
Center Frequency	C_1 = 40 pF	3	—		—										
	R_1 = 3 kΩ	4.5	17		17										
f_o	R_2 = ∞	6	—		—										MHz
	$VCO_{IN} = \frac{V_{CC}}{2}$														
Frequency Linearity,	R_1 = 100 kΩ	3	—		—										
Δf_{vco}	R_2 = ∞	4.5	0.4		0.4										%
	C_1 = 100 pF	6	—		—										
Offset Frequency	R_2 = 220 kΩ	3	—		—										
	C_1 = 1 nF	4.5	400		400										kHz
		6	—		—										
DEMODULATOR SECTION															
V_{OUT} vs. f_{IN}	R_1 = 100 kΩ														
	R_2 = ∞														
	C_1 = 100 pF	3	—		—										
	R_S = 10 kΩ	4.5	330		330										mV/kHz
	R_3 = 100 kΩ	6	—		—										
	C_2 = 100 pF														

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Figure References for DC Characteristics

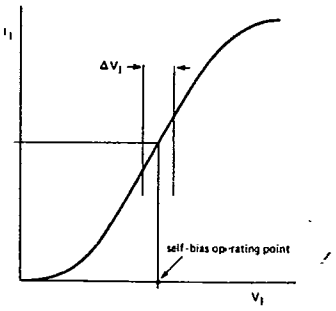

Fig. 10 - Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

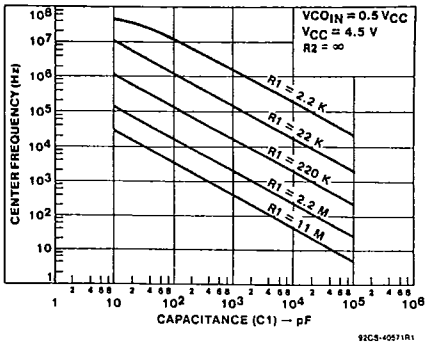

Fig. 11 - HC7046A typical center frequency vs. R1, C1.

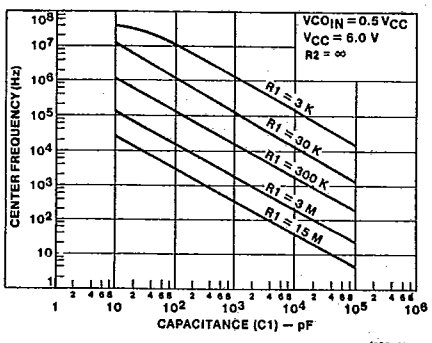

Fig. 12 - HC7046A typical center frequency vs. R1, C1.

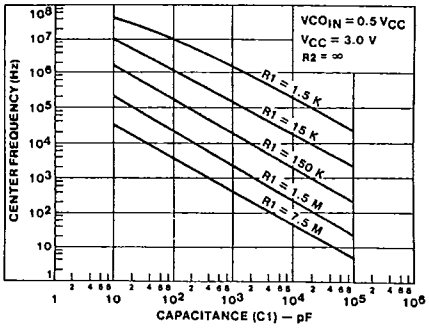

Fig. 13 - HC7046A typical center frequency vs. R1, C1.

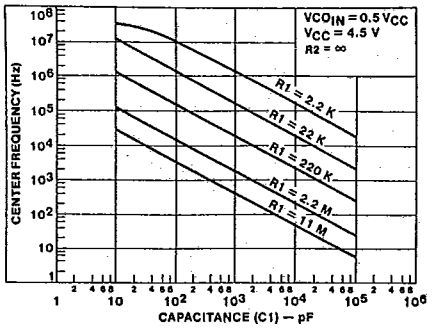

Fig. 14 - HCT7046A typical center frequency vs. R1, C1.

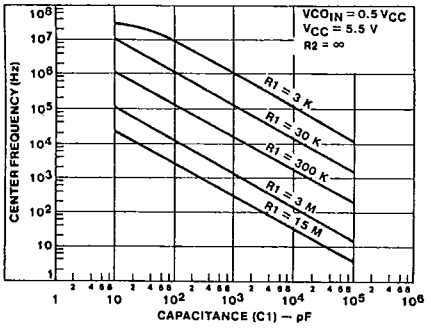

Fig. 15 - HCT7046A typical center frequency vs. R1, C1.

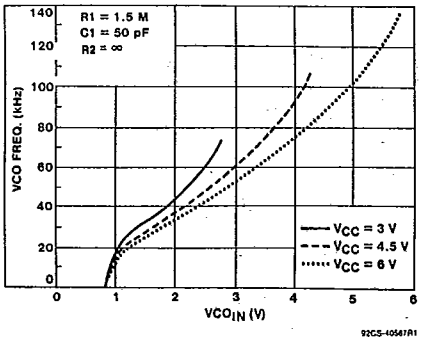

Fig. 16 - HC7046A typical VCO frequency vs. VCO_{IN}.

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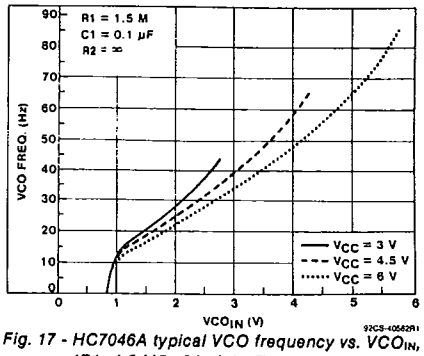

Fig. 17 - HC7046A typical VCO frequency vs. VCO_{IN}, (R1=1.5 MΩ, C1=0.1 µF).

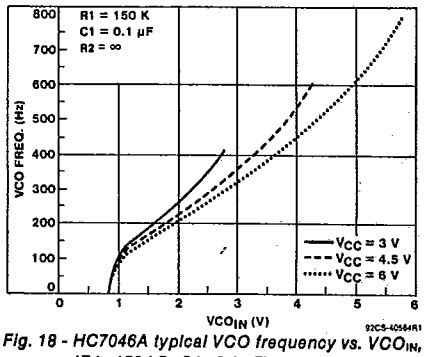

Fig. 18 - HC7046A typical VCO frequency vs. VCO_{IN}, (R1=150 kΩ, C1=0.1 µF).

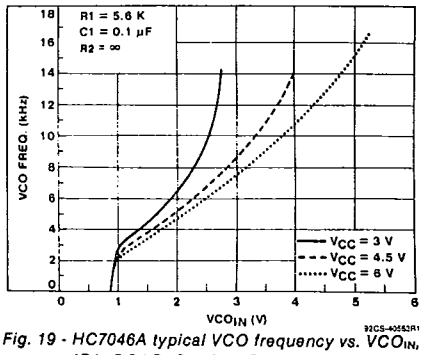

Fig. 19 - HC7046A typical VCO frequency vs. VCO_{IN}, (R1=5.6 kΩ, C1=0.1 µF).

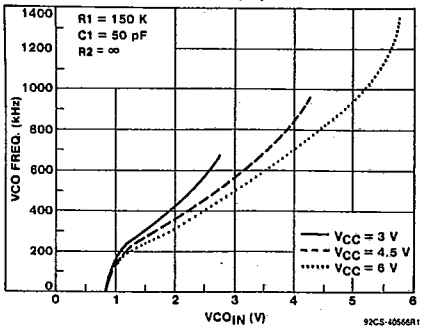

Fig. 20 - HC7046A typical VCO frequency vs. VCO_{IN}, (R1=150 kΩ, C1=50 pF).

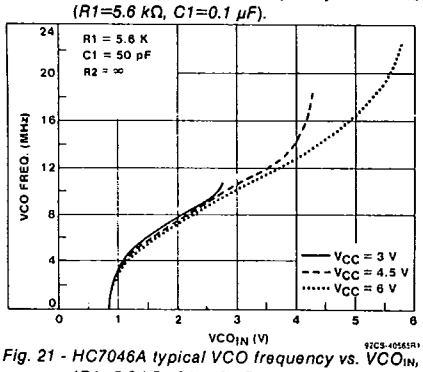

Fig. 21 - HC7046A typical VCO frequency vs. VCO_{IN}, (R1=5.6 kΩ, C1=50 pF).

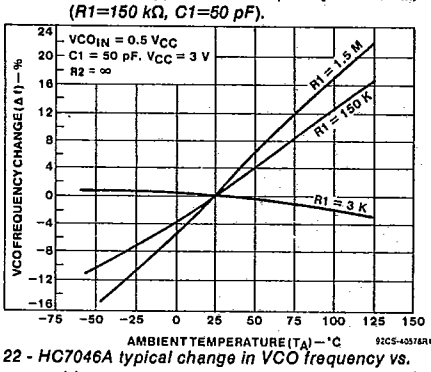

Fig. 22 - HC7046A typical change in VCO frequency vs. ambient temperature as a function of R1 (V_{CC}=3 V).

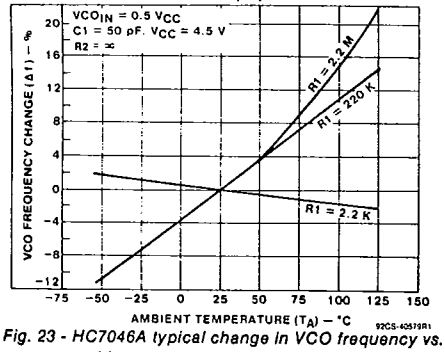

Fig. 23 - HC7046A typical change in VCO frequency vs. ambient temperature as a function of R1.

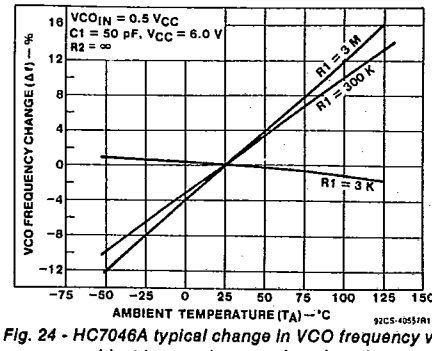

Fig. 24 - HC7046A typical change in VCO frequency vs. ambient temperature as a function of R1.

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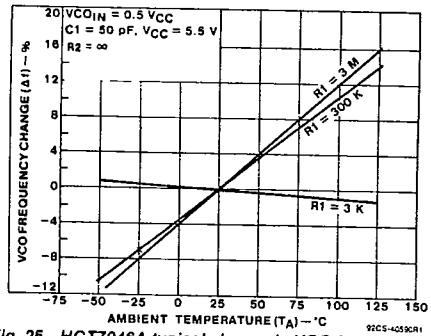

Fig. 25 - HCT7046A typical change in VCO frequency vs. ambient temperature as a function of R1.

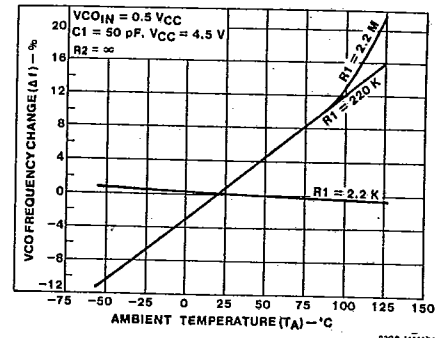

Fig. 26 - HC7046A typical change in VCO frequency vs. ambient temperature as a function of R1.

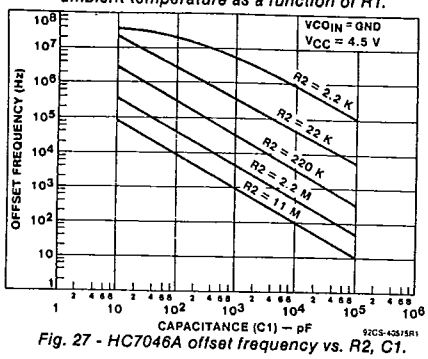

Fig. 27 - HC7046A offset frequency vs. R2, C1.

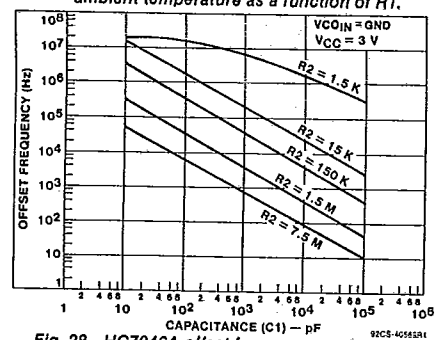

Fig. 28 - HC7046A offset frequency vs. R2, C1.

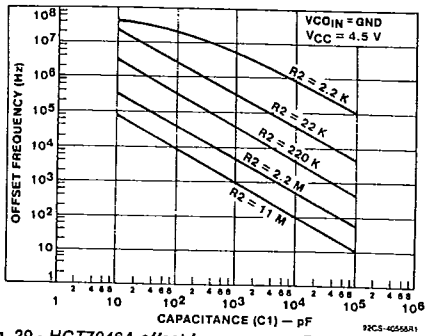

Fig. 29 - HCT7046A offset frequency vs. R2, C1 (V_{CC}=4.5 V).

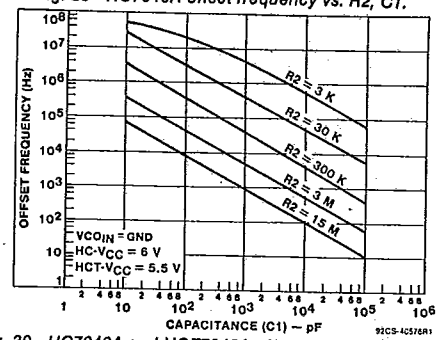

Fig. 30 - HC7046A and HCT7046A offset frequency vs. R2, C1.

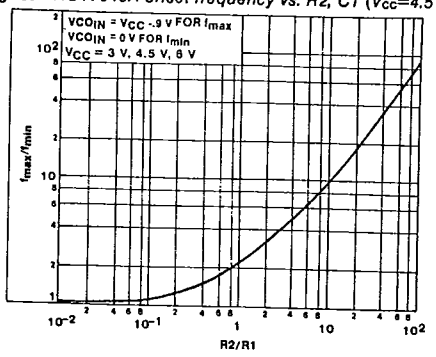

Fig. 31 - HC7046A f_{MAX}/f_{MIN} vs. R2/R1.

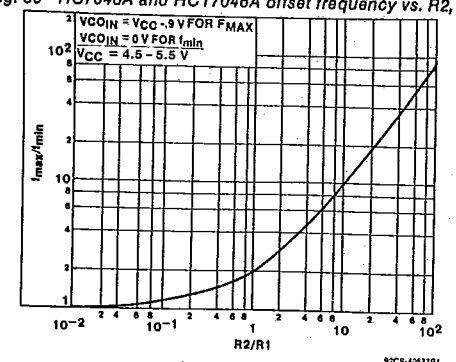

Fig. 32 - HCT7046A f_{MAX}/f_{MIN} vs. R2/R1.

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AC WAVEFORMS

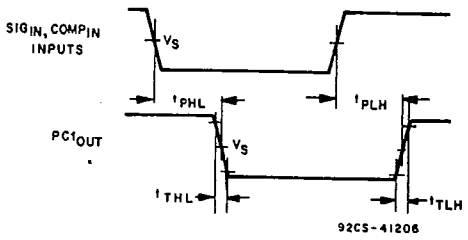


Fig. 33 - Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output ($PC1_{OUT}$) propagation delays and the output transition times.

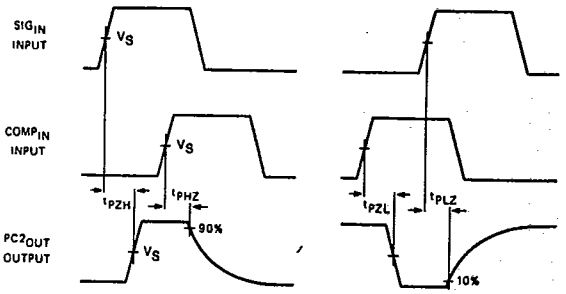
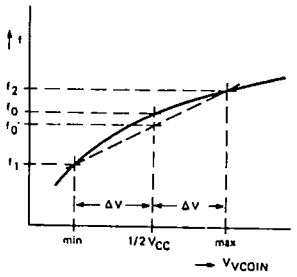


Fig. 34 - Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

	HC	HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V



$\Delta V = 0.5$ V over the V_{CC} range:

for VCO linearity

$$f'_o = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_o - f_o}{f'_o} \times 100\%$$

Fig. 35 - Definition of VCO frequency linearity.

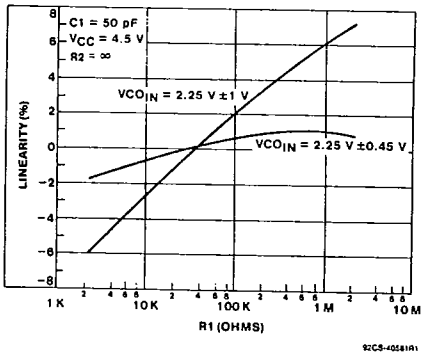


Fig. 36 - HC7046A VCO linearity vs. R1.

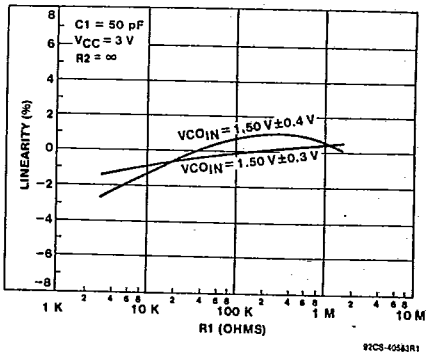


Fig. 37 - HC7046A VCO linearity vs. R1.

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CD54/74HCT7046A

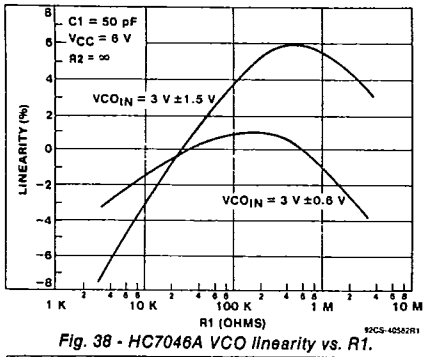


Fig. 38 - HC7046A VCO linearity vs. R1.

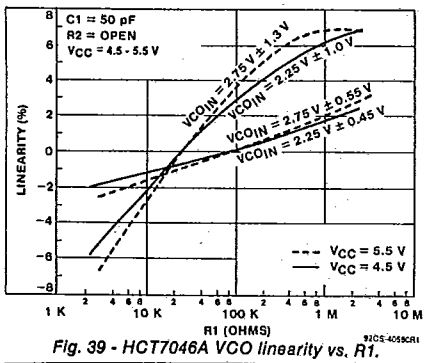


Fig. 39 - HCT7046A VCO linearity vs. R1.

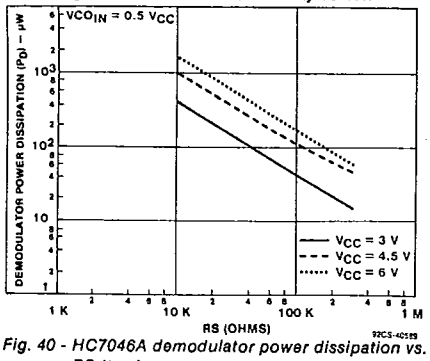


Fig. 40 - HC7046A demodulator power dissipation vs. RS (typ.).

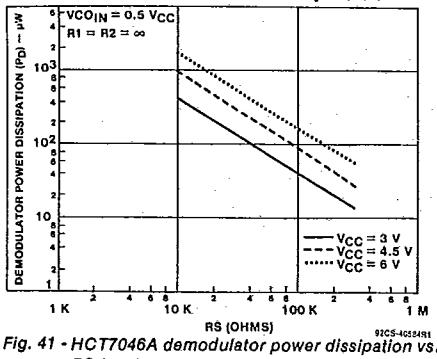


Fig. 41 - HCT7046A demodulator power dissipation vs. RS (typ.).

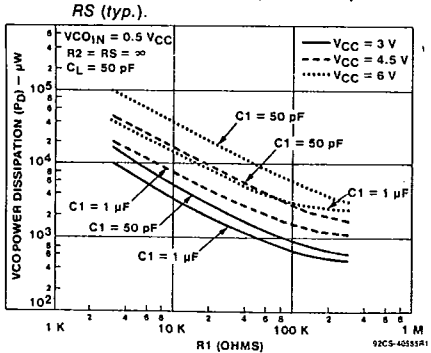


Fig. 42 - HC7046A VCO power dissipation vs. R1 (C1=50 pF, 1 µF).

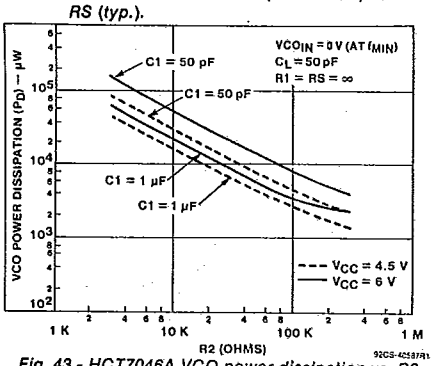


Fig. 43 - HCT7046A VCO power dissipation vs. R2 (C1=50 pF; 1 µF).

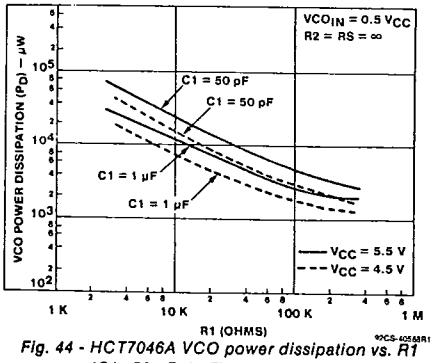


Fig. 44 - HCT7046A VCO power dissipation vs. R1 (C1=50 pF; 1 µF).

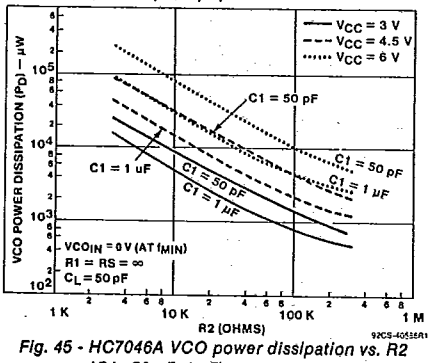


Fig. 45 - HC7046A VCO power dissipation vs. R2 (C1=50 pF, 1 µF).

CD54/74HC7046A
CD54/74HCT7046A

HC/HCT7046A C_{PD}

Chip Section	HC	HCT	Unit
Comparator 1	48	50	pF
Comparator 2	39	48	
VCO	61	53	

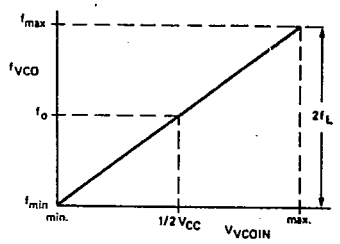
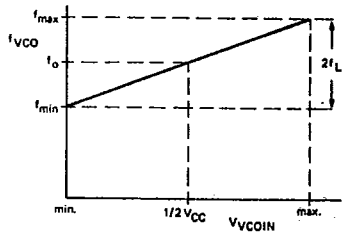
APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046A in a phase-lock-loop system.

References should be made to Fig. 11 through 21 and 27 through 32 as indicated in the table.

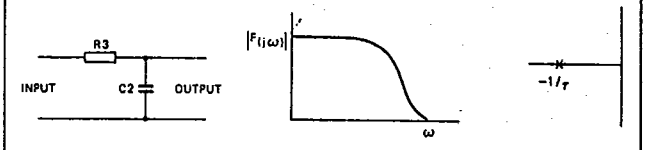
Values of the selected components should be within the following ranges:

R1 > 3 kΩ;
R2 > 3 kΩ;
R1 ‖ R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO Frequency **without extra offset** ($R2 = \infty$)	PC1 or PC2	**VCO Frequency Characteristic** The characteristics of the VCO operation are shown in Figs. 11-21.  *Fig. 46 - Frequency characteristic of VCO operating without offset: f_o = center frequency: $2f_L$ = frequency lock range.*
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Figs. 11-15.
	PC2	Given f_{max} and f_o, determine the values of R1 and C1 using Figs. 11-15. To obtain $2f_L$: $2f_L \approx \frac{2(\Delta VCO_{IN})}{R1C1}$ where $0.9\ V < VCO_{IN} < V_{CC} - 0.9\ V$ is the range of ΔVCO_{IN}
VCO Frequency **with extra offset** ($R2 > 3$ kΩ)	PC1 or PC2	**VCO Frequency Characteristic** The characteristics of the VCO operation are shown in Figs. 27-30.  *Fig. 47 - Frequency characteristic of VCO operating with offset: f_o = center frequency; $2f_L$ = frequency lock range.*
	PC1 or PC2	**Selection of R1, R2 and C1** Given f_o and f_L, offset frequency, f_{min}, may be calculated from $f_{min} \approx f_o - 1.6\ f_L$. Obtain the values of C1 and R2 by using Figs. 27-30. Calculate the value of R1 from the value of C1 and the product R1C1.

APPLICATION INFORMATION (Cont'd)

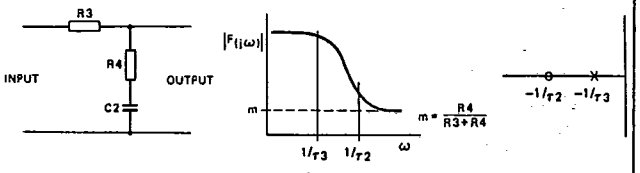
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL Conditions with No Signal at the SIG_{IN} Input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = ½ V_{CC} (see Fig. 2).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = -360° and V_{VCOIN} = 0 V (see Fig. 4).
PLL Frequency Capture Range	PC1 or PC2	**Loop Filter Component Selection**
PLL Locks on Harmonics at Center Frequency	PC1	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2	Low
AC Ripple Content When PLL is Locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°



(a) τ_1 = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram

A small capture range ($2f_c$) is obtained if $\tau > 2f_c \approx (1/\pi)\ (2\pi f_L/\tau_1)^{1/2}$

Fig. 48 - Simple loop filter for PLL without offset.



(a) τ_2 = R4 x C2; (b) amplitude characteristic (c) pole-zero diagram

τ_3 = (R3 + R4) x C2

Fig. 49 - Simple loop filter for PLL with offset.

Lock Detector Circuit

The lock detector feature is very useful in data synchronization, motor speed control, and demodulation. By adjusting the value of the lock detector capacitor so that the lock output will change slightly before actually losing lock, the designer can create an "early warning" indication allowing corrective measures to be implemented. The reverse is also true, especially with motor speed controls, generators, and clutches that must be set up before actual lock occurs or disconnected during loss of lock.

When using phase comparator 1, the detector will only indicate a lock condition on the fundamental frequency and not on the harmonics, which PC1 will lock on.