TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C
HIGH-PERFORMANCE LATCHED-INPUT *PAL*® CIRCUITS

D2709, DECEMBER 1982 – REVISED AUGUST 1989

- **High-Performance Operation . . . 30 MHz**
- **Preload Capability on Output Registers**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALT19L8	11	2	2	0	6
'PALT19R4	11	0	0	4 (3-state buffers)	4
'PALT19R6	11	0	0	6 (3-state buffers)	2
'PALT19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type transparent latches on the inputs. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

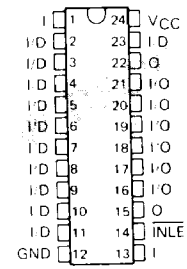
A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT LATCH FUNCTION TABLE

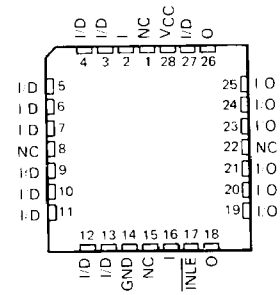
$\overline{INLE}$	D	LATCH OUTPUT
L	L	L
L	H	H
H	X	Q_0

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a trademark of Monolithic Memories Inc.

TIBPALT19L8'
JW OR NT PACKAGE
(TOP VIEW)



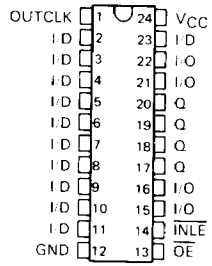
TIBPALT19L8'
FN PACKAGE
(TOP VIEW)



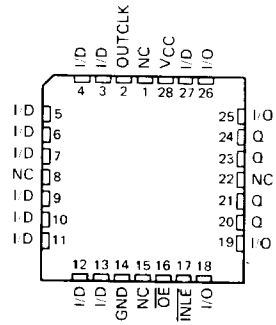
NC No internal connection

Pin assignments in operating mode

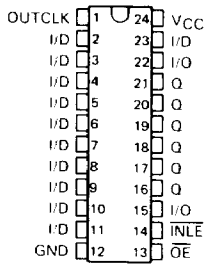
TIBPALT19R4'
JW OR NT PACKAGE
(TOP VIEW)



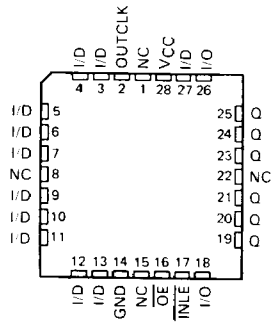
TIBPALT19R4'
FN PACKAGE
(TOP VIEW)



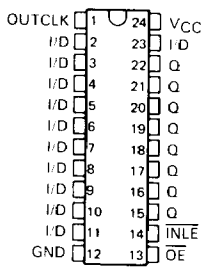
TIBPALT19R6'
JW OR NT PACKAGE
(TOP VIEW)



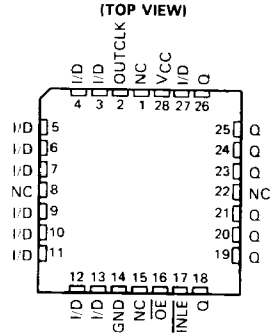
TIBPALT19R6'
FN PACKAGE
(TOP VIEW)



TIBPALT19R8'
JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19R8'
FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

TEXAS INSTRUMENTS
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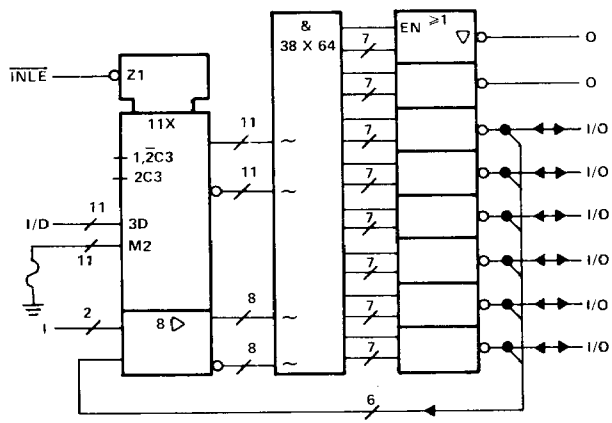
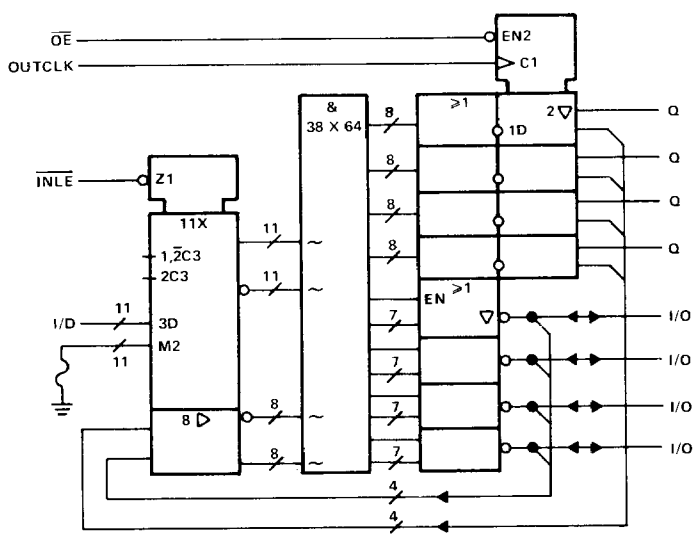
functional block diagrams (positive logic)

'PALT19L8

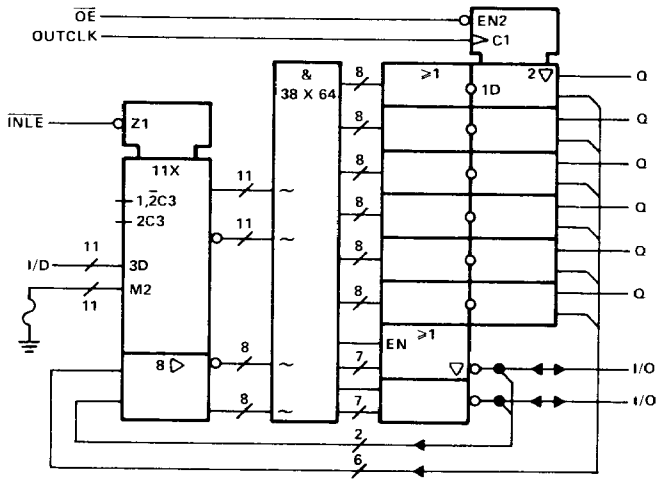


'PALT19R4

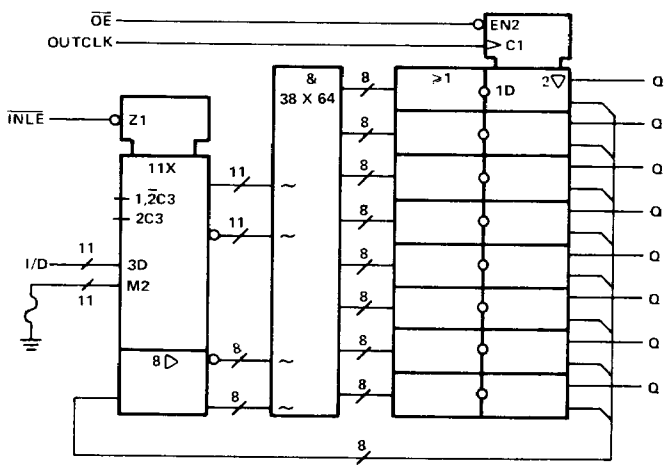


functional block diagrams (positive logic)

'PALT19R6



'PALT19R8



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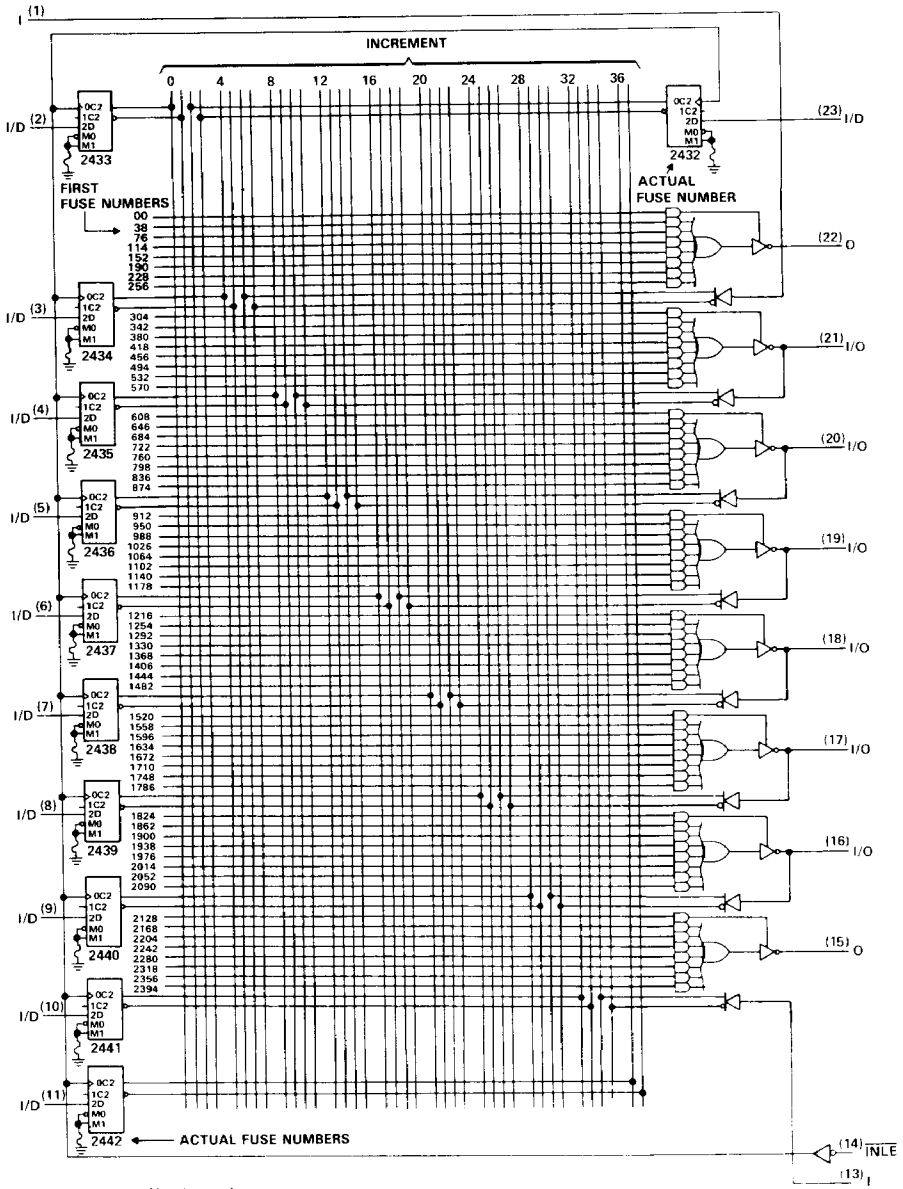
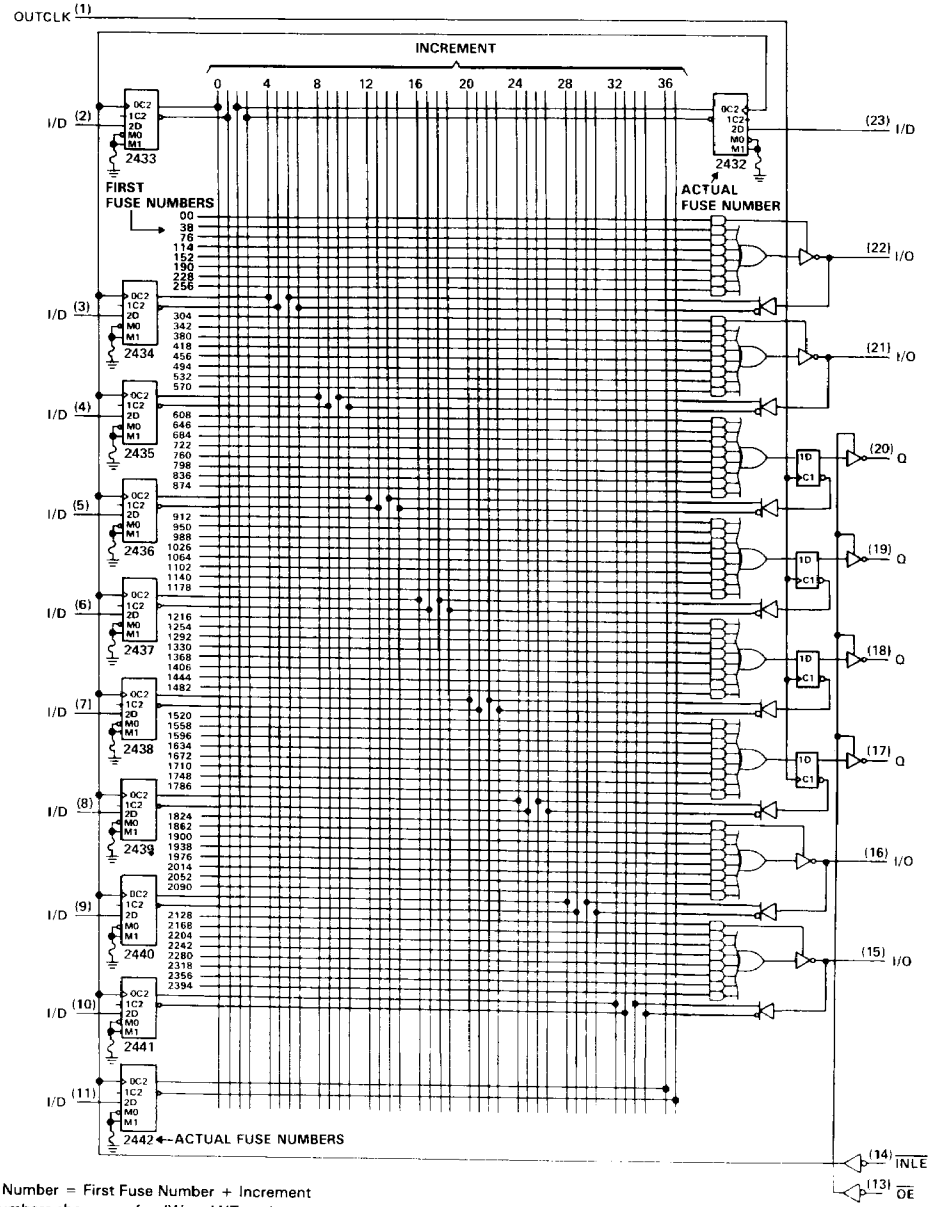
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

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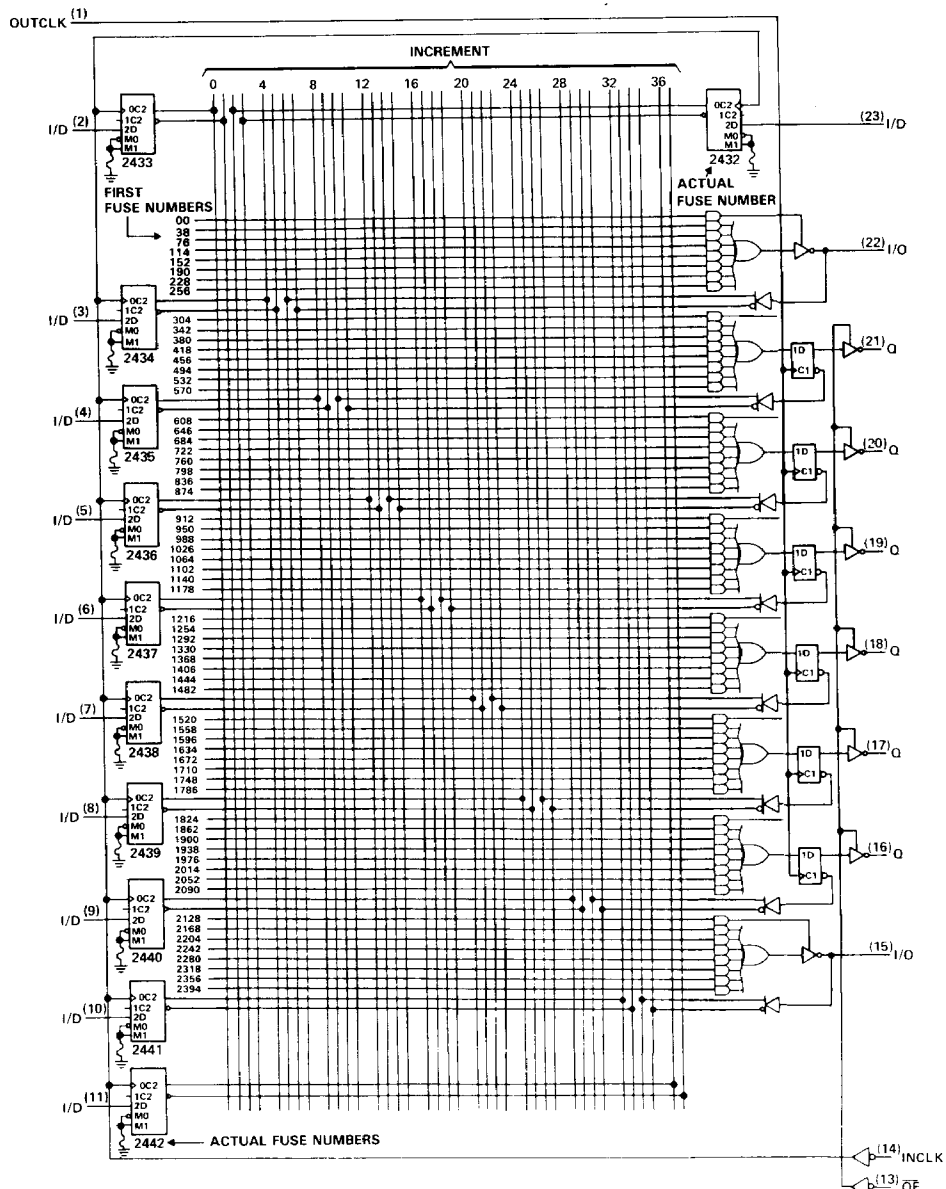
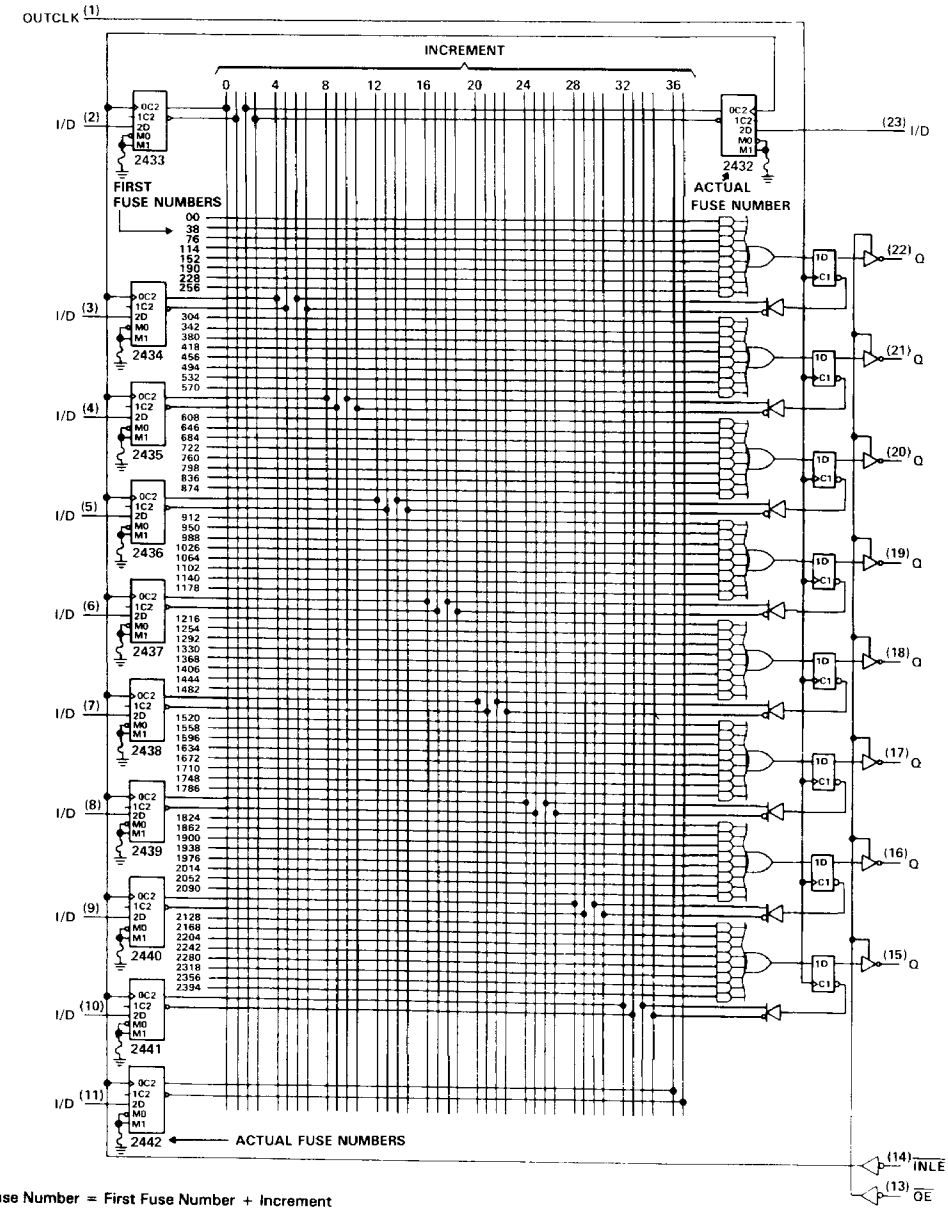
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment
Pin numbers shown are for JW and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency	OUTCLK	0		30	MHz
t_w	Pulse duration	$\overline{INLE}$ low	15			ns
		OUTCLK high	15			
		OUTCLK low	15			
t_{su}	Setup time	Data before $\overline{INLE}$ ↑	10			ns
		Data before OUTCLK↑	25			
		$\overline{INLE}$ low before OUTCLK↑ (See Note 2)	30			
t_h	Hold time	Data after $\overline{INLE}$ ↑	5			ns
		Data after OUTCLK↑	0			
T_A	Operating free-air temperature		0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input latches.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = 5.25 V,	V_{IH} = 0.4 V			−20	μA
	I/O ports					−250	
I_I	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
	All others					0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 2.7 V			40	μA
	All others					20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.4	mA
	All others					−0.2	
I_O‡		V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open	V_I = 0 V,		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	OUTCLK↑	Q	R1 = 500 Ω, R2 = 500 Ω, C_L = 50 pF, See Figure 1	30			MHz
t_{pd}	I, I/O	I/O, O			15	25	ns
t_{pd}	I/D§	I/O, O			25	40	ns
t_{pd}	$\overline{INLE}$↓	I/O, O			28	40	ns
t_{pd}	OUTCLK↑	Q			10	20	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{en}	I, I/O	I/O, O			14	25	ns
t_{en}	I/D§	I/O, O			30	40	ns
t_{en}	$\overline{INLE}$↓	I/O, O			30	40	ns
t_{dis}	$\overline{OE}$↑	Q			11	20	ns
t_{dis}	I, I/O	I/O, O			12	25	ns
t_{dis}	I/D§	I/O, O			14	25	ns
t_{dis}	$\overline{INLE}$↓	I/O, O			14	25	ns

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.
§ Input configured as an input buffer or $\overline{INLE}$ low.

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programming information

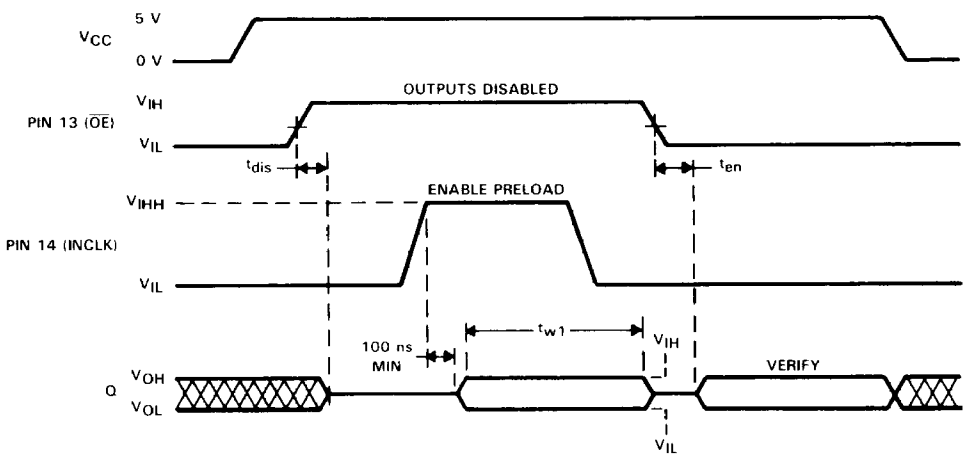
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

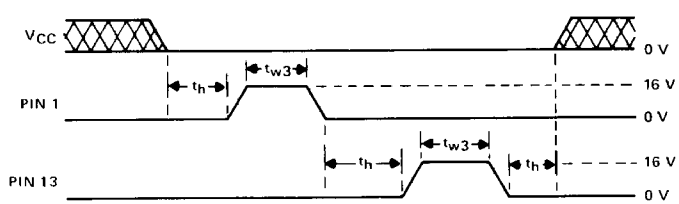
preload procedure for registered outputs (see Note 3)

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}
Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}
Step 7 Check the output states to verify preload.

preload waveforms (see Note 3)

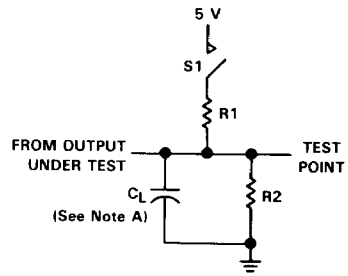


security fuse programming (see Note 3)

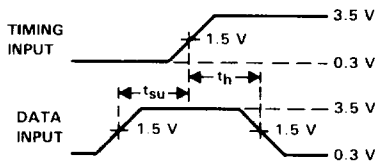


NOTE 3: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

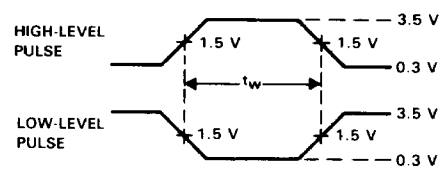
PARAMETER MEASUREMENT INFORMATION



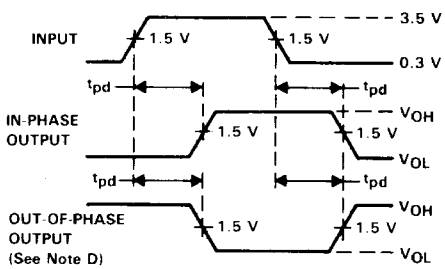
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



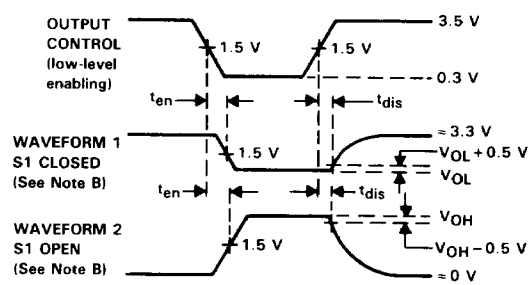
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

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