ICS853111-01

LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-3.3V LVPECL/ECL FANOUT BUFFER

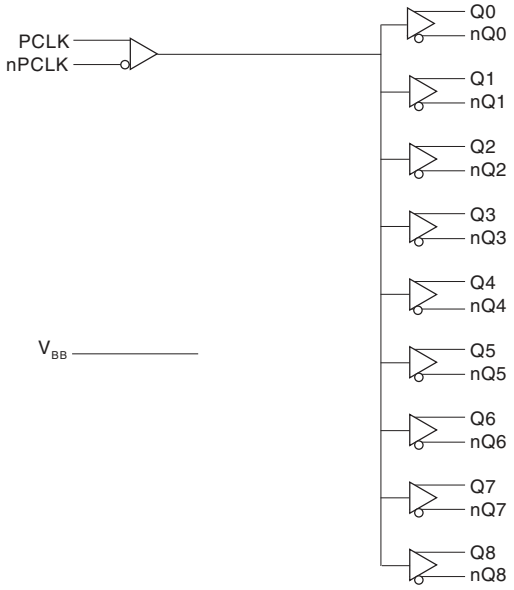
GENERAL DESCRIPTION

The ICS853111-01 is a low skew, high performance 1-to-9 Differential-to-3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The PCLK, nPCLK pair can accept LVPECL, CML and SSTL differential input levels. The ICS853111-01 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853111-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

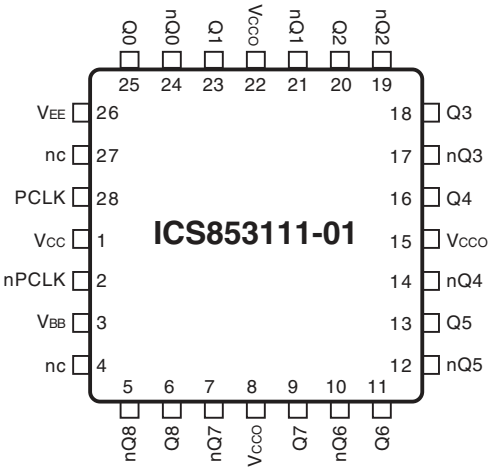
FEATURES

- 9 differential 3.3V LVPECL / ECL outputs
- 1 differential LVPECL input pair
- PLCK, nPLCK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >2GHz (typical)
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Additive phase jitter, RMS: 0.03ps (typical)
- Output skew: 35ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 675ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 3V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3V to -3.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



28-Lead PLCC
11.6mm x 11.4mm x 4.1mm package body
V Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CC}	Power		Core supply pin.
2	nPCLK	Input	Pullup/ Pulldown[1]	Inverting differential LVPECL clock input. Bias to V_{CC}/2 w/no input.
3	V_{BB}	Output		Bias voltage.
4, 27	nc	Unused		No connect.
5, 6	nQ8, Q8	Output		Differential output pair. LVPECL interface levels.
7, 9	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
8, 15, 22	V_{CCO}	Power		Output supply pins.
10, 11	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
12, 13	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
14, 16	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
21, 23	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
24, 25	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
26	V_{EE}	Power		Negative supply pin.
28	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				1	pF
R_{PULLUP}	Input Pullup Resistor			50		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{PULLDOWN}$[1]	Input Pulldown Resistor			50		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (LVECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (LVECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	37.8°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. LVPECL POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3V TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.0	3.3	3.8	V
V_{CCO}	Output Supply Voltage		3.0	3.3	3.8	V
I_{EE}	Power Supply Current				75	mA

Table 3B. LVPECL DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 3C. ECL POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3V TO -3.8V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{EE}	Supply Voltage		-3.0	-3.3	-3.8	V
I_{EE}	Power Supply Current			55		mA

Table 3D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -3V to -3.8V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

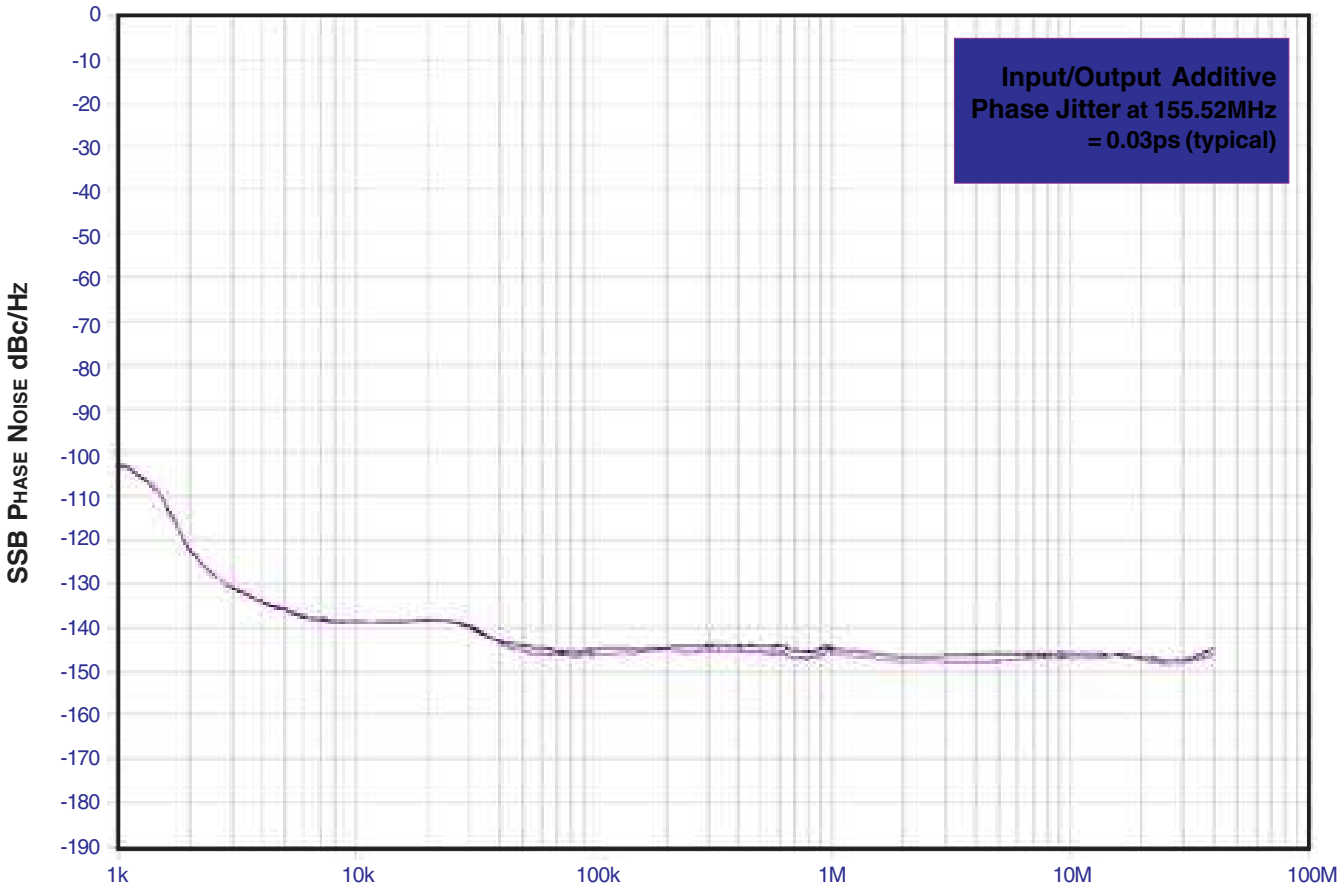
TABLE 4. AC CHARACTERISTICS, V_{CC} = 3V TO 3.8V; V_{EE} = 0V OR V_{CC} = 0V; V_{EE} = -3V TO -3.8V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			>2			>2			>2		GHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		350	500	650	385	525	675	410	350	700	ps
tp_{HL}	Propagation Delay, High to Low; NOTE 1		450	600	750	480	620	760	515	650	785	ps
*t*sk(o)	Output Skew; NOTE 2, 4			20	35		20	35		20	35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				200			200			200	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.03			0.03			0.03		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	90	200	315	100	203	310	95	210	300	ps

All parameters measured at f ≤ 1GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

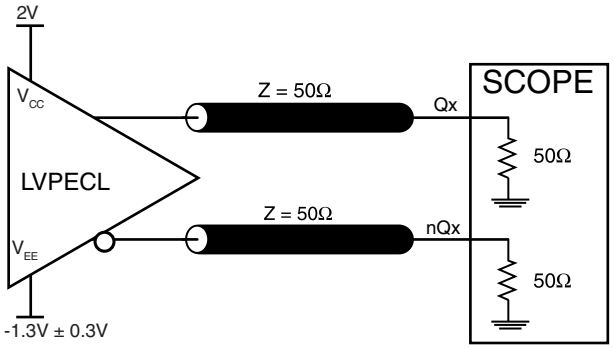
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

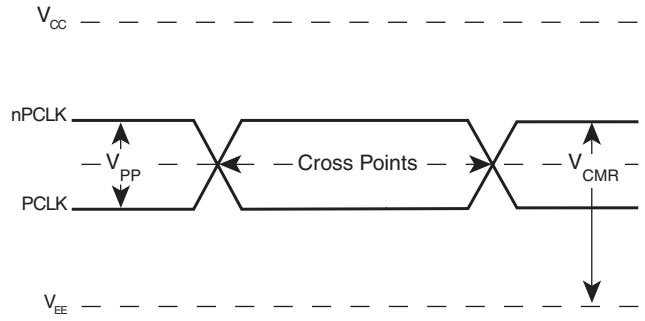


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

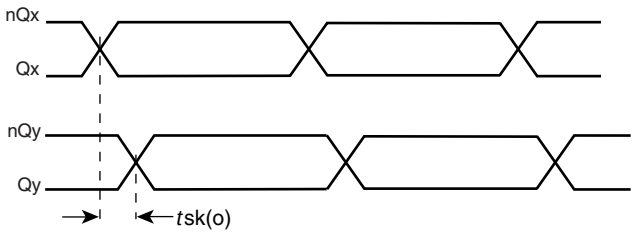
PARAMETER MEASUREMENT INFORMATION



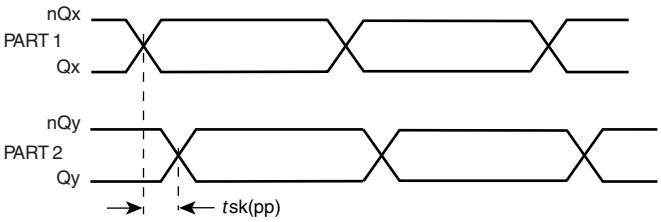
OUTPUT LOAD AC TEST CIRCUIT



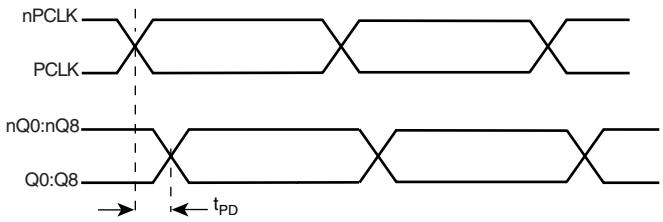
DIFFERENTIAL INPUT LEVEL



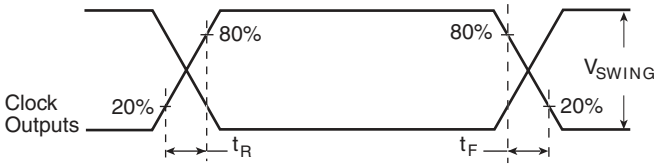
OUTPUT SKEW



PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows an example of the differential input that can be wired to accept single ended levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

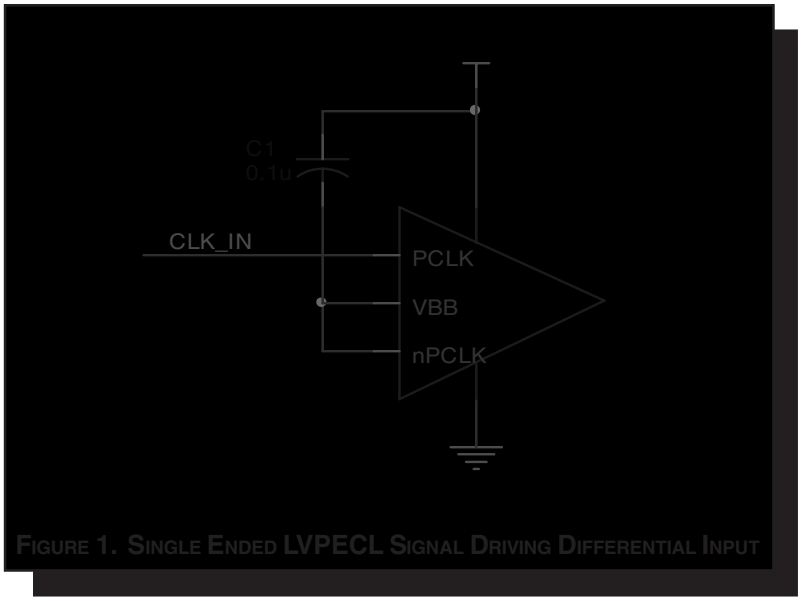


FIGURE 1. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

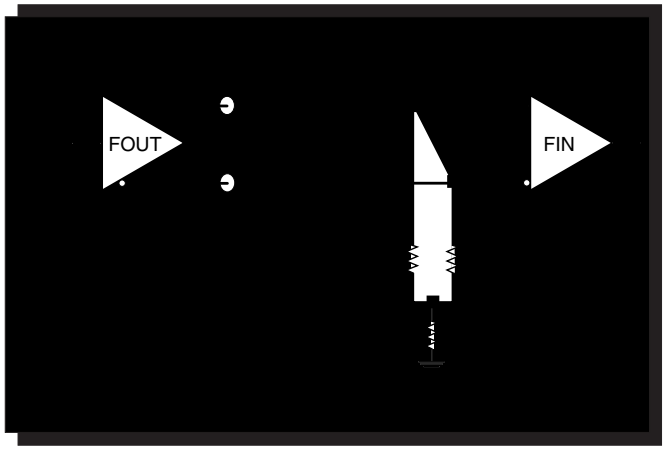


FIGURE 2A. LVPECL OUTPUT TERMINATION

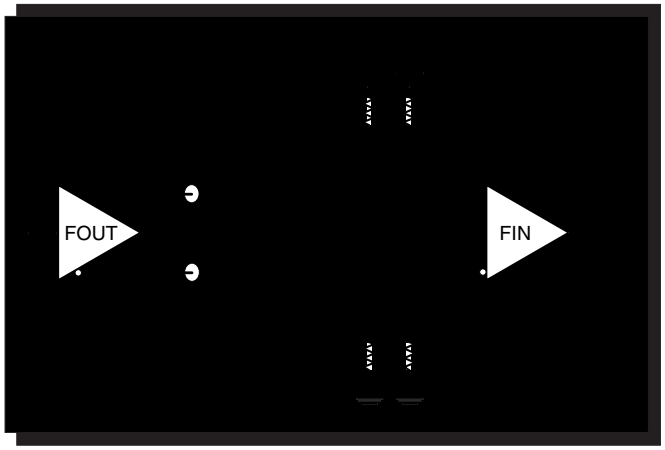


FIGURE 2B. LVPECL OUTPUT TERMINATION

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

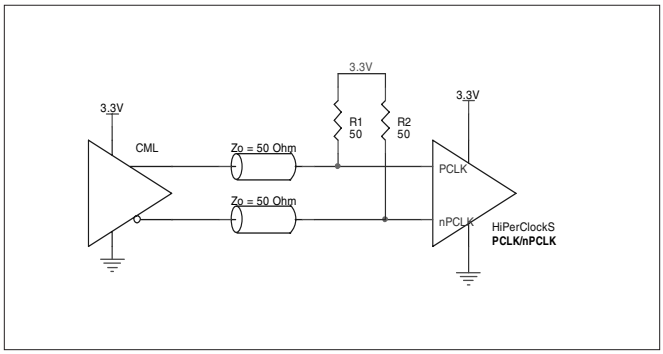


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

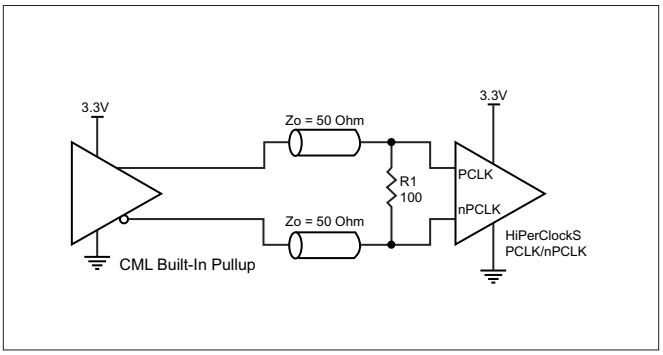


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

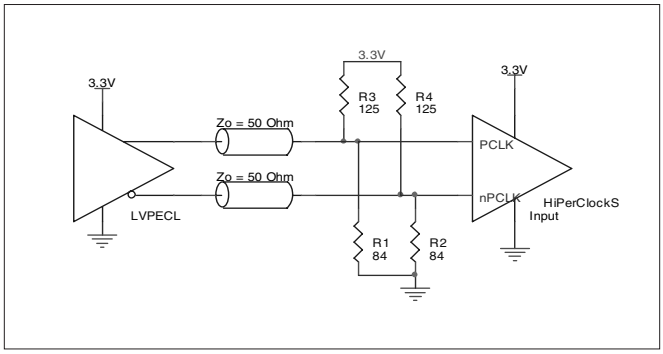


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

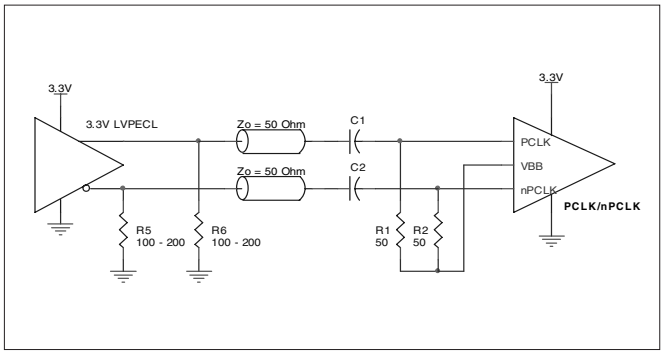


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

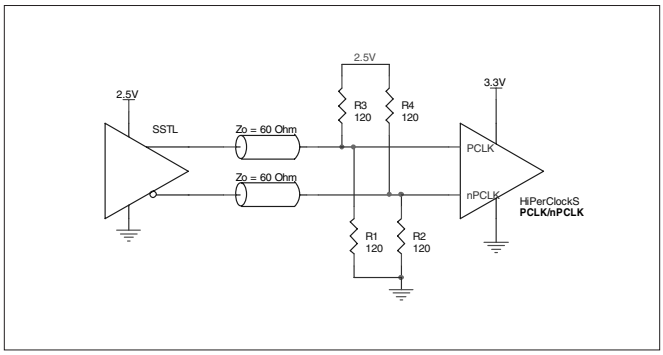


FIGURE 3E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

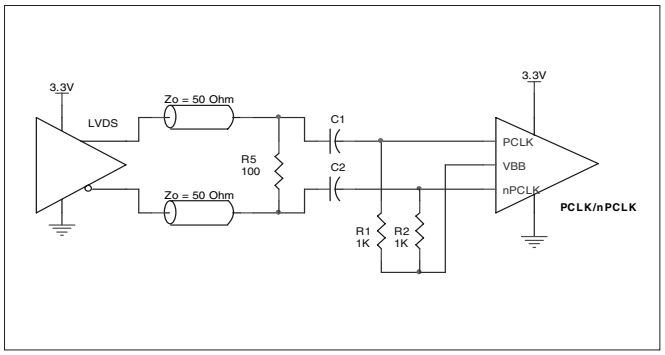


FIGURE 3F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

SCHEMATIC EXAMPLE

This application note provides general design guide using ICS853111-01 LVPECL buffer. *Figure 4* shows a schematic example of the ICS853111-01 LVPECL clock buffer. In this example, the input is driven by an LVPECL driver.

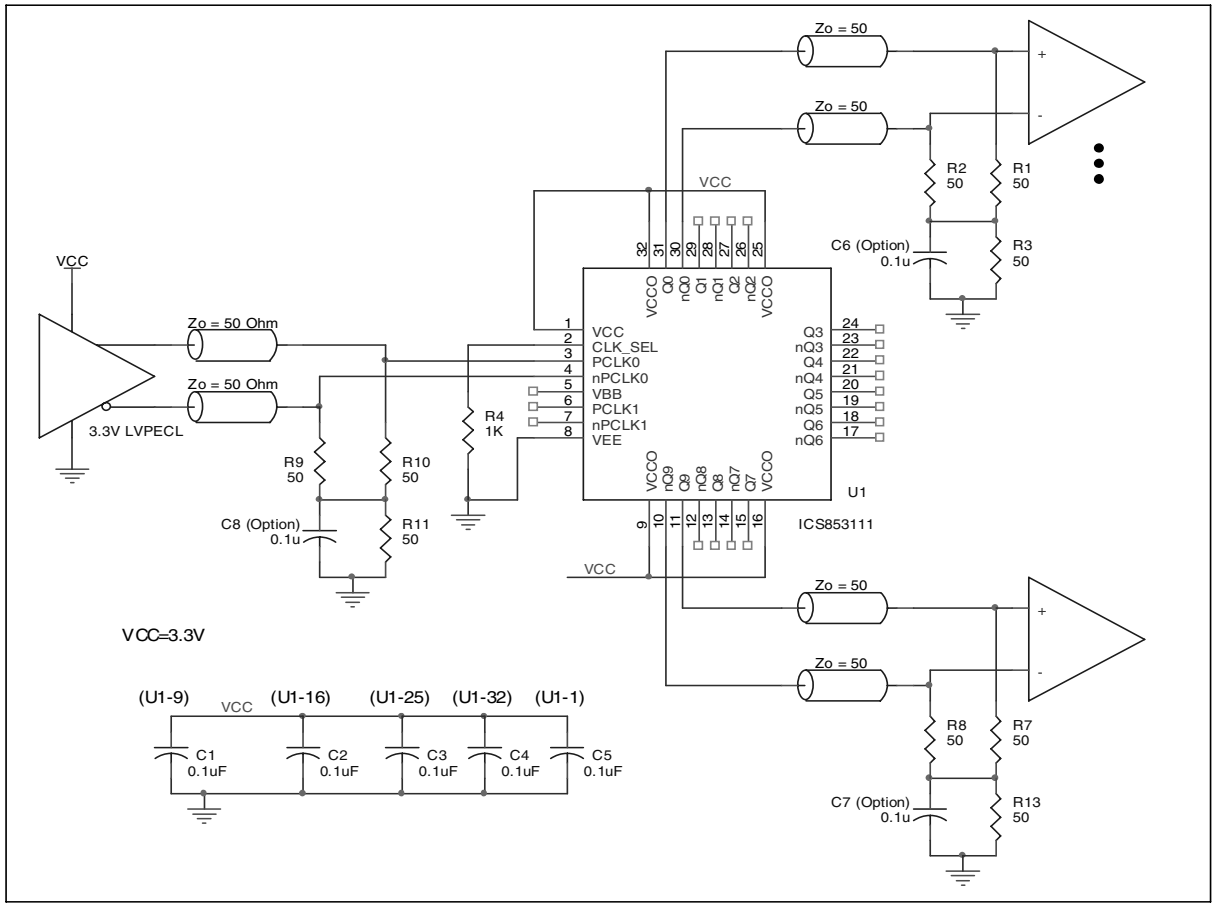


FIGURE 4. EXAMPLE ICS853111-01 LVPECL CLOCK OUTPUT BUFFER SCHEMATIC

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853111-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853111-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 75mA = **285mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 9 * 30.94mW = **278.5mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 285mW + 278.5mW = **563.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.564W * 31.1°C/W = 102°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 28-PIN PLCC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 5.

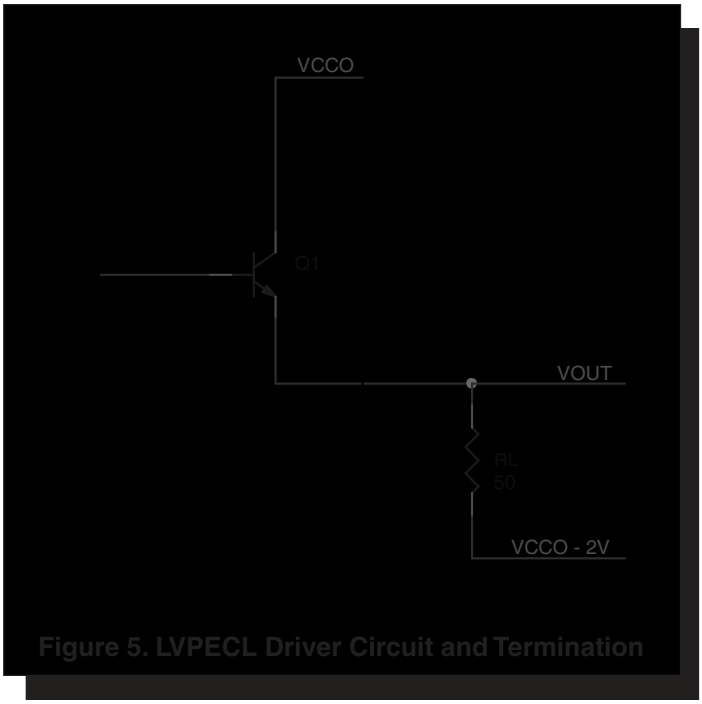


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX}} \mathbf{- 0.935V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.935V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX}} \mathbf{- 1.67V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD PLCC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS853111-01 is: 265

Pin compatible with MC100LVE111

PACKAGE OUTLINE - V SUFFIX FOR 28 LEAD PLCC

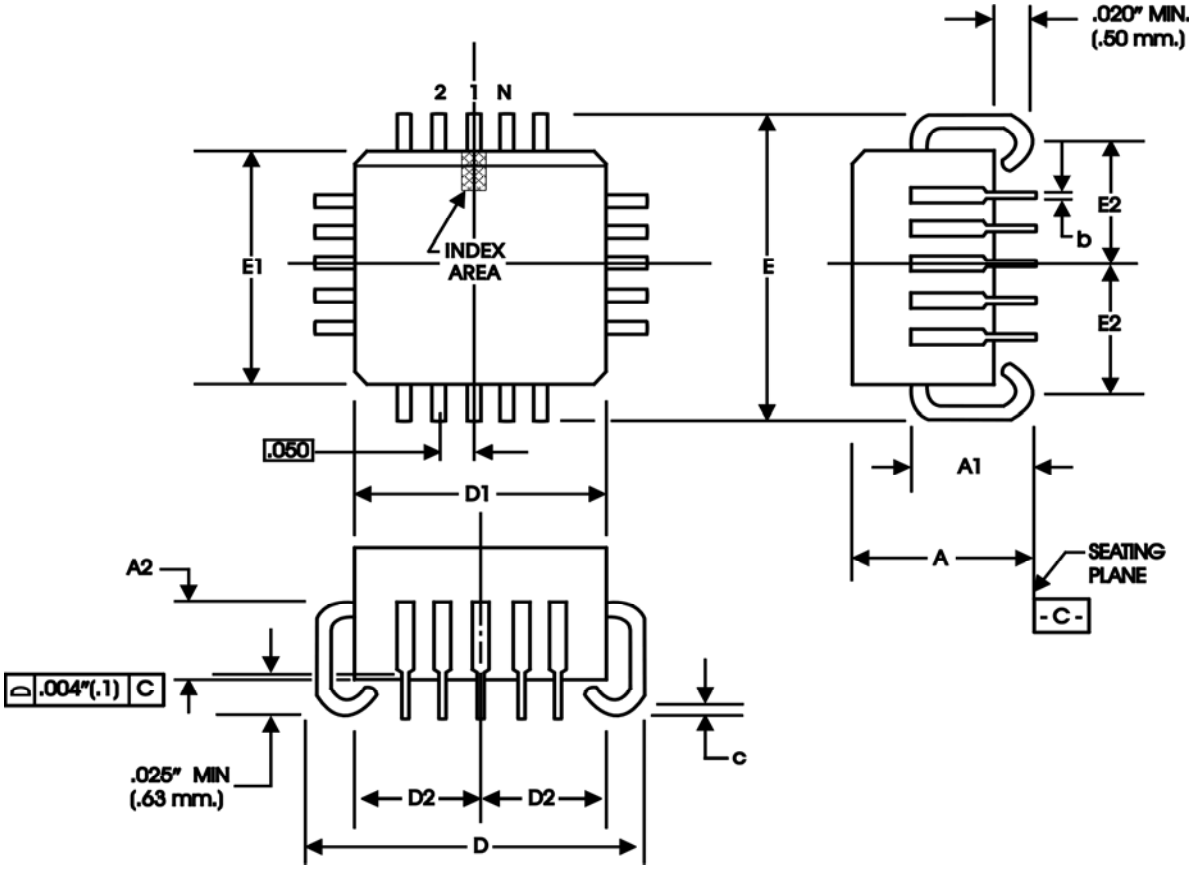


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D	12.32	12.57
D1	11.43	11.58
D2	4.85	5.56
E	12.32	12.57
E1	11.43	11.58
E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853111AV-01	ICS853111AV-01	28 Lead PLCC	Tube	-40°C to 85°C
853111AV-01T	ICS853111AV-01	28 Lead PLCC	500 Tape & Reel	-40°C to 85°C
853111AV-01LF	ICS853111AV01L	28 Lead "Lead-Free" PLCC	Tube	-40°C to 85°C
853111AV-01LFT	ICS853111AV01L	28 Lead "Lead-Free" PLCC	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the pat number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
		1 5	Features Section - added Lead-Free bullet. Added Additive Phase jitter section.	4/25/05
A	T8	14	Ordering Information Table - Added Lead-free marking	11/14/07