THS8135EVM Evaluation Module

User's Guide

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THS8135EVM Evaluation Module

1 Functional Description

The THS8135EVM is a four-layer printed circuit board designed for evaluation of the THS8135 or THS8136 triple DAC. A TVP7002 video and graphics digitizer is included on THS8135EVM for digitizing analog RGB graphics inputs, providing a digital source for evaluation of the THS8135. The THS8135EVM is configured for support of RGB graphics formats. The maximum conversion rate of the EVM is 162MSPS providing support for graphics formats up to UXGA – 60 Hz. I^2C communication with the EVM is provided by a host PC USB port and the Video Control Center (VCC) software tool provided with the EVM.

1.1 Description Overview

The THS8135EVM is powered by both a 5-VDC universal supply and a host PC USB connection. The 5-VDC input is used to supply on-board 1.8-V and 3.3-V voltage regulators that provide power for the majority board. The 5-V USB power provides power for the USB interface and associated I^2C circuitry required for TVP7002 register programming.

The TVP7002 triple ADC converts three channels of analog graphics RGB input into digital RGB data. This digital data and associated clock from the TVP7002 are sent indirectly to the THS8135 through a 3.3-V/1.8-V level translator. The HSYNC and VSYNC synchronization signals required for RGB graphics are supplied by the TVP7002, bypassing the THS8135.

Control of the THS8135EVM is provided by Video Control Center (VCC), a Windows-based application developed by Texas Instruments and provided free of charge. This application uses a USB port on the PC to provide I^2C communication to the THS8135EVM. VCC provides a graphics user interface and a register level interface that can be used to program various registers in the TVP7002 Triple ADC. An initialization file is included that provides preconfigured setups for some of the more common PC graphics formats.

2 Board Level Description

This chapter describes the various features available on the THS8135EVM. Figure 1 shows the block diagram for the THS8135EVM.

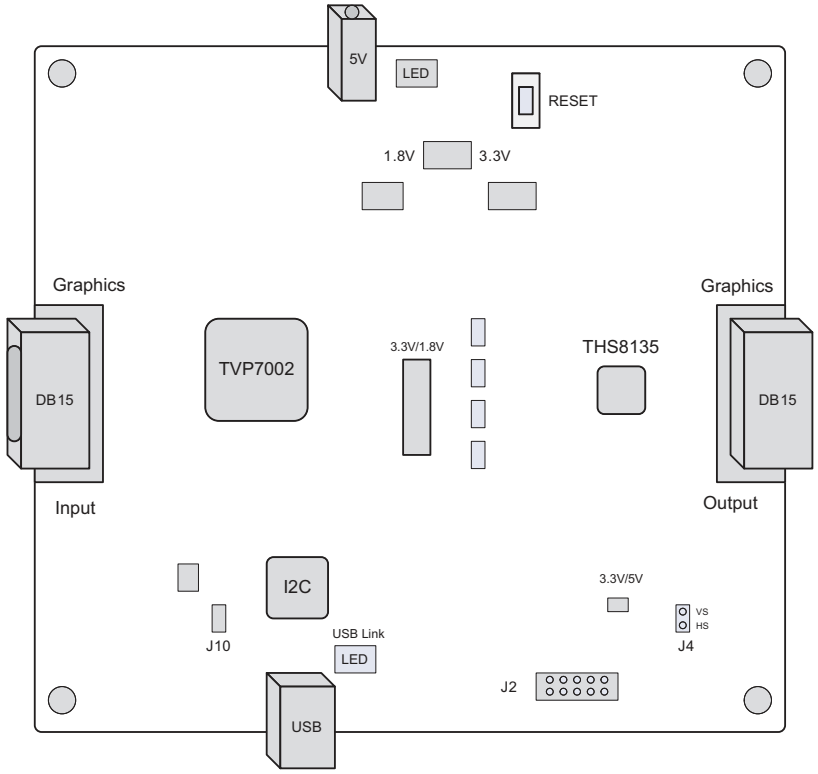

Figure 1. THS8135EVM Block Diagram

2.1 Analog Inputs and Outputs

The THS8135EVM is designed to allow evaluation of the THS8135 triple DAC through use of the TVP7002 triple ADC configured for RGB graphics support. One standard DB15 graphics input connector is provided for input, and another DB15 connector is provided for output and connection to a monitor. Footprints for ferrite beads are provided on the RGB input and output signal paths, but are factory populated with 0-Ω resistors to provide maximum RGB bandwidth.

The THS8135 DACs are current-steering DACs designed to directly drive a doubly terminated 75-Ω load. One 75-Ω load resistor is present on the EVM board at each DAC output. The other 75-Ω termination is typically present in the monitor. When viewing the DAC outputs on an oscilloscope, a 75-Ω termination resistor is required at the oscilloscope input to provide the correct load and voltage level. The full-scale output current supplied by the THS8135 DACs may be adjusted by the resistor connected to the THS8135 FSADJ pin. The factory installed resistors should provide a full-scale output range near 700 mV when the THS8135EVM outputs are terminated with 75 Ω.

2.2 USB Interface and Power

A USB cable must be connected between the host PC and THS8135EVM. The USB interface provides the I^2C communications required for programming the TVP7002 and also provides the power required for the TUSB3210 and associated USB to I^2C circuitry. A 5-V power jack (J8) is also provided on the board to provide power for the rest of the board. Voltage regulators on the EVM are used to generate the 1.8-V and 3.3-V power supply levels required for the components on the board. LEDS are included on the board to indicate the presence of 5-V power and USB connectivity. The J10 jumper must be installed for proper USB operation.

2.3 Test Points

The test points shown Table 1 in are provided on the THS8135EVM to assist in trouble-shooting and signal monitoring.

Table 1. Test Points

Test Point Designator	Function	Description
TP1	SDA	I^2C data
TP2	SCL	I^2C clock
TP3, TP6, TP8, TP10	GND	Ground
TP4	3.3 V	3.3-V main for the TVP7002 and THS8135
TP5	1.8 V	1.8-V main for the TVP7002 and THS8135
TP9	DCLK	Data clock from the TVP7002
J4	HS and VS	Horizontal and vertical sync signals

2.4 THS8135 Control Signals

The operating mode of the THS8135 is determined from the state of the logic control signals shown in Table 2. The THS8135EVM is configured for generic RGB DAC operation by default. The J2 header may be used for evaluation of the control inputs. Please refer to the THS8135 or THS8136 datasheet for more information on the control inputs.

NOTE: The BLANK/ and SYNC/ inputs have priority over the RGB inputs. When at logic low levels, these signals will force the DAC outputs to sync or blank levels.

Table 2. THS8135 Control Signals

Control Signal	Default	Description
BLANK/	High	Blank level insertion disabled
SYNC/	High	Sync insertion disabled
SYNC-T	High	Positive sync insertion enabled
M1	Low	M1 set for generic DAC operation
M2	Low	M2 set for generic DAC operation

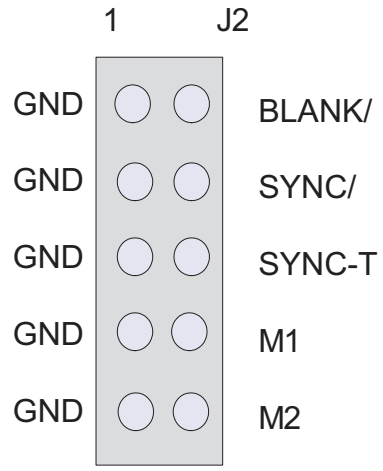

Figure 2. J2 Control Input Header

3 Software Installation

The following summarizes the steps for setup and operation of the THS8135EVM. If THS8135EVM software has been previously installed on the PC, you will be prompted to first uninstall the previous version.

3.1 Uninstalling Previous Version

If the dialog box in Figure 3 appears, select Remove THS8135EVM Software and Finsh to remove the software.

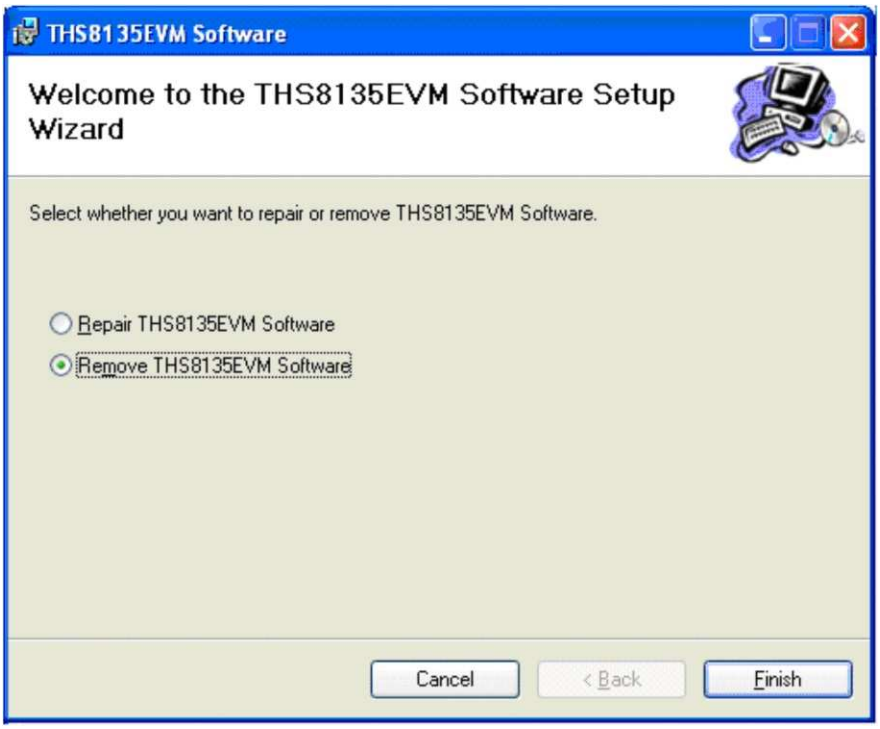

Figure 3. THS8135EVM Software Removal

Alternatively, the THS8135EVM software may be removed by following these steps:

1. Start > Control Panel > Add or Remove Programs
2. Wait for the list to populate.
3. Scroll down and click on THS8135EVM Software to highlight it.
4. Click the remove button.
5. When prompted with Are you sure you want to remove the THS8135EVM Software from your computer?, click Yes.

3.2 THS8135EVM Software Installation

All necessary software for the THS8135EVM is provided on the enclosed CD-ROM. Both the EVM software and the device files must be installed on the PC that will be emulating the I^2C bus via the USB port. Follow these steps to install the software (see Figure 4 through Figure 7):

1. Insert the CD-ROM into the computer that will emulate the I^2C bus via the USB port.
2. Run the SETUP.EXE file to install VCC and documentation.
3. Click Next at all prompts and finally click Finish to complete the installation process.

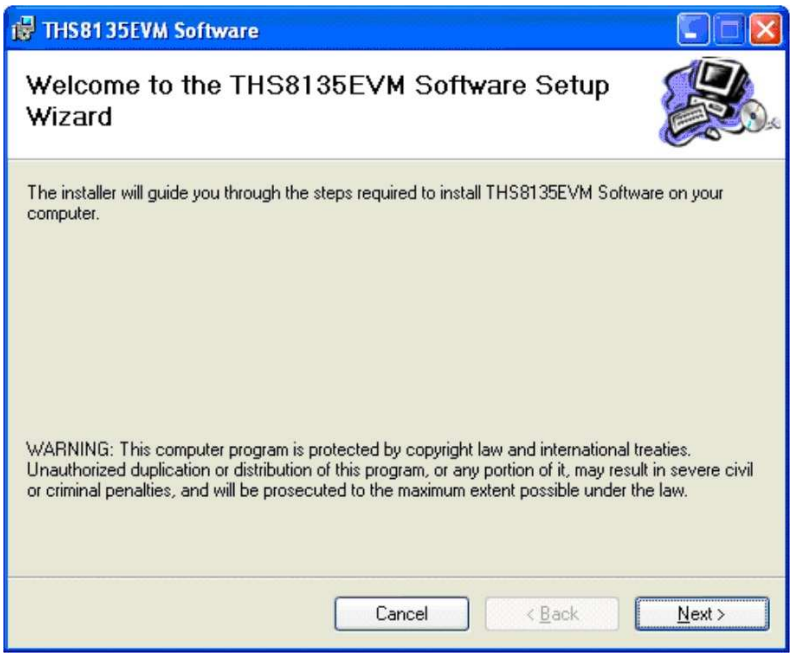

Figure 4. TVP5151EVM Software Setup Wizard

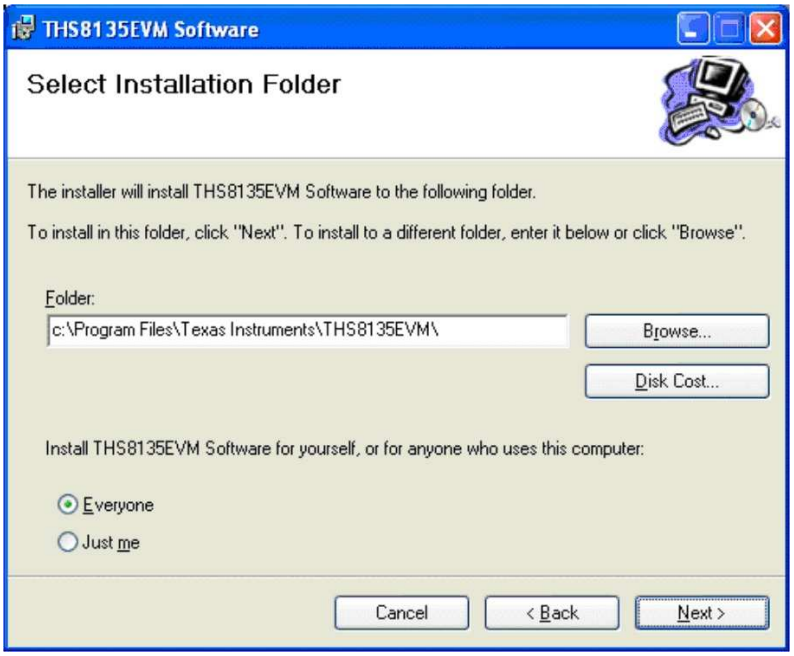

Figure 5. Select Installation Folder

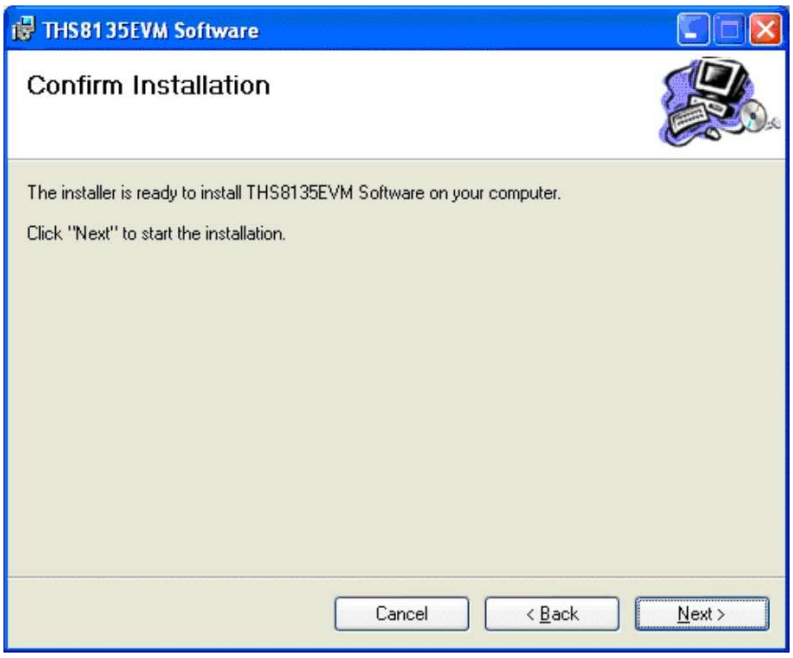

Figure 6. Confirm Installation

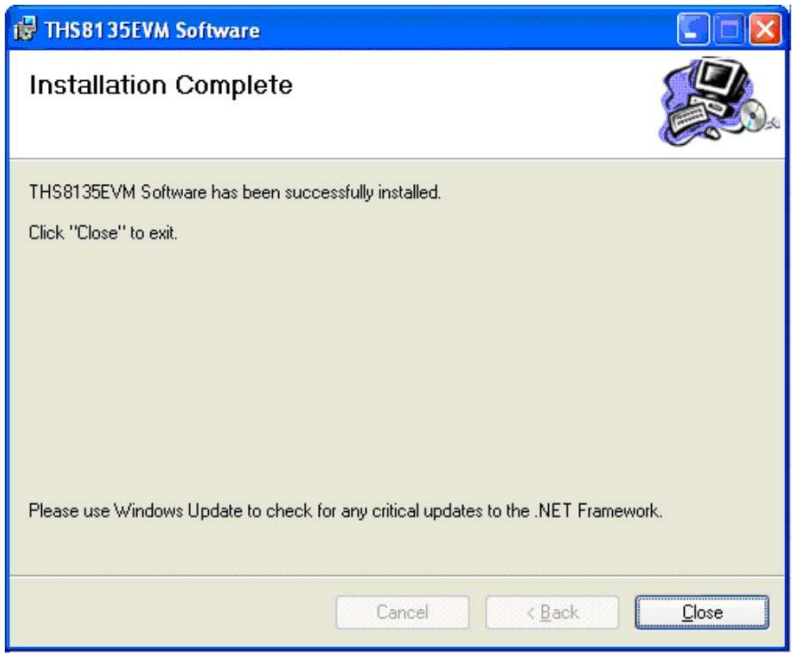

Figure 7. Installation Complete

Following installation, documentation and a shortcut to the THS8135EVM VCC application can be found in the Windows start menu at:

Start > All Programs > THS8135EVM > THS8135EVM User Guide

Start > All Programs > THS8135EVM > THS8135EVM Software

4 Hardware Setup

Figure 8 shows a typical THS8135EVM setup used for evaluation. An analog RGB graphics input must be provided by a graphics/video source such as a pattern generator or PC. The on-board TVP7002 triple ADC digitizes the analog input and supplies digital data to the THS8135 which converts the digital data back to analog RGB for display on a graphics monitor. The host PC USB interface is used to program the TVP7002 for various RGB graphics formats up to UXGA – 60 Hz.

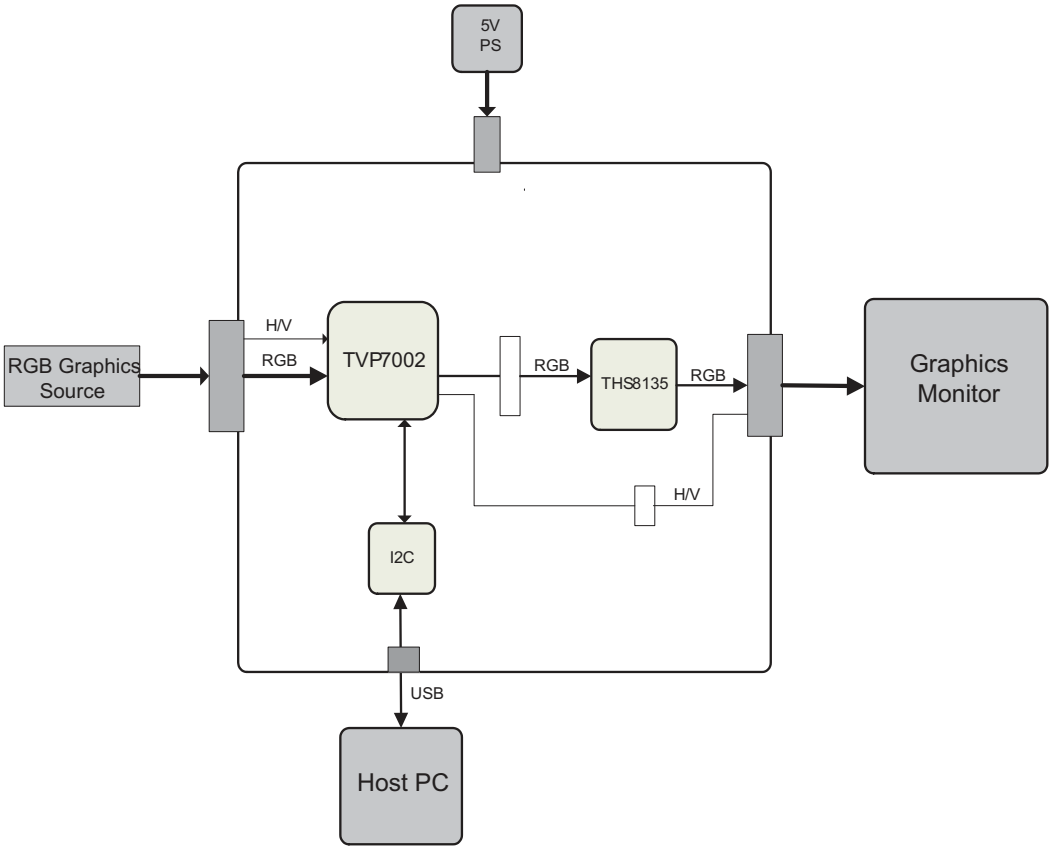

Figure 8. Typical Hardware Setup

4.1 Required Equipment

- THS8135EVM (provided)
- Universal 5-V power supply (provided)
- USB cable (provided)
- Windows-based PC
- Two DB15 PC graphics cables (provided)
- Graphics source (multi-format video/graphics signal generator)
- Display monitor that supports PC graphics

To prepare the THS8135EVM for operation:

1. Connect the USB cable from the THS8135EVM to the host PC. The green USB Link LED on the board should turn on.
2. Connect the 5-V power supply to the dc jack on the THS8135EVM board. The green power LED on the board should turn on.
3. Connect a graphics source to the DB15 input connector.
4. Connect a graphics monitor to the DB15 output connector.

5 Video Control Center (VCC) Quick Start

After THS8135EVM software installation (see Section 3) and hardware setup (see Section 4) are complete, follow these steps to bring up the THS8135EVM:

1. Following execution of VCC, the VCC Configuration screen appears (see Figure 9). This dialog box configures the I²C bus. Next to TVP7000, select the TVP7002 and ensure the I²C slave address is set to B8h

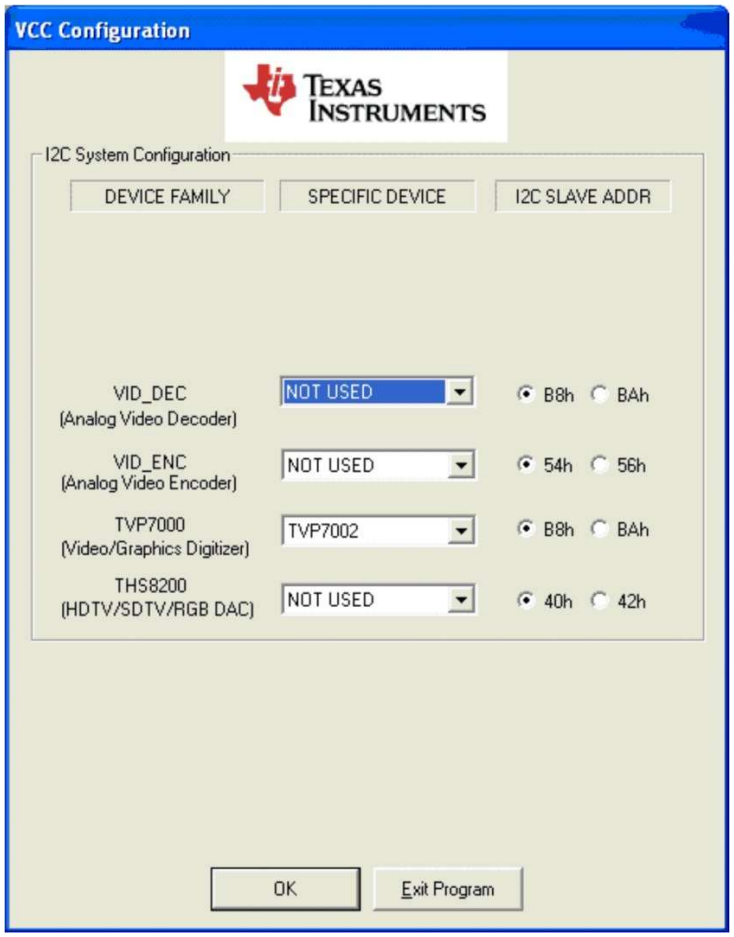

Figure 9. VCC I²C Configuration Dialog

2. Ensure that all other boxes are set to Not Used.
3. If there are no I²C communication issues, then the Main Screen window displays (see Figure 10). If I²C or USB communication issues are reported, see Section 7.2 for possible solutions.

Figure 10. VCC Main Screen

4. Load the provided Initialize.CMD file into VCC by clicking on Tools -> System Initialization. The System Initialization window opens (see Figure 11). The default directory is C:\Program Files\Texas Instruments\THS8135EVM\Initialization.
5. Click the desired "TVP7002_..." dataset in the window and then click the Program Device button to initialize the TVP7002 on the THS8135EVM.

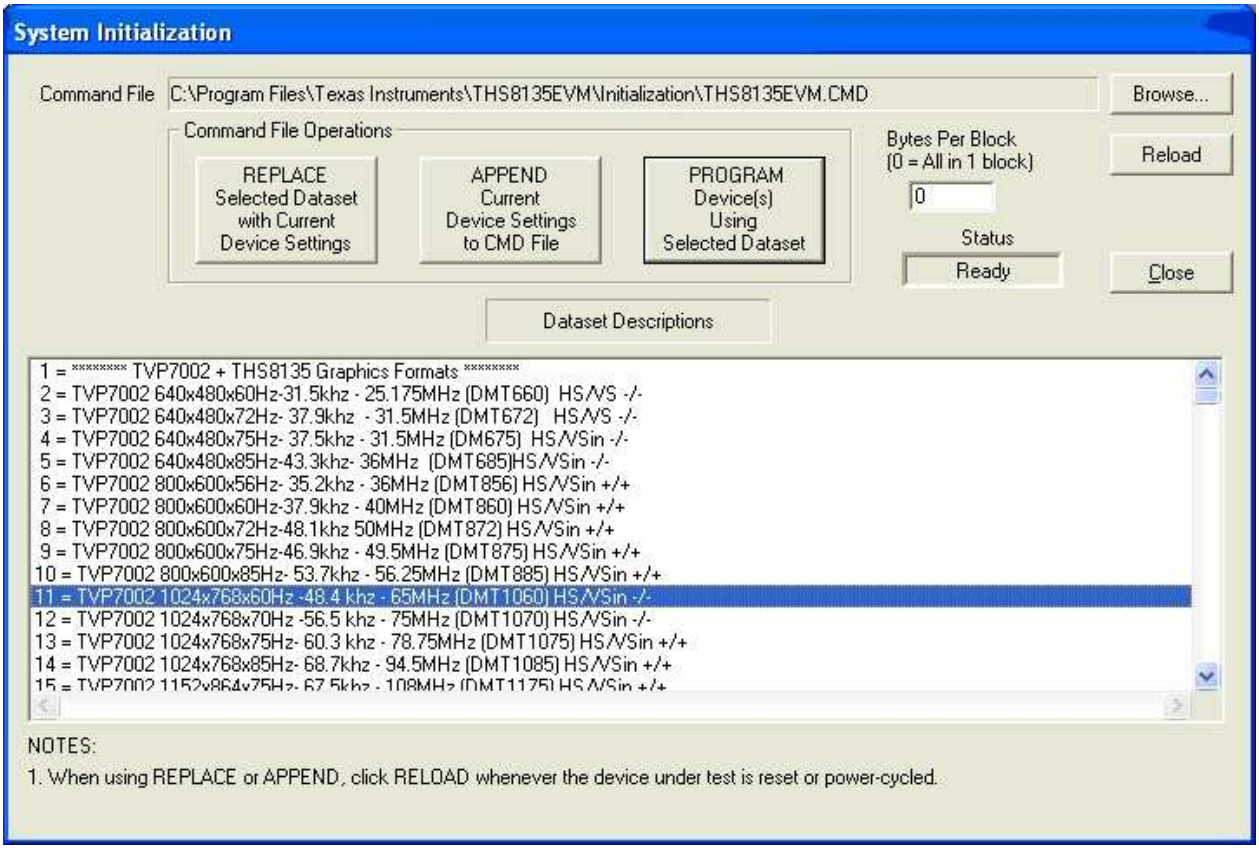

Figure 11. VCC System Initialization

6. With a graphics source provided at the DB15 graphics input connector and with the proper resolution configured, graphics should now be viewable on the display monitor.

6 VCC Operation

The following sections describe how to use VCC in depth. It discusses various features and screens which the user may encounter while evaluating the THS8135EVM.

6.1 Starting the VCC Application Program

VCC may be started by clicking on Start > All Programs > THS8135EVM > THS8135EVM Software.

6.2 VCC Configuration Dialog Box

Each time the THS8135EVM Software is started, the VCC Configuration dialog box opens, as shown in Figure 12. This is pre-configured to specify one TVP7002 device on the I^2C bus at slave address 0xB8. Click OK to begin I^2C communication.

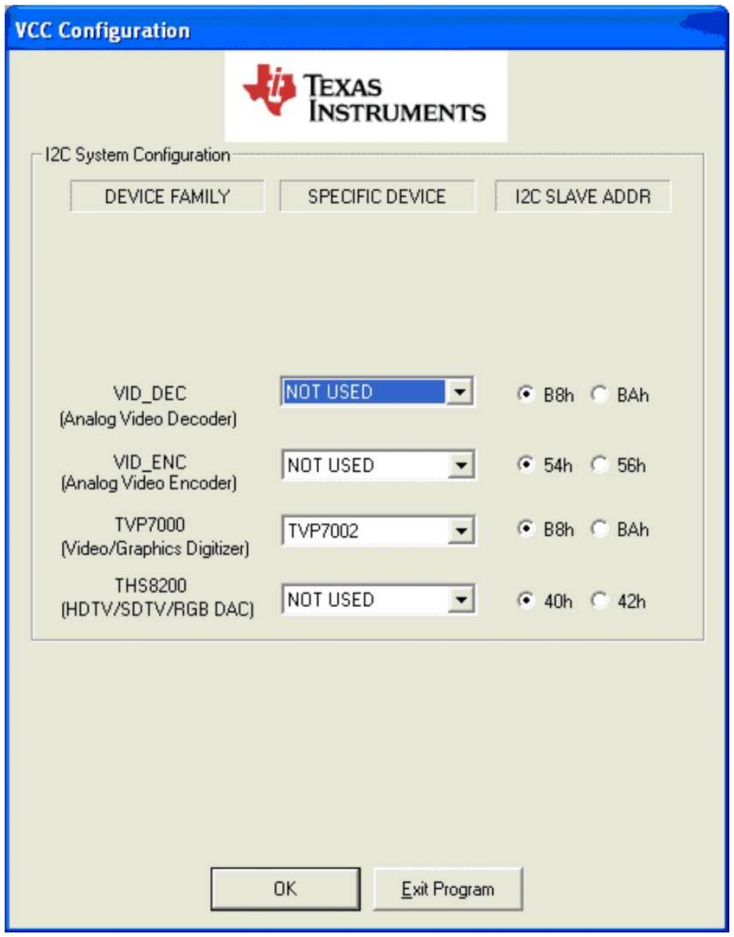

Figure 12. VCC I^2C Address Configuration

6.3 USB I^2C System Test

If a message occurs indicating that the USB device was not found (see Figure 13), disconnect the USB cable, wait three seconds, reconnect the USB cable, and click Continue. If USB or I^2C communication issues persist, see Section 7.2 for possible solutions.

Figure 13. I²C System Failure

6.4 Main Menu

If USB and I²C communications are working properly, the main menu is displayed (see Figure 14). The menus, which are used to operate VCC, are File, Edit, Tools, Window, and Help. The File menu's only function is Exit, which terminates the program. Table 3 summarizes the main menu contents.

Figure 14. Video Control Center Main Screen

Table 3. Main Menu Summary

Menu	Contents
File	Exit
Edit	Register Map TVP7002 (0xB8) Generic I²C Editor
	Property Sheets TVP7002 (0xB8)
Tools	System Initialization
	Real-time Polling (not supported on the THS8135EVM platform)
	USB/LPT/I²C Options I²C Bit Rate (100KHz or 400KHz)
Window	Allows selection of the active window. Multiple windows can be open at the same time.
Help	About VCC

6.5 System Initialization

Clicking System Initialization in the Tools menu displays the dialog box shown in Figure 15. This dialog box provides the means for initializing the TVP7002 Triple ADC for a particular graphics mode. The details of the initialization are contained in the command file (with a CMD file extension).

The command file is loaded using the Browse... button. Once the command file is opened, a text list displays descriptions of the individual data sets contained within the command file.

Click once on the desired data set description to select it. Click the Program Device(s) Using Selected Dataset button to run the selected data set, which loads the TVP7002 via the I²C bus. When the device initialization has completed, the status indicator reads Ready.

NOTE: If Ready does not display, then the TVP7002 is not initialized and the I²C bus is not communicating. See Section 7 for possible solutions.

Click the Close button to close the dialog box.

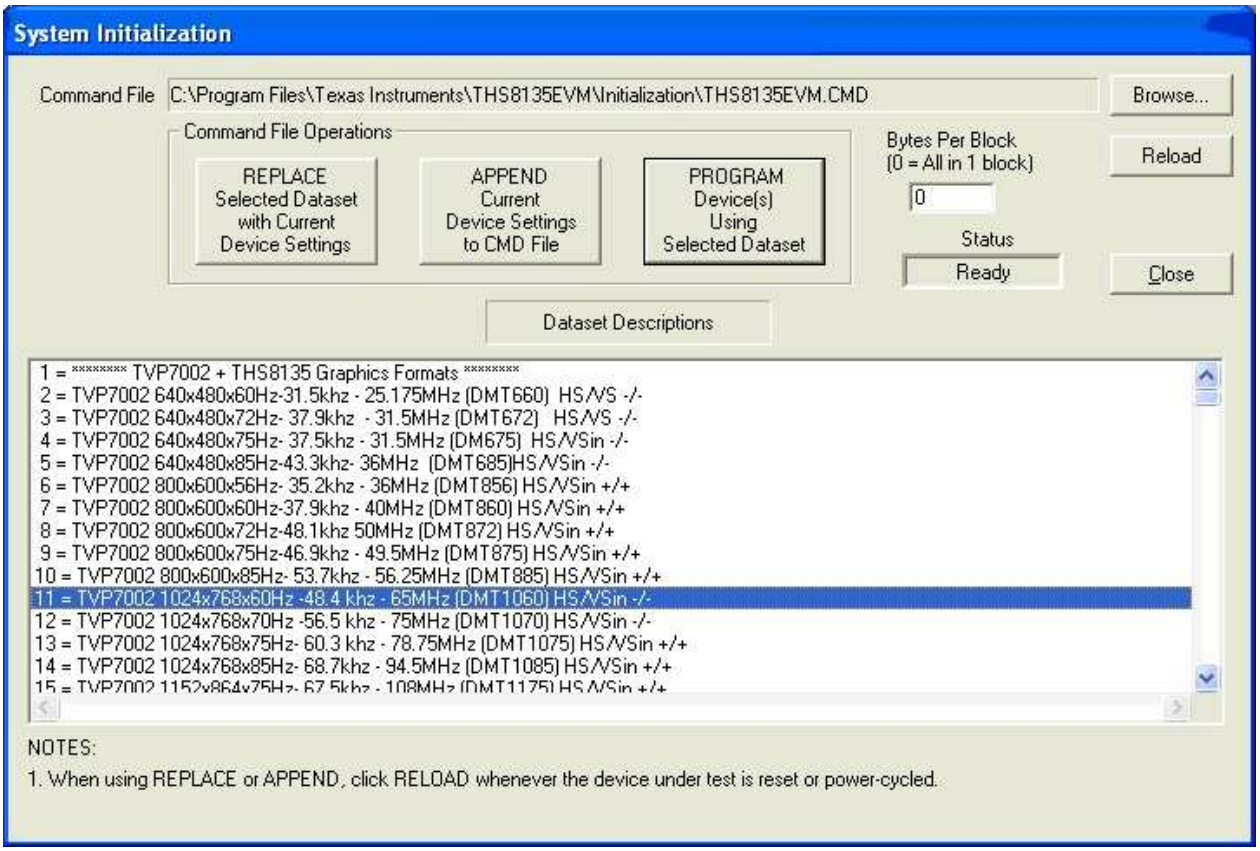

Figure 15. System Initialization

6.6 Command Files

The command file is a text file that can be generated using any common editor; however, it must be saved as plain text. Command files are especially useful for quickly switching between the various system configurations. These .CMD files are unrelated to the typical Windows .CMD files.

A default command file containing some of the more popular graphics formats is included on the CD-ROM. This command file is located at:

C:\Program Files\Texas Instruments\THS8135EVM\Initialization\THS8135EVM.cmd

A command file can contain up to 250 data sets. A data set is a set of register settings to initialize the TVP7002 Triple ADC for a particular graphics mode. Each data set includes a description that is displayed in one row of the dataset descriptions list. The register settings may be located in the command file itself and/or may be stored in separate include file(s) (with an .INC file extension) and be included into the command file using the INCLUDE statement.

6.6.1 Example Command File

The following is an example of one data set within a command file.

```
BEGIN_DATASET                                  // Dataset 1

DATASET_NAME,"TVP7002 1024x768x60Hz -48.4 khz - 65MHz (DMT1060) HS/VSin -/-"

WR_REG,TVP7000,0x01,0x01,0x54 // PLL DIVMSB 1344 pix/line
WR_REG,TVP7000,0x01,0x02,0x00 // PLL DIVLSB
WR_REG,TVP7000,0x01,0x03,0x58 // PLL CONTROL
WR_REG,TVP7000,0x01,0x04,0x80 // PHASE SEL(5) CKDI CKDI DIV2
WR_REG,TVP7000,0x01,0x05,0x06 // CLAMP START
WR_REG,TVP7000,0x01,0x06,0x10 // CLAMP WIDTH
WR_REG,TVP7000,0x01,0x07,0x60 // HSYNC OUTPUT WIDTH - 96
WR_REG,TVP7000,0x01,0x08,0x3C // Blue Fine Gain
WR_REG,TVP7000,0x01,0x09,0x3C // Green Fine Gain
WR_REG,TVP7000,0x01,0x0A,0x3C // Red Fine Gain
WR_REG,TVP7000,0x01,0x0E,0x24 // SYNC CONTROL    HSout+ VSout+
WR_REG,TVP7000,0x01,0x0F,0x2E // PLL and CLAMP CONTROL bit0 (0=  HSPO by chip)
WR_REG,TVP7000,0x01,0x10,0x58 // SOG Threshold-(RGB Clamp)
WR_REG,TVP7000,0x01,0x11,0x40 // Sync Separator Threshold
WR_REG,TVP7000,0x01,0x12,0x01 // PRE_COAST
WR_REG,TVP7000,0x01,0x13,0x00 // POST_COAST
WR_REG,TVP7000,0x01,0x15,0x04 // Output Formatter
WR_REG,TVP7000,0x01,0x17,0x00 // MISC Control 2  FID out, Enable Outputs
WR_REG,TVP7000,0x01,0x18,0x01 // Clock polarity
WR_REG,TVP7000,0x01,0x19,0xAA // INPUT MUX SELECT, RGB CH3 selected
WR_REG,TVP7000,0x01,0x1A,0xCA // INPUT MUX SELECT, HSYNC_A and VSYNC_A selected
WR_REG,TVP7000,0x01,0x21,0x15 // HSOUT START
WR_REG,TVP7000,0x01,0x22,0x00 //
WR_REG,TVP7000,0x01,0x26,0x80 // ALC RED and GREEN LSB
WR_REG,TVP7000,0x01,0x28,0x53 // AL FILTER Control
WR_REG,TVP7000,0x01,0x2A,0x87 // Enable FINE CLAMP CONTROL
WR_REG,TVP7000,0x01,0x2B,0x00 // POWER CONTROL-SOG ON
WR_REG,TVP7000,0x01,0x2C,0x50 // ADC Setup
WR_REG,TVP7000,0x01,0x31,0x18 // ALC PLACEMENT
WR_REG,TVP7000,0x01,0x35,0x00 // VSout Align
WR_REG,TVP7000,0x01,0x36,0x02 // VSync Bypass
WR_REG,TVP7000,0x01,0x3D,0x06 // Line Length Tolerance (Pixel Tolerance)
WR_REG,TVP7000,0x01,0x40,0x32 // AVID Start  306 (296+10)
WR_REG,TVP7000,0x01,0x41,0x01 // AVID Start
WR_REG,TVP7000,0x01,0x42,0x32 // AVID  Stop 1330 ((306 +1024 )
WR_REG,TVP7000,0x01,0x43,0x05 // AVID Stop
WR_REG,TVP7000,0x01,0x44,0x03 // VBLK F0 Offset (3)
WR_REG,TVP7000,0x01,0x45,0x03 // VBLK F1 Offset
WR_REG,TVP7000,0x01,0x46,0x26 // VBLK F0 Duration  38 lines
WR_REG,TVP7000,0x01,0x47,0x26 // VBLK F1 Duration

END_DATASET
```

6.6.2 Command File Syntax

- The comment indicator is the double-slash //.
- The command file is not case-sensitive and ignores all white-space characters.
- All numbers can be entered as hexadecimal (beginning with 0x) or as decimal.
- Every data set in a command file begins with BEGIN_DATASET and ends with END_DATASET. The maximum number of datasets is 250.
- The dataset text description is entered between double quotes using the DATASET_NAME command. The enclosed text can be up to 128 characters in length. This text appears in the System Initialization dialog box when the command file is opened.

- The INCLUDE command inserts the contents of an include file (with an .INC file extension) in-line in place of the INCLUDE command. Therefore, the include file must not contain the BEGIN_DATASET, END_DATASET, and DATASET_NAME commands.

NOTE: All included files must be located in the same directory as the command (CMD) file.

- The write-to-register command is written as:

```
WR_REG, <DeviceFamily>, <Number of data bytes (N)>, <subaddress>, <Data1>,..., <DataN>
```

or

```
WR_REG, <Literal slave address>, <Number of data bytes (N)>, <subaddress>,
<Data1>,..., <DataN>
```

- The valid device family mnemonics for the THS8135EVM is TVP7000 for the TVP7002

  VCC translates the device family mnemonic to the slave address that was selected in the VCC Configuration window at program startup. This eliminates having to edit command files if the alternate slave address must be used.

  If the literal slave address method is used, then the slave address entered is used directly.

- A delay may be inserted between commands using the WAIT command, which is written as follows:

```
WAIT,<# milliseconds>
```

6.6.3 Adding a Custom Data Set to a CMD File

To create a custom dataset, program the EVM via the system initialization tool using the factory-supplied command file. Through the property sheets tool or I^2C Register Map Editor, you can then customize the device register settings to suit your needs and save the settings as a new dataset. To save your custom settings:

1. Open the System Initialization dialog box via the Tools menu.
2. Click the Append Current Device Settings to Command File button. A dialog box requesting a description of the new data set appears.
3. Optionally, click the drop-down box and select one of the existing descriptions.
4. Modify the description text or type your own description.
5. Click OK. All non-default register values from the TVP7002 are appended to the current command file as an additional data set.

Now, you can select your custom data set and send it with a press of the Program... button.

6.7 Register Editing

The following sections describe the three available modes of register editing: Register Map Editor, Generic I^2C Register Editor, and TVP7002 Property Sheets. Each of these functions can be selected from the Edit menu.

6.7.1 Register Map Editor

The register map editor (see Figure 16) allows the display and editing of the entire register space of the device within a simple scrolling text box. To open this window, click Edit Register Map in the Edit menu and click on the device type to edit. If the intended device type is not shown, then use the Windows menu to activate the existing window.

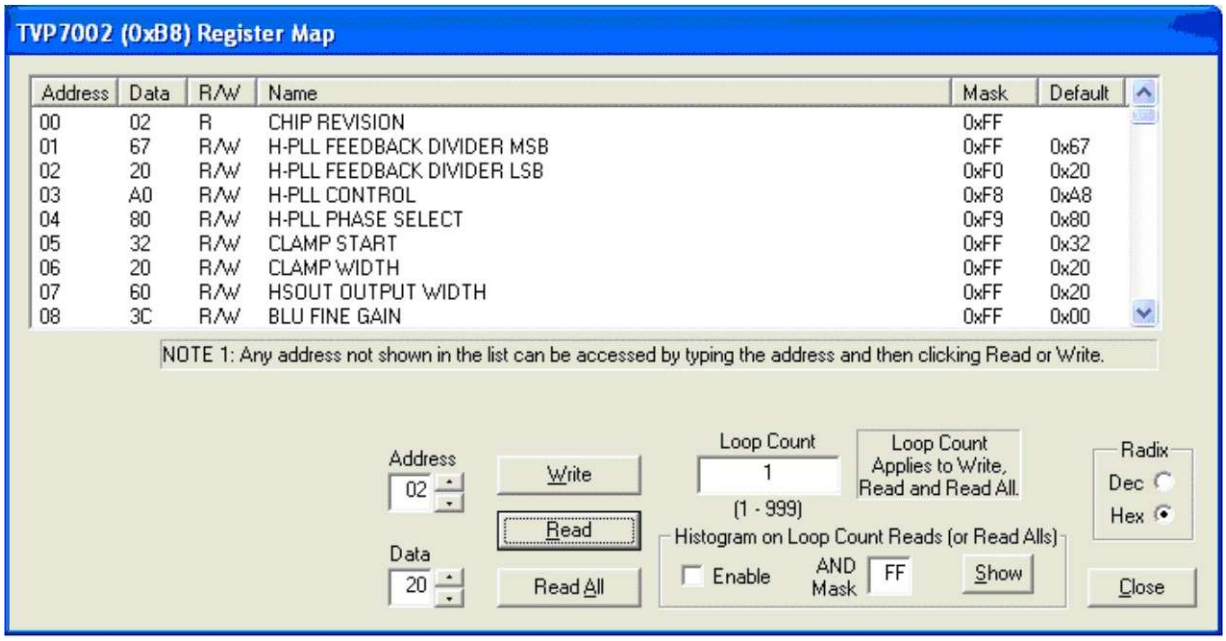

Figure 16. Register Map Editor

Table 4. Register Map Editor Controls

Control	Definition
Register Window	Scrolling text box that displays the address and data for the I^2C registers that are defined for the device.
Address Edit Box	This contains the I^2C subaddress that will be accessed using the Write and Read buttons. Clicking on a row selects an address, which then appears in the address edit box. NOTE: After clicking on a row, the Data Edit Box contains the data that was in the register window. This data may not correspond to the actual data in the device (until Read or Read All is clicked). The address up/down arrows are used to jump to the next/previous sub–address that is defined for the device. NOTE: If an address is not defined for the device, it can still be accessed by typing the sub–address in the Address Edit Box.
Data Edit Box	This contains the data which will be written to or read from the I^2C subaddress. The data up/down arrows increases / decreases the data value by 1.
Write Button	Writes the byte in the Data Edit box to the address in the Address Edit box. The I^2C register is written to whether or not the data is different from the last time the register was read.
Read Button	Reads the data from the address in the Address Edit box into the Data Edit box and the register window.
Read All Button	Reads all defined readable registers from the device and updates the register window.
Hex Button	Converts all values in the register window and address and data edit boxes to hexadecimal.
Dec Button	Converts all values in the register window and address and data edit boxes to decimal.
Close Button	Closes the dialog. NOTE: Multiple edit register map windows can be open at the same time (one for each device). Use the Window menu to navigate.
Loop Count	Causes subsequent write or read operations to be performed N times. N is entered as a decimal number from 1 to 999.

6.7.2 Generic I²C Register Editor

The Generic I²C Register Editor (see Figure 17) allows the display and editing of any device on the I²C bus. This editor works like the Register Map Editor, except that the I²C slave address must be entered and the Read All button is disabled.

To open this window, click on Edit Register Map in the Edit menu and then click on Generic I²C.

The Generic I²C Register Editor may be useful when connecting other devices to the I²C bus on the THS8135EVM but is not required for typical operation of the THS8135EVM.

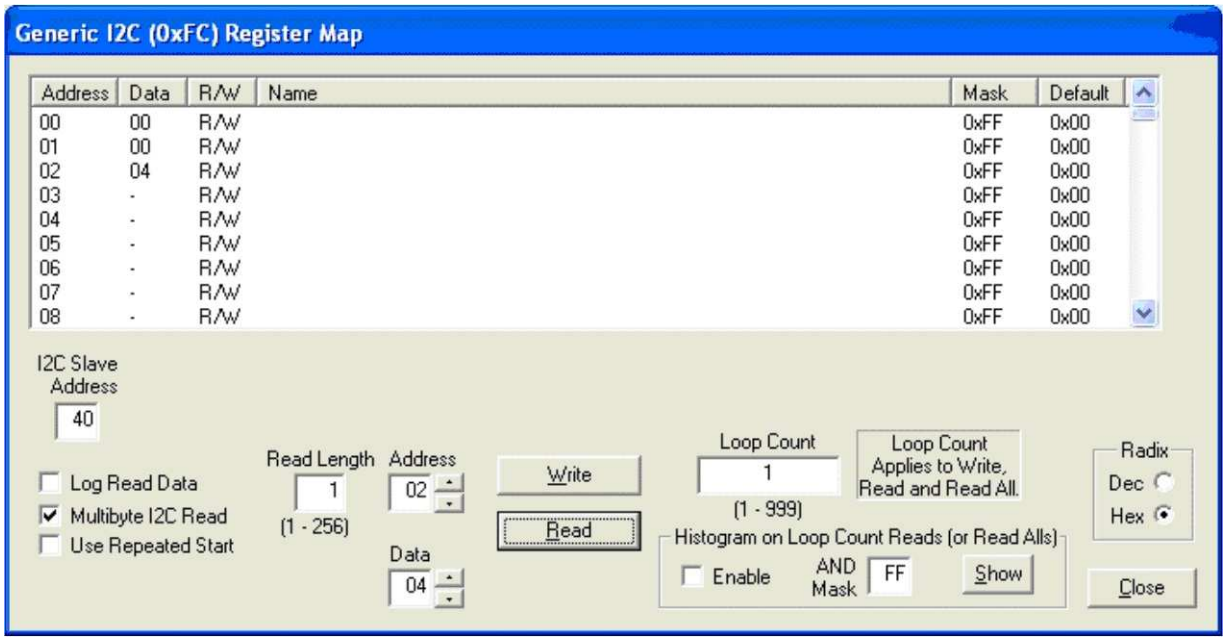

Figure 17. Generic I²C Register Map Editor

6.8 TVP7002 Property Sheets

The property sheets represent the TVP7002 register data in a user-friendly format. The data is organized by function, with each function having its own page and being selectable via tabs at the top.

To open this, click Edit Property Sheets in the Edit menu and select the device type to edit.

When the property sheet function is started or whenever you tab to a different page, all readable registers in the device are read from hardware to initialize the dialog pages. Values on the page are changed by manipulating the various dialog controls as described in Table 5.

There are OK, Cancel, and Apply buttons at the bottom of each property page (see Table 6).

Table 5. Use of Property Sheet Controls

Dialog Control	What Do I Do With It?	When is Hardware Updated?
Read-Only Edit Box	Read status information	N/A
Check Box	Toggle a single bit	After Apply
Drop-Down List	Select from a text list	After Apply
Edit Box	Type a number	After Apply
Edit Box with Up/Down arrows	Use up/down arrows or type a number	Up/Down Arrows: Immediately Type a number: After Apply
Slider	Slide a lever	Immediately
Pushbutton	Initiate an action	Immediately

Table 6. Property Sheet Button Controls

Button Control	Definition
OK	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address. Closes the dialog.
Cancel	Causes all changes made to the property page since the last Apply to be discarded. Changes made to dialog controls with "immediate hardware update" are not discarded, since they have already been changed in hardware. Does not write to hardware. Closes the dialog.
Apply	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address.

6.8.1 Input Mux Property Sheet

The Input Mux property sheet (see Figure 18) provides controls for configuring the input connections and sync options. Auto detect is recommended for the THS8135EVM HSYNC/VSYNC selection and HSYNC input polarity. The TVP7002 automatically determines the presence of the discrete HSYNC/VSYNC inputs. The VGA connector MUX selection must be selected for proper THS8135EVM operation. The SOG and sync separator controls are not applicable to RGB with separate syncs.

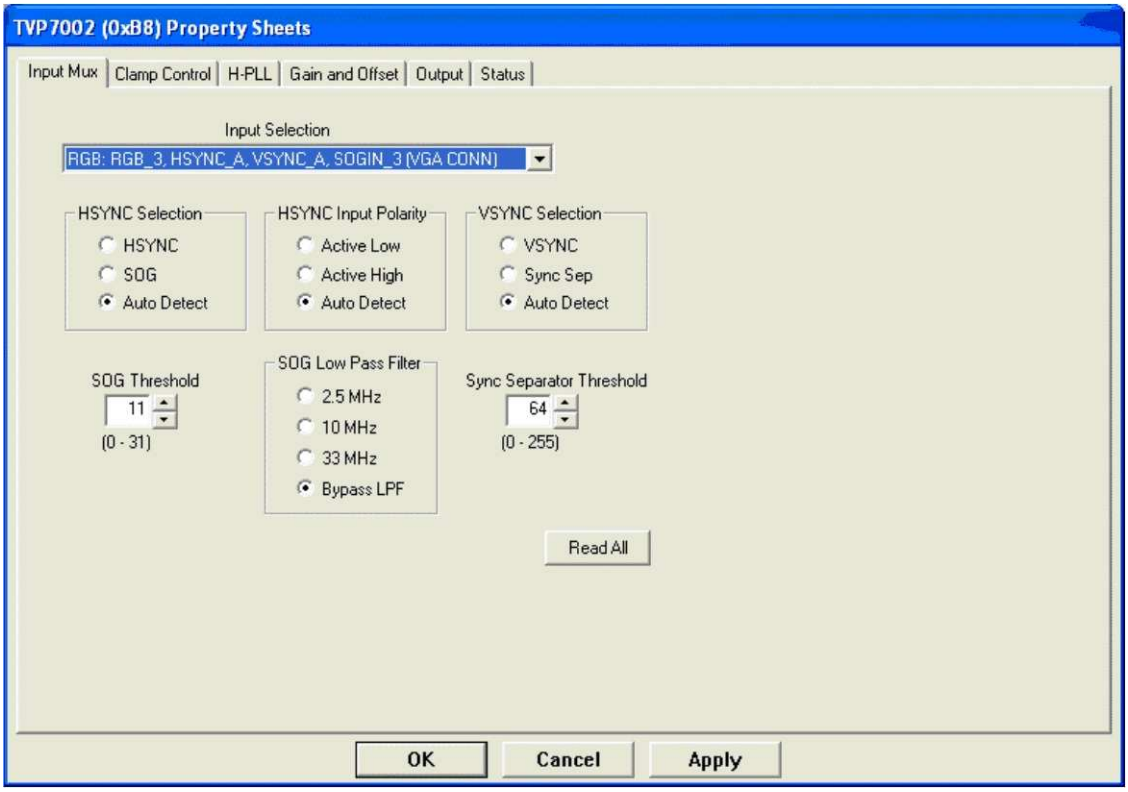

Figure 18. Input Mux Property Sheet

6.8.2 Clamp Control Property Sheet

The analog RGB inputs on the THS8135EVM are AC-coupled and require the TVP7002 internal clamp circuit to restore the proper DC levels. The position of the internal fine clamp pulse is relative to HSYNC trailing or leading edge depending on the Clamp REF bit setting in I²C register 15h. In most cases, the trailing edge of HSYNC will be used to ensure clamping during black level when sync on green is present.

The fine clamp must be enabled in I²C Register 2Ah and correctly positioned during the horizontal blanking interval. The recommended settings for PC graphics in Table 7 may be used for all RGB graphics formats. Bottom level clamping must be used for RGB graphics. The initialization file included with the THS8135EVM automatically sets the clamp settings appropriately for RGB graphics inputs when the TVP7002 is programmed with one of the datasets.

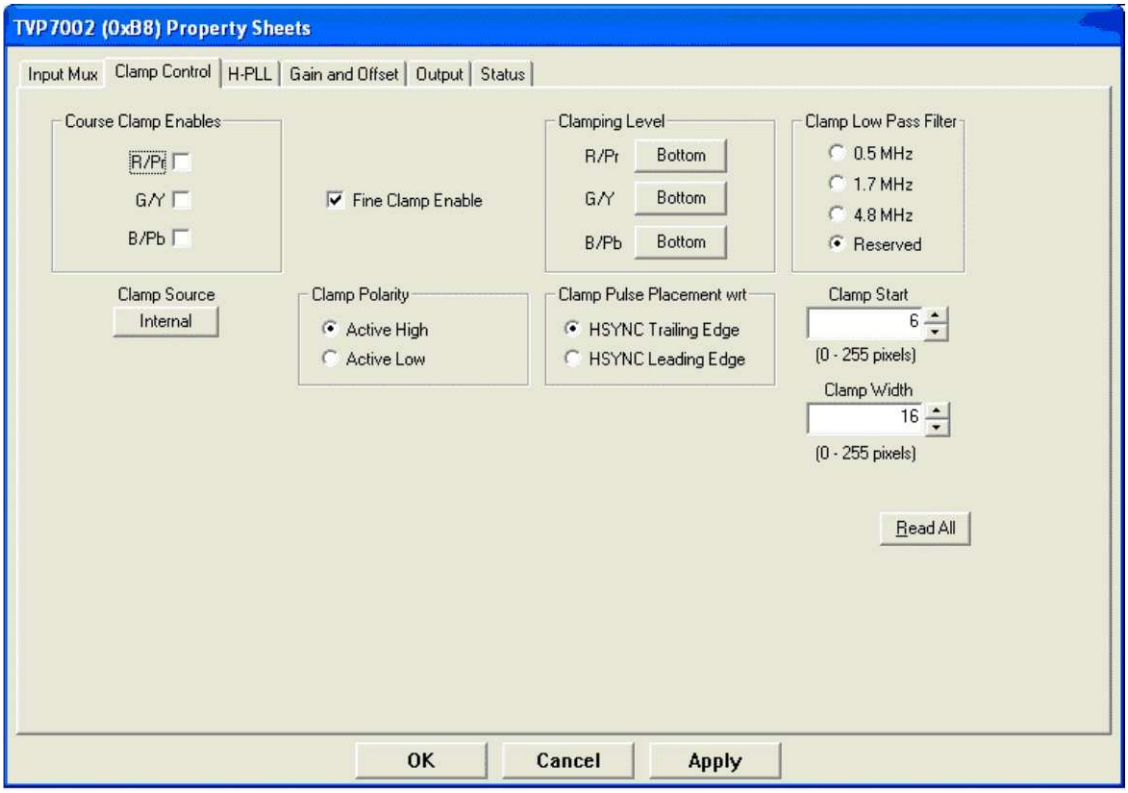

Figure 19. Clamp Control Property Sheet

Table 7. Typical Clamp Setup for RGB Graphics

I²C Address	Setting	Description
05h	06h	Clamp start
06h	10h	Clamp width
0Fh	0Eh	Internal Clamp enabled
10h	80h	Bottom level clamping for RGB
15h	00h	Clamp pulse relative to HSYNC trailing edge
2Ah	07h	Enable fine clamps
2Dh	00h	Coarse Clamp disabled

6.8.3 H-PLL Property Sheet

A PLL setup calculator is integrated into the H-PLL property sheet (see Figure 20). The H-PLL Feedback Divider, VCO range, and Charge Pump settings can be automatically calculated by entering the HSYNC and Pixel frequencies and pressing the Calculate button. The new settings are not written to the TVP7002 until the Program button is pressed.

The feedback divider is typically set to the total number of pixels per line and used with a Post Divider of 1. The initialization file included with the THS8135EVM will automatically set up the PLL appropriately for the RGB graphics formats included.

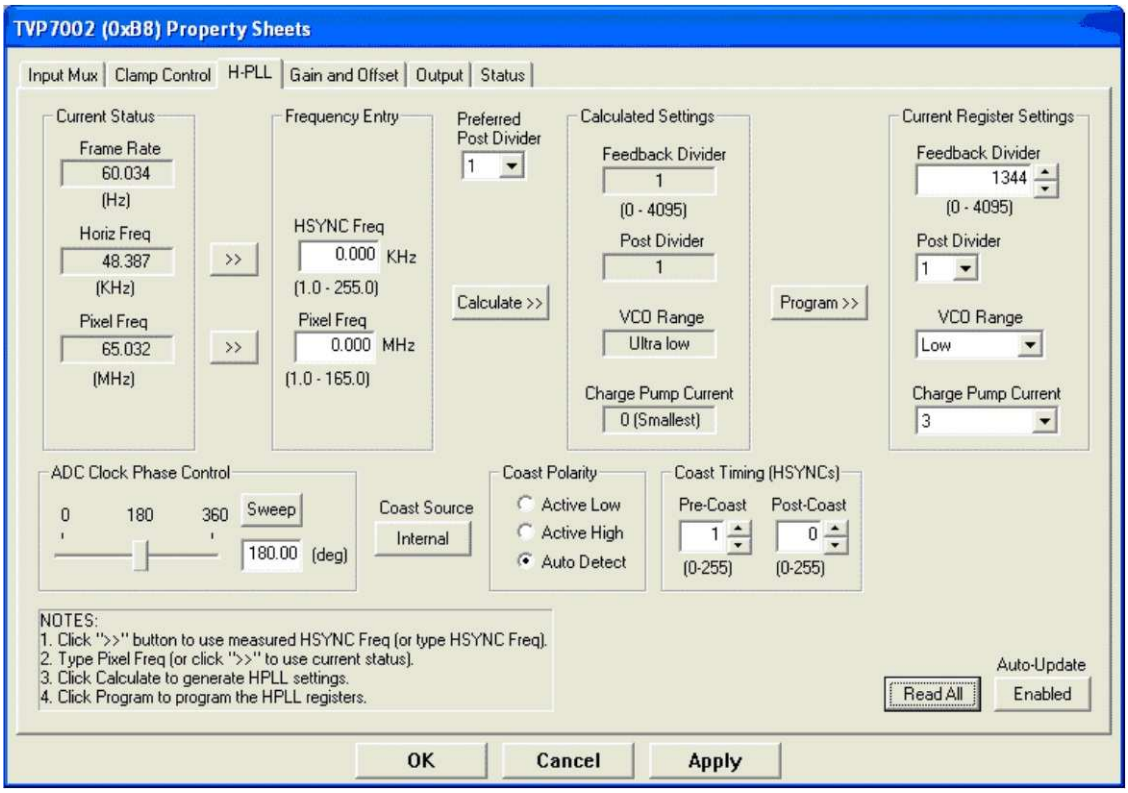

Figure 20. PLL Property Sheet

The Frame Rate, Horiz Freq, and Pixel Freq information reported in the Current Status frame are calculated values based on the current H-PLL Feedback Divider and the Lines/Frame and Clocks/Line Status read form the TVP7002. The precision of these calculated values will depend on whether the internal reference clock or the 27-MHz external reference clock is selected (see Status Property Sheet). Current settings and status can be read at any time by pressing the Read All button. All read-only status is continuously updated provided that the TVP7002 Property Sheet is the active window and the Auto-Update button has not been set to Disabled.

An internally-generated coast signal can be used to put the PLL in coast or free-run mode to avoid disruptions in HSYNC during vertical blanking. When the internal coast is in use, the pre-coast and post-coast settings specify the coast interval range relative to the internally-detected VSYNC. Pre-coast specifies the number of lines before detecting VSYNC, and post-coast specifies the number of lines after VSYNC that are used for the coast interval. Coast operation is not applicable to RGB graphics with separate syncs.

The ADC Clock Phase control is used to adjusting sampling phase of the ADC clock relative to HSYNC and the RGB graphics input. This must be adjusted to align the sample clock with the RGB pixel input.

6.8.4 Gain and Offset Property Sheet

The Gain and Offset property sheet (see Figure 21) provides controls for both analog and digital gain/offset adjustment. The coarse gain and offset are analog in nature and are applied prior to the ADCs. Fine gain, fine offset, and automatic level correction (ALC) are applied in the digital domain after the ADCs. Coarse gain provides an analog gain range of 0.5 to 2.0, while Fine gain provides a digital gain range of 1 to 2.

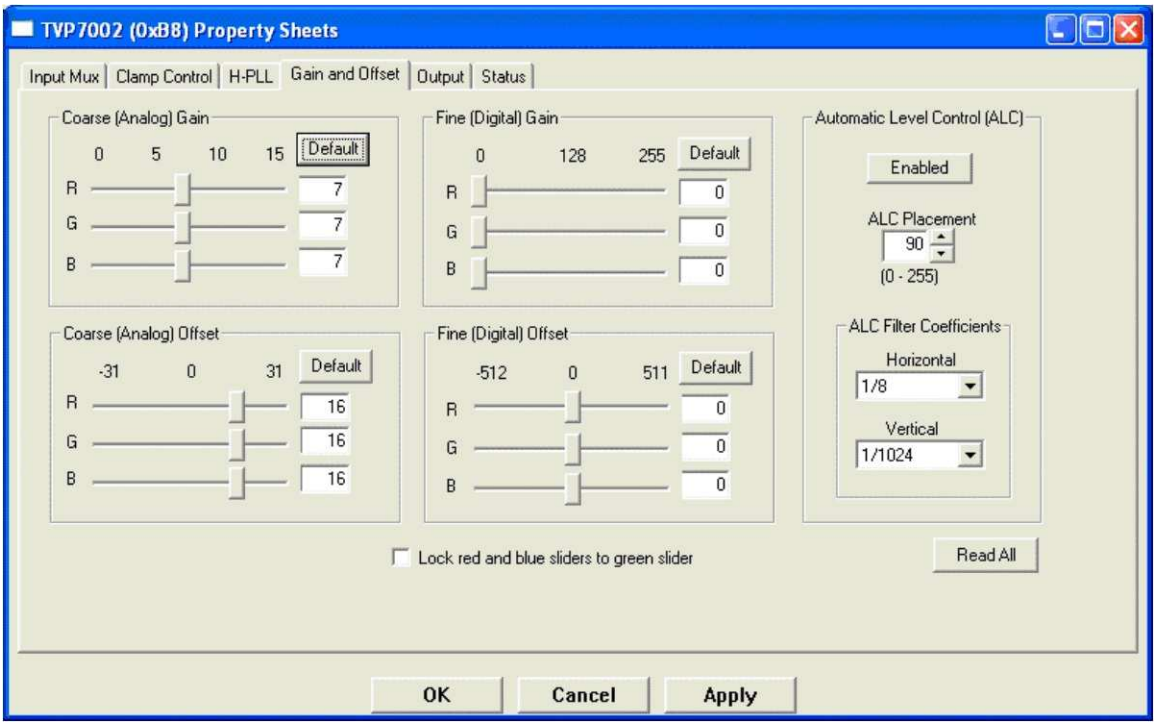

Figure 21. Gain and Offset Property Sheet

Stable output offset levels are maintained by use of the ALC feedback level control in the TVP7002. Two sets of filter coefficients are available that define the level of filtering applied on each line (horizontal) and the amount of feedback correction that is applied per line update (vertical). The horizontal coefficient (I^2C register 28h, NSH[2:0]) specifies the number of pixels that are used in the horizontal filter. The ALC filter must be applied during the horizontal blank interval following the clamp pulse, so it must be correctly positioned using the ALC placement register (register 31h). The amount of horizontal filtering that can be used will depend on the ALC placement and the horizontal blanking interval of the input video format.

The vertical coefficient (I^2C register 28h, NSV[3:0]) specifies the amount of feedback error correction derived from the horizontal filter that is applied to each line update. The NSV coefficient can range from 1 (maximum error applied) to 1/1024 (minimum error applied). The TVP7002 default filter coefficients should be adequate for most applications.

In the ALC operating mode, the fine offset registers are used to position the final digital output levels. To prevent bottom level clipping at the ADCs, a coarse offset setting of 16 (10h) is recommended. Any clipping that occurs at the ADC input cannot be recovered by the ALC. The initialization file included with the THS8135EVM will automatically set up the ALC appropriately for the RGB graphics support.

6.8.5 Output Property Sheet

The Output property sheet (see Figure 22) provides various controls for enabling outputs, selecting the output format, setting HSOUT polarity/position/width, and specifying embedded sync or Data Enable (DE) output timing. At power-up, the RGB data, DATACLK, and syncs will be in a high impedance state until enabled in I^2C register 17h or until programming the TVP7002 with one of the datasets included in the initialization file. The DATACLK output polarity is selectable in I^2C register 18h.

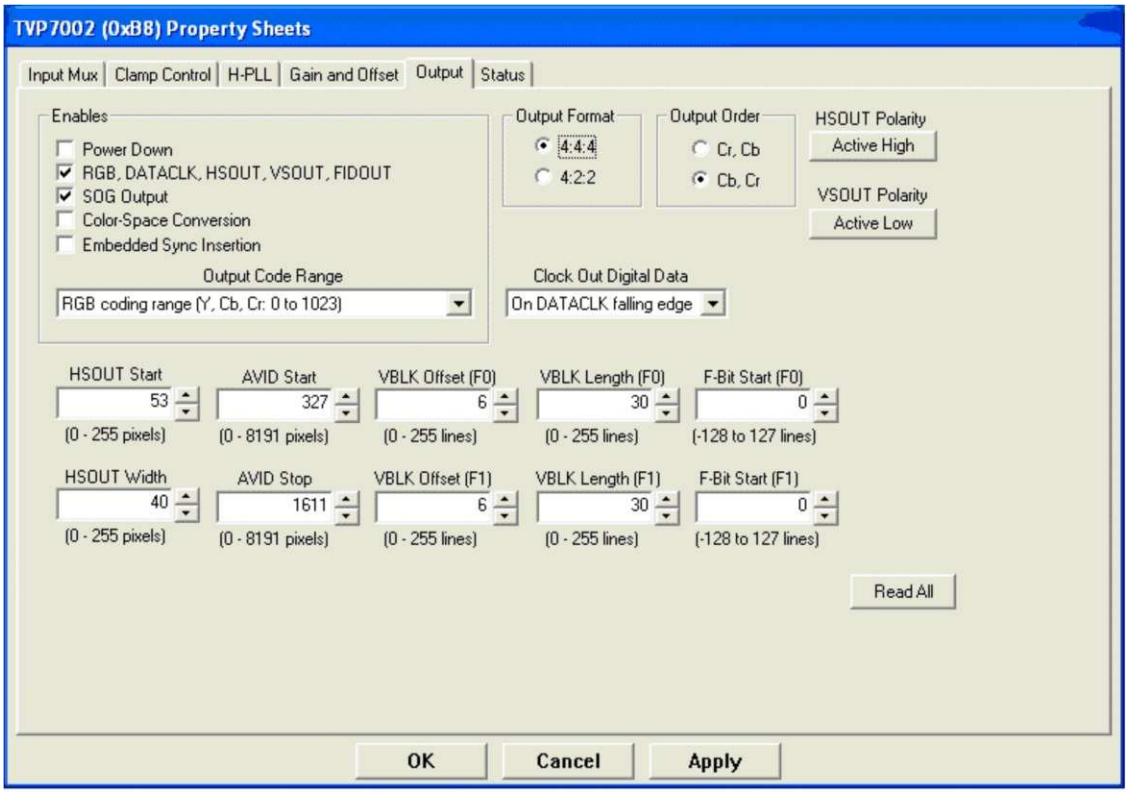

Figure 22. Output Property Sheet

Graphics monitors use sync polarities and widths for format detection, so it is imperative that the output syncs are programmed correctly for the graphics format being used. Horizontal alignment may be adjusted with HSOUT Start control.

The TVP7002 provides support for a 30-bit 4:4:4 or a 20-bit 4:2:2 output format. The THS8135EVM provides support for the 30-bit 4:4:4 output format only. Embedded syncs are not supported by the THS8135EVM.

The TVP7002 color space converter included in the TVP7002 is not required for displaying RGB graphics formats with the THS8135EVM.

NOTE: Data Enable (DE) output support is provided through use of the TVP7002 multi-function FIDOUT pin (#22). See the TVP7002 I^2C register 17h for more information. This DE signal can be connected to the THS8135 Blank input if desired. The DE position and duration can be adjusted by the AVID Start and Stop settings and the VBLK Offset and Length settings.

6.8.6 Status Property Sheet

The Status Property Sheet (see Figure 23) reports input sync status from the TVP7002 I^2C register 14h and additional input format information from I^2C registers 37h to 39h. Lines per Frame and REFCLKs per Line are read directly from the I^2C registers, while the Calculated Status is calculated from these measured values and the current H-PLL feedback divider.

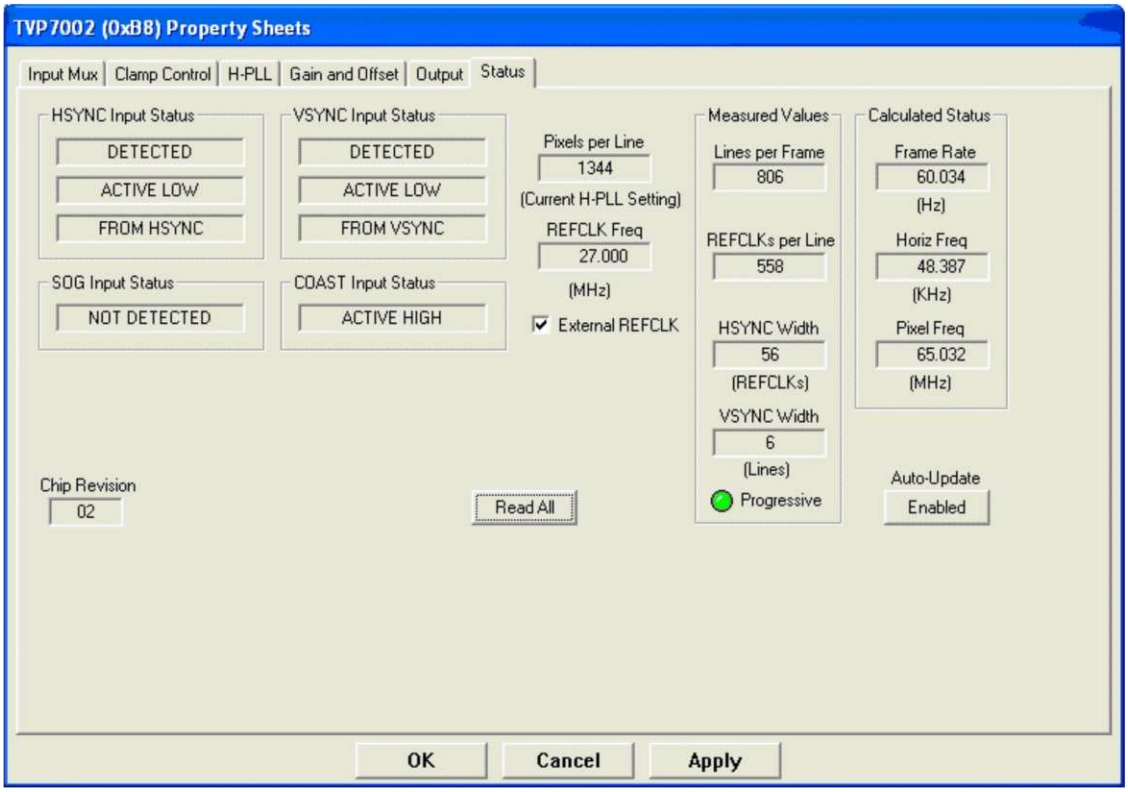

Figure 23. Status Property Sheet

The THS8135EVM is shipped with an on-board 27-MHz REFCLK that is used by the TVP7002 for REFCLKS per Line and HSYNC Width detection. HSYNC width and REFCLKs per Line are reported in 27-MHz REFCLK cycles. External REFCLK must remain checked to provide status read-back based on the external 27-MHz REFCLK.

6.9 Property Sheet Refresh

The property sheets are designed so that the data displayed is always current. The following actions cause the entire register map to be read from the device and update the property sheets:

- Property sheets are initially opened
- When tabbing from one page to another
- When Read All is clicked
- When making the Property Sheets window the active window (by clicking on it)
- When making a Register Map Editor window the active window (by clicking on it)

6.10 Auto-Update When Activating Windows

When you open both the property sheets and the register map editor at the same time, changes made to the property sheets (and applied) are updated in the register map window as soon as the register map window is clicked on. It also works the other way; changes made in the register map editor are updated in the property sheets as soon as the property sheets window is clicked on.

6.11 Property Page Auto Update

When the TVP7002 H-PLL property sheet or Status property sheet are showing and the property sheets window is the active window and the Auto Update button on that page is enabled (default), the TVP7002 register map is read continuously and the status controls on that page are continuously updated.

7 Troubleshooting the THS8135EVM

This chapter discusses ways to troubleshoot the THS8135EVM.

7.1 Troubleshooting Guide

If you are experiencing problems with the THS8135EVM hardware or the VCC software, see Table 8 for available solutions.

Table 8. THS8135EVM Troubleshooting

Symptom	Cause	Solution
Blank screen	Bad cable	Check cables with direct connection to the monitor.
	THS8135EVM not correctly programmed	Ensure that the input format precisely matches the VCC dataset used.
	Sync/ or Blank control signals are at logic low level	Check levels at J2 header.
Line noise present with high-frequency vertical line input pattern	TVP7002 H-PLL phase setting is not set correctly for the input source	Adjust TVP7002 H-PLL phase setting.
Display shifted horizontally	TVP7002 HSOUT polarity set wrong	Change HSOUT polarity setting.
	TVP7002 HSOUT Start setting	Adjust HSOUT start setting.
Picture too dark	Clamp or ALC not set correctly	Reposition Clamp or ALC. Reduce ALC horizontal filter coefficient.
	Monitor clamping during active RGB	Adjust HSOUT position or polarity.
	TVP7002 gain setting too low	Adjust gain.
	THS8135EVM not correctly programmed	Ensure that the input format precisely matches the VCC dataset used.
Colors incorrect	Gain not set the same for all channels	Check TVP7002 gain settings.
	Incorrect clamp setting	Use TVP7002 bottom level clamping for all channels.
Monitor does not detect the right format	The THS8135EVM is not programmed to match the graphics input format	Ensure that the input format precisely matches the VCC dataset used.
Missing color	Bad cable.	Check cables with direct connection the monitor.
	Damaged RGB input or output PCB trace	Check continuity of traces to the VGA connectors.
Edges of text appear noisy	TVP7002 H-PLL phase setting is not set correctly for the input source	Adjust TVP7002 H-PLL phase setting.
Vertical banding artifacts	TVP7002 H-PLL pixel clock is not set properly for the input format	Ensure that the input format precisely matches the VCC dataset used.
	TVP7002 PLL phase setting is not set correctly for the input source	Adjust TVP7002 H-PLL PLL phase setting.
	Monitor scaling artifacts	
DAC outputs too high and distorted when viewed with an oscilloscope.	DAC outputs improperly terminated	Terminate with 75 Ω at the oscilloscope input.

7.2 Resolving I^2C Communication Problems

If the dialog box shown in Figure 24 appears, check the USB connection and USB Link LED on the THS8135EVM. The USB Link LED is lit if a valid USB link is established. If the USB cable is connected, but the USB Link LED is not lit, disconnect the USB cable, wait three seconds, and then reconnect. Press the Continue button after the USB link is established.

Figure 24. USB Device Not Found

If the dialog box shown in Figure 25 appears, exit the THS8135EVM Software, power-cycle the THS8135EVM and restart the THS8135EVM Software. This condition can occur if the EVM is powered off while I^2C activity is running continuously via USB.

Figure 25. USB Invalid Response Code

If an I^2C acknowledge error occurs, a dialog box like Figure 26 appears. This dialog box reports that an I^2C read from the TVP7002 failed, using slave address 0xBA, sub-address 0x00.

If this dialog box appears, click on Exit Program. Restart VCC and ensure that the TVP7002 I^2C sub-address is set to the correct address. The hardware default I^2C slave address for the TVP7002 is 0xB8.

Figure 26. USB I^2C Error Addressing Slave Address 0xBA

If a dialog box indicating that failure occured using I^2C slave address 0xB8 appears (see Figure 27), click on Exit Program. Restart VCC and ensure that the 5-V power supply is connected. Both the 5-V LED and the USB Link LED must be lit for proper operation.

Figure 27. USB I²C Error Addressing Slave Address 0xB8

8 Schematics

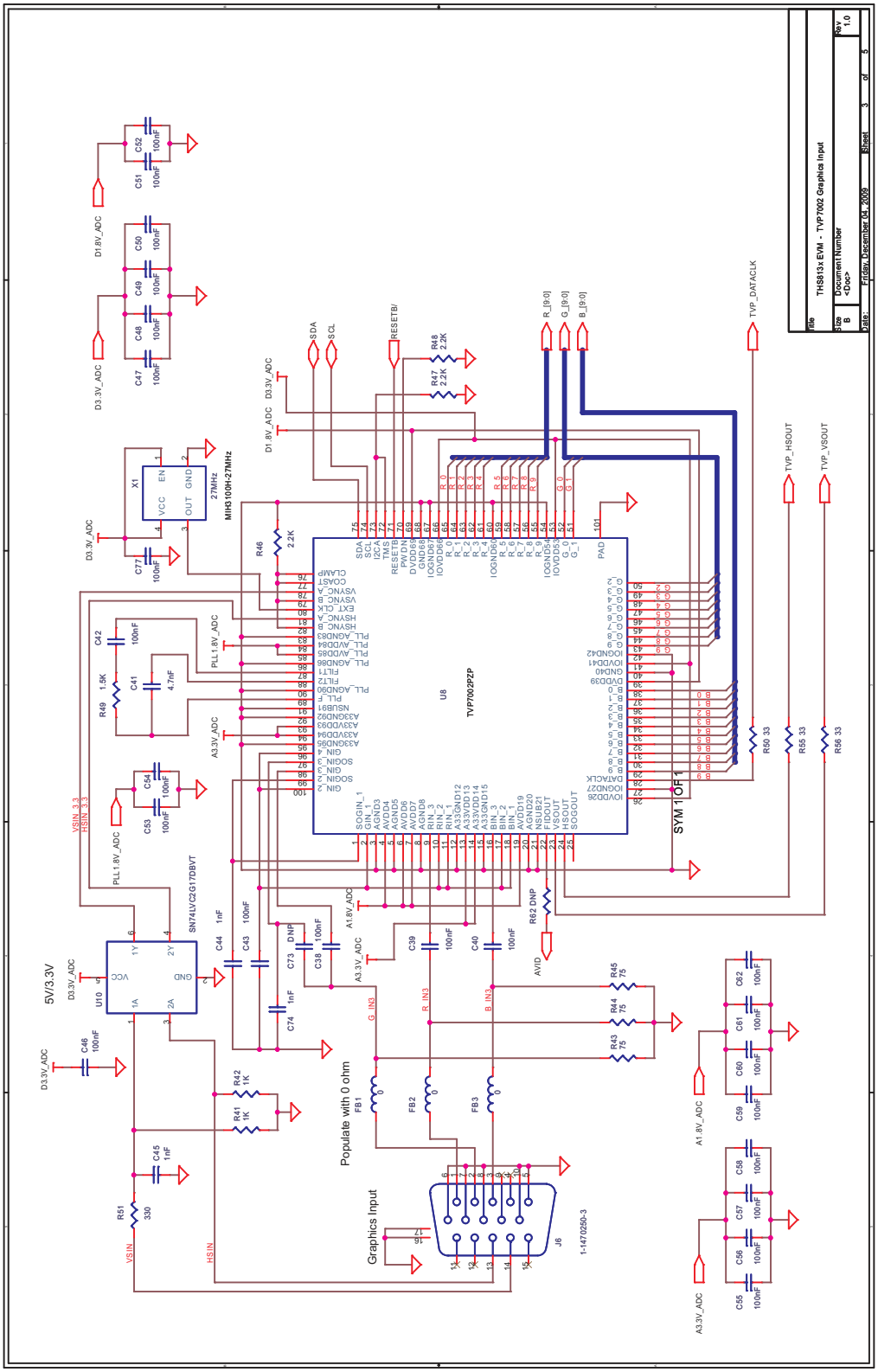

Figure 28. Schematic – TVP7002 Graphics Input

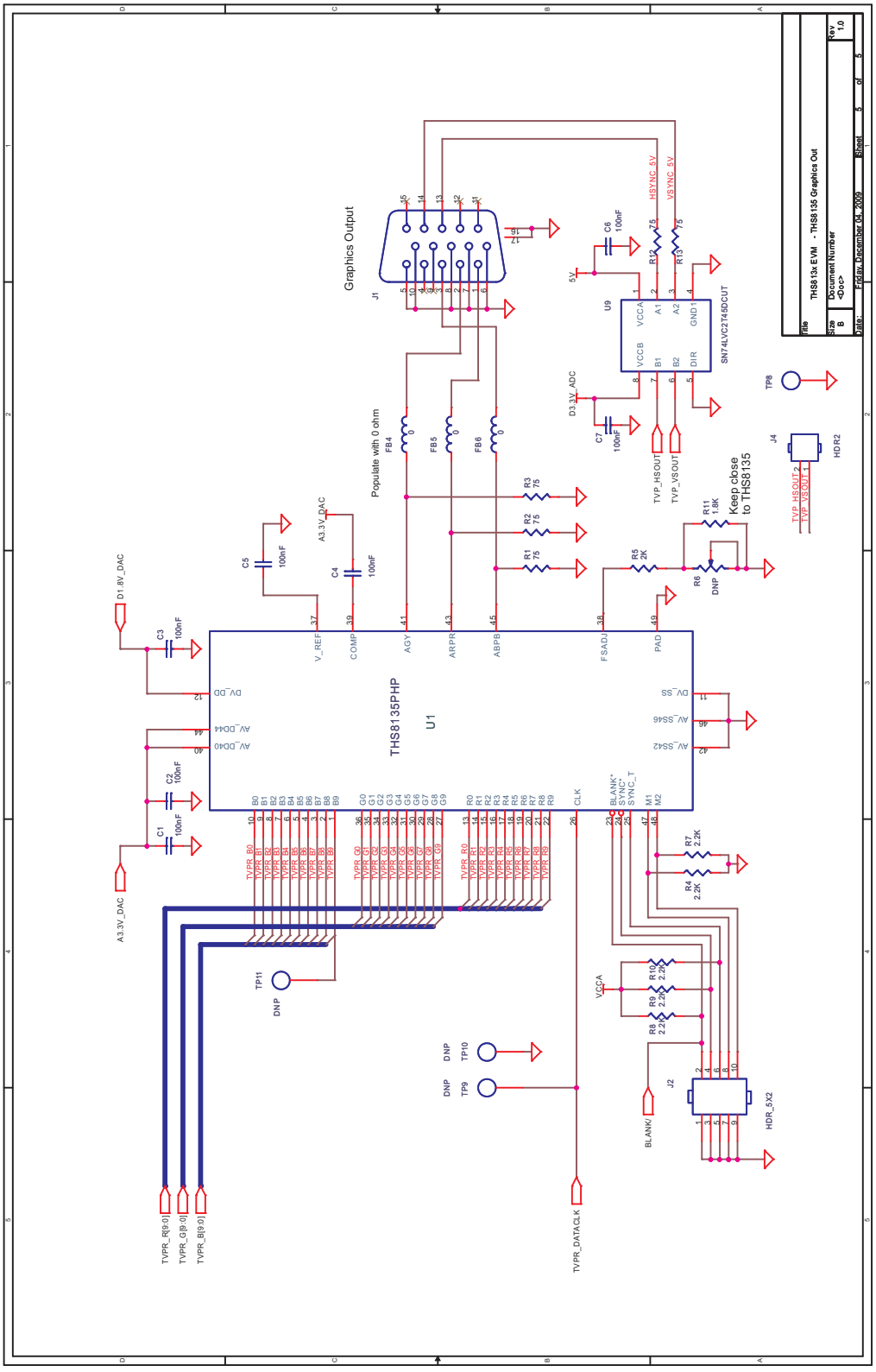

Figure 29. Schematic – THS8135 Graphics Output

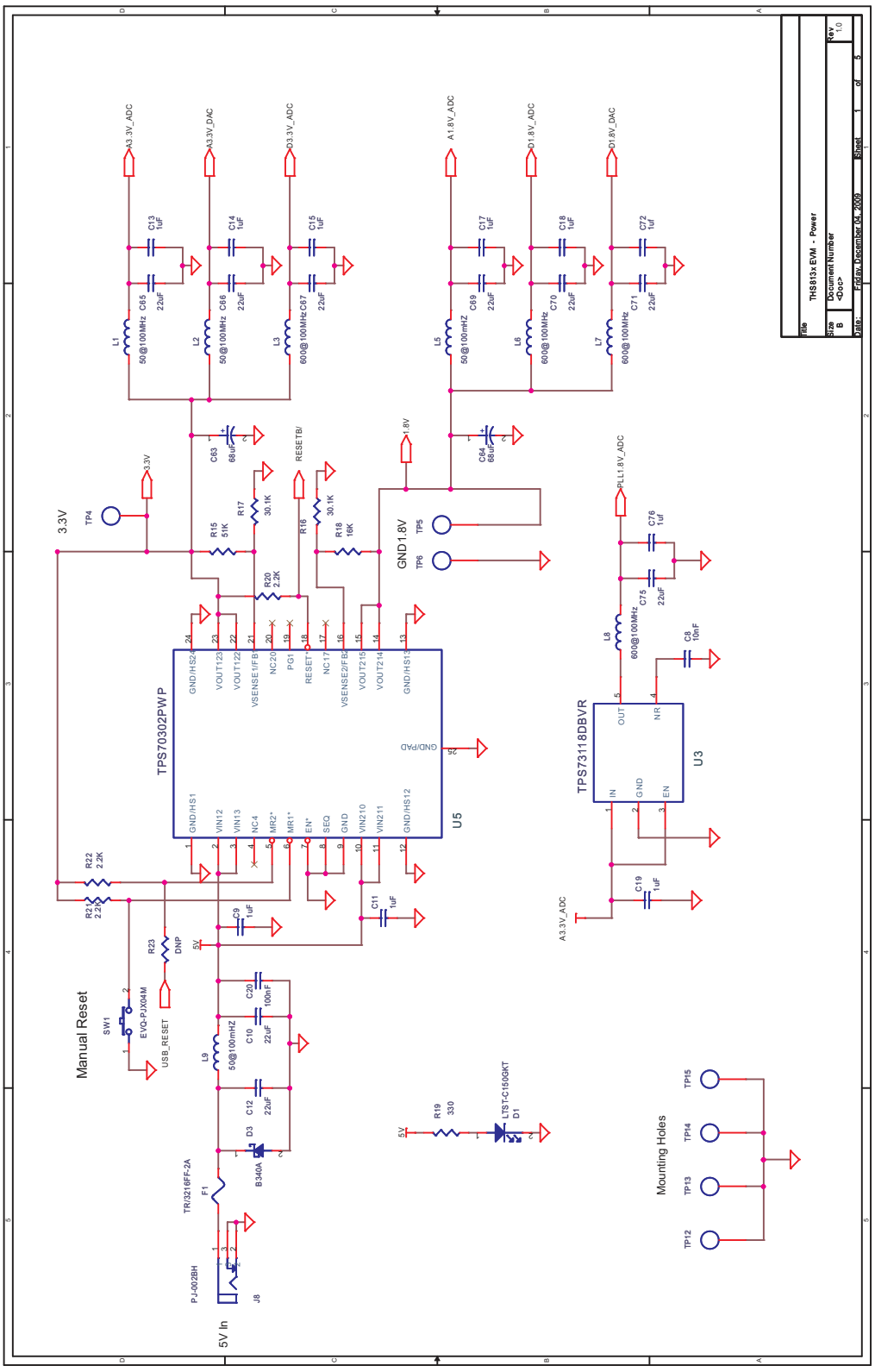

Figure 30. Schematic – Power

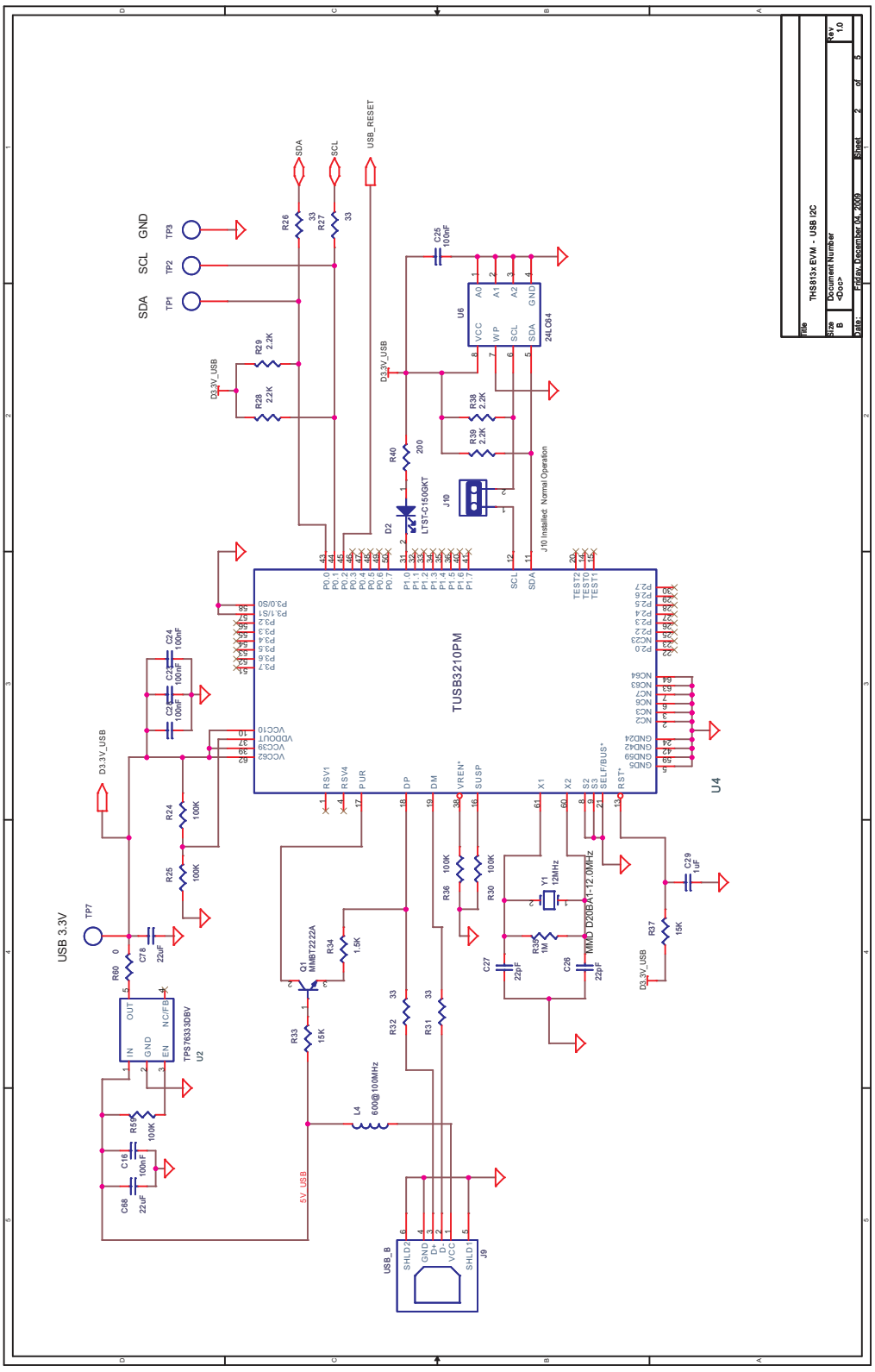

Figure 31. Schematic – USB I²C

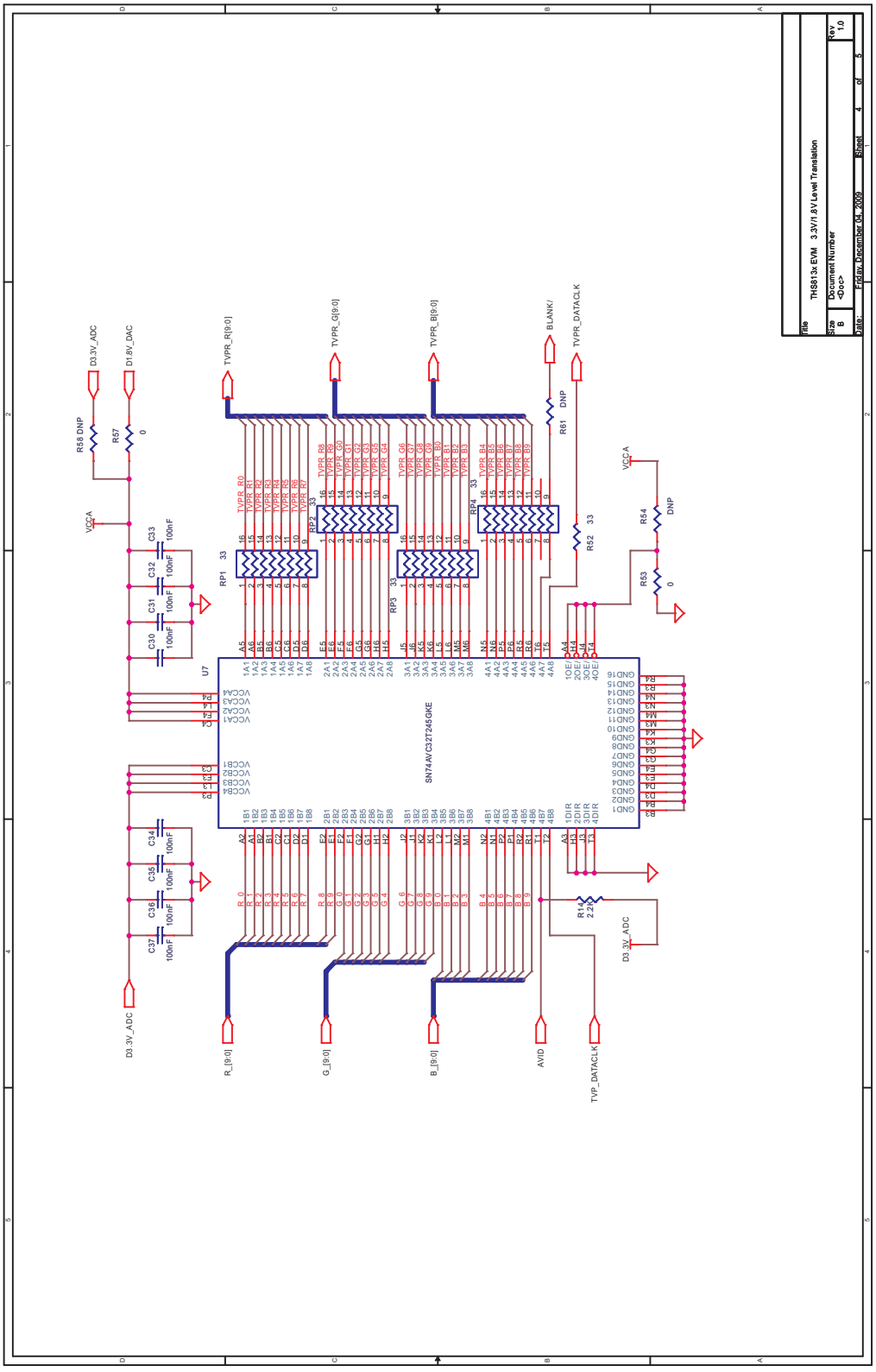

Figure 32. Schematic – 3.3-V/1.8-V Level Translation

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